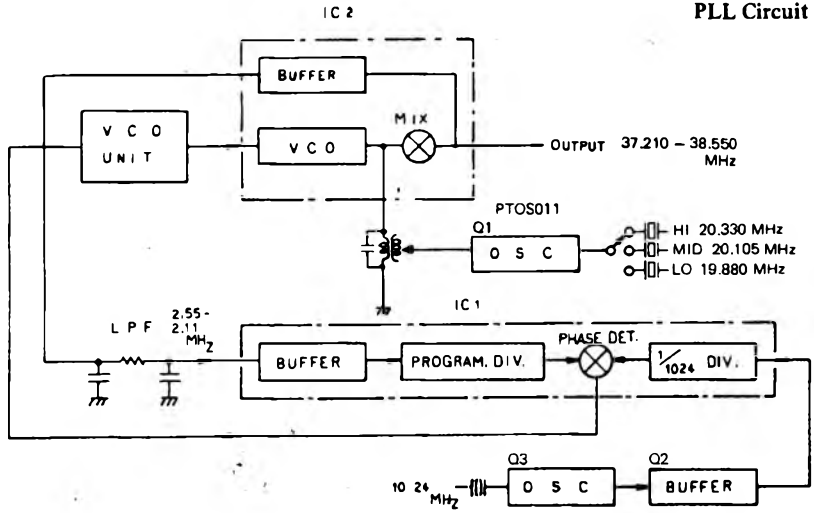
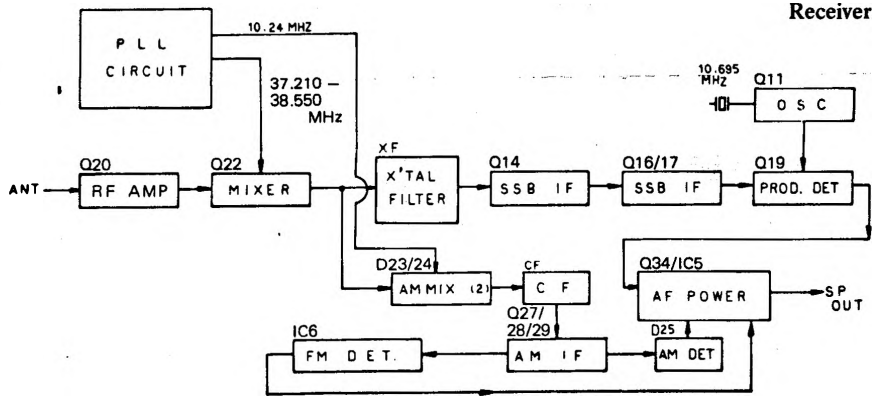


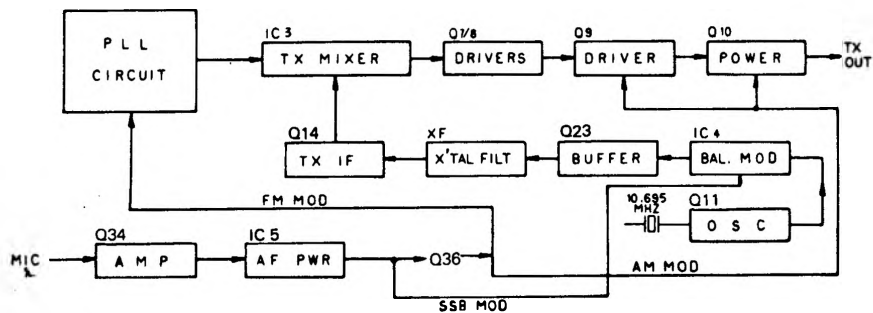
### PLL Circuit

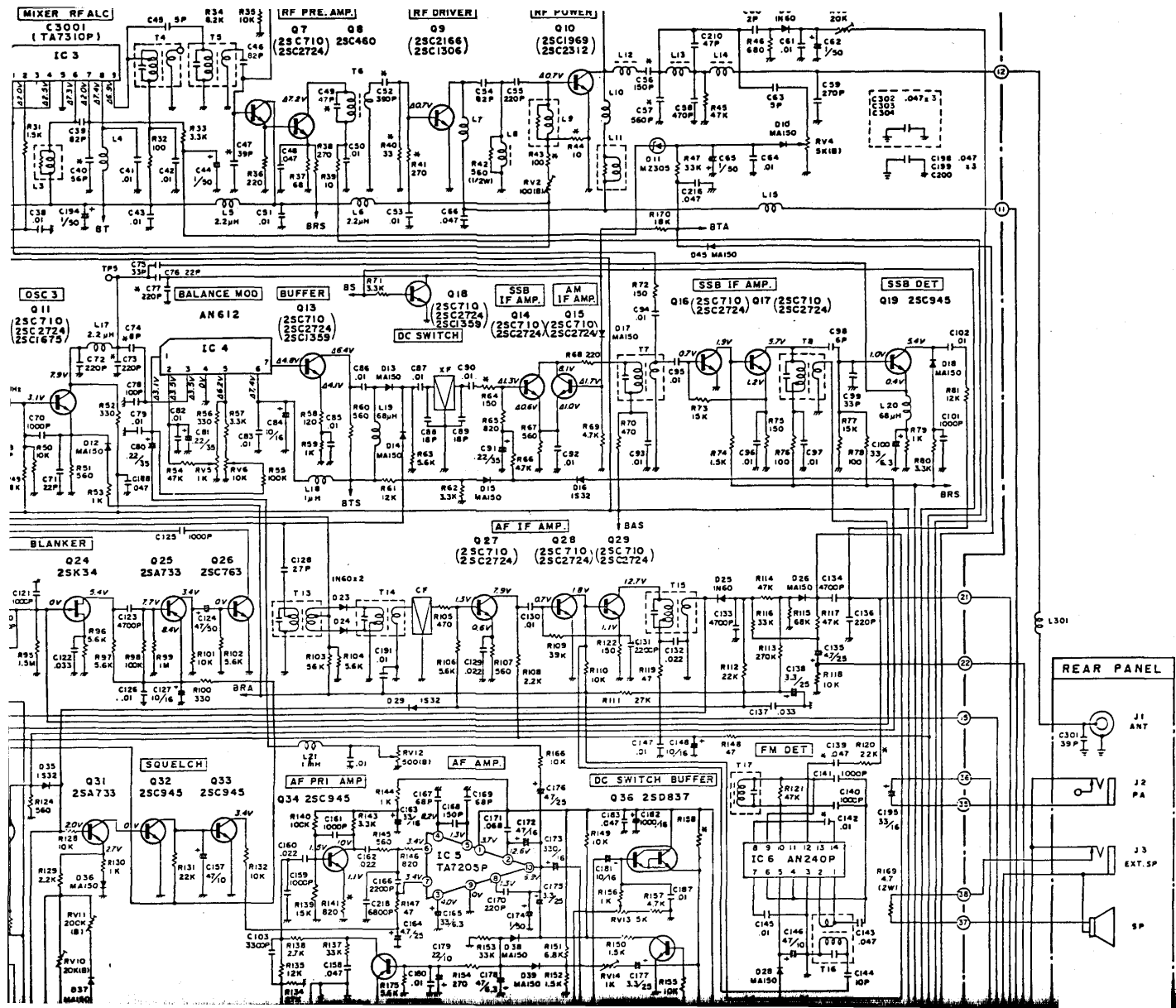


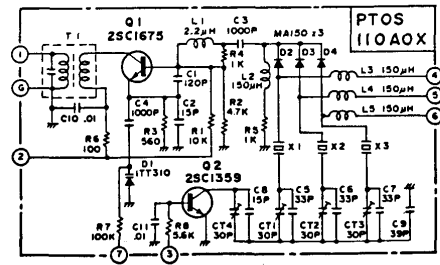
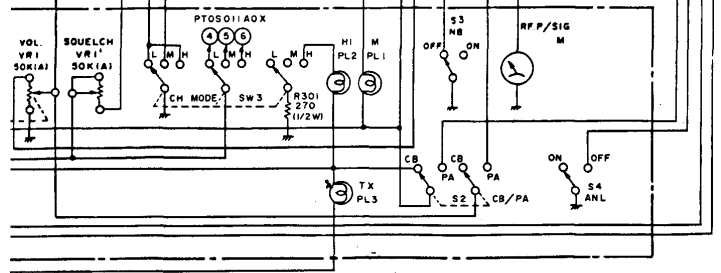
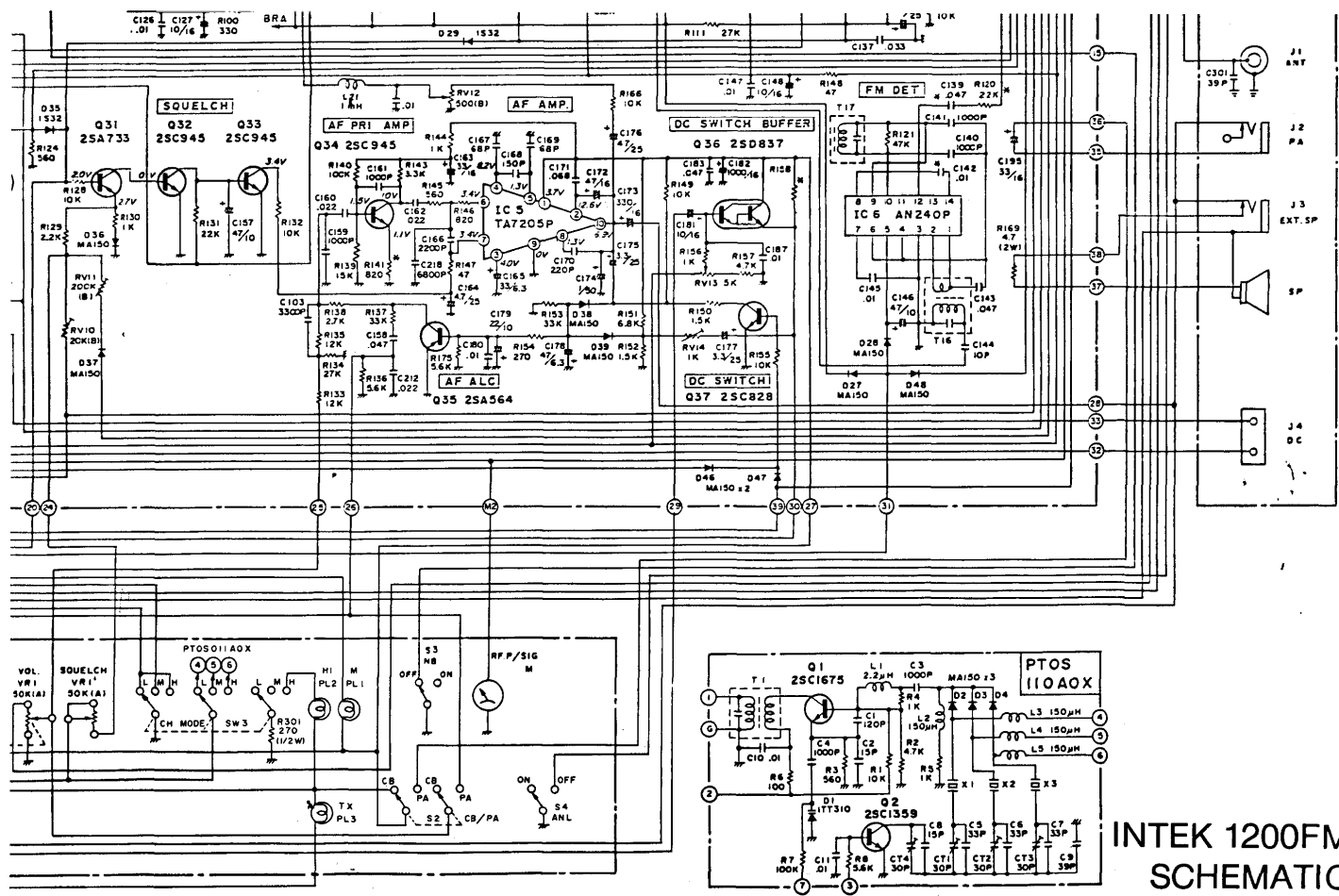
### Receiver



### Transmitter

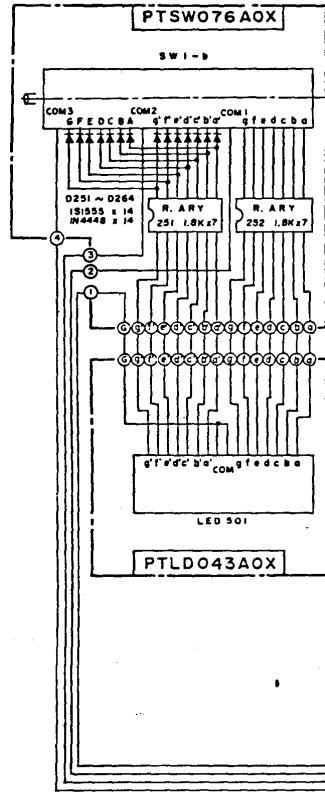






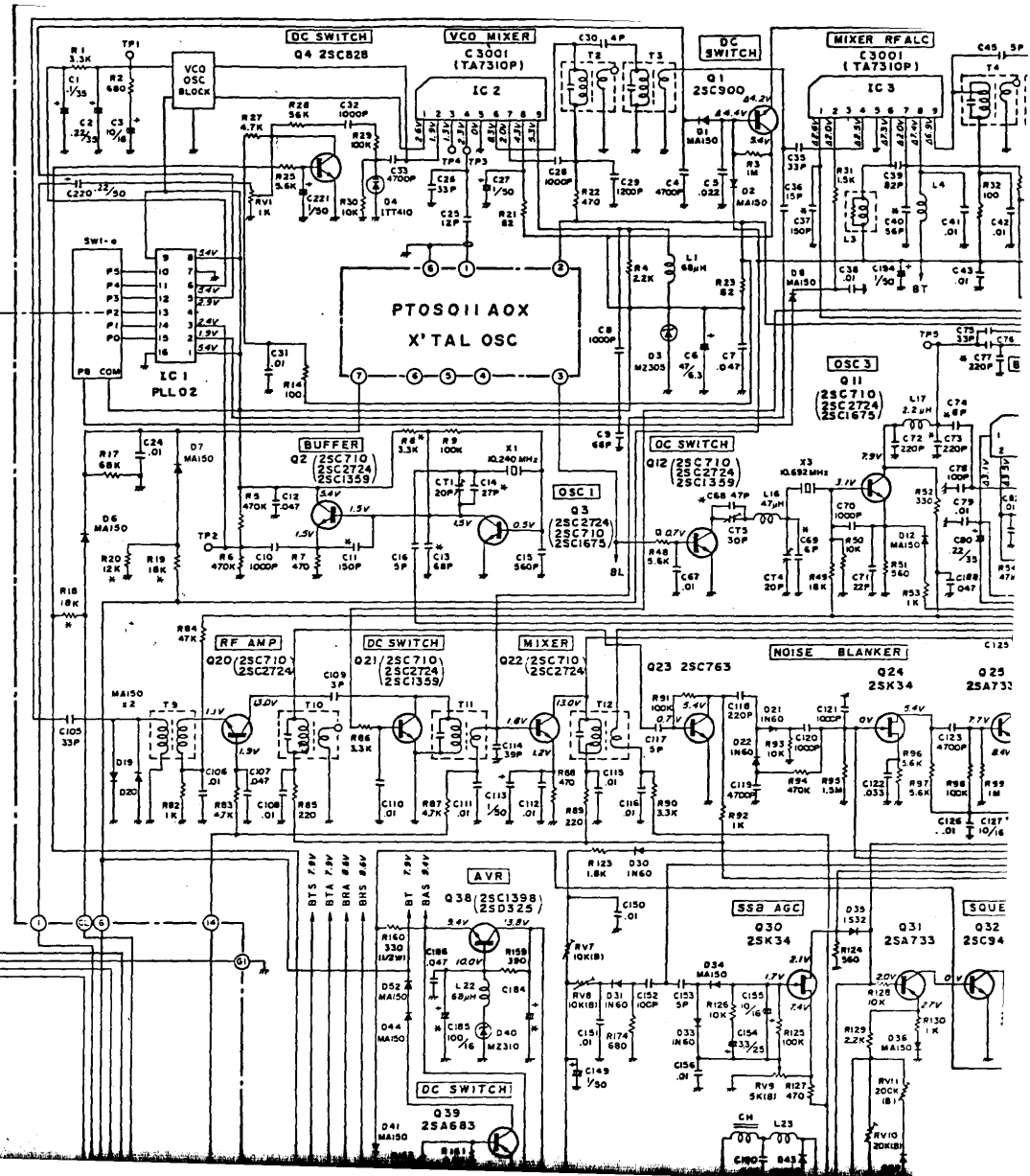
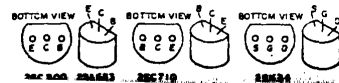
**INTEK 1200FM  
SCHEMATIC  
DIAGRAM**

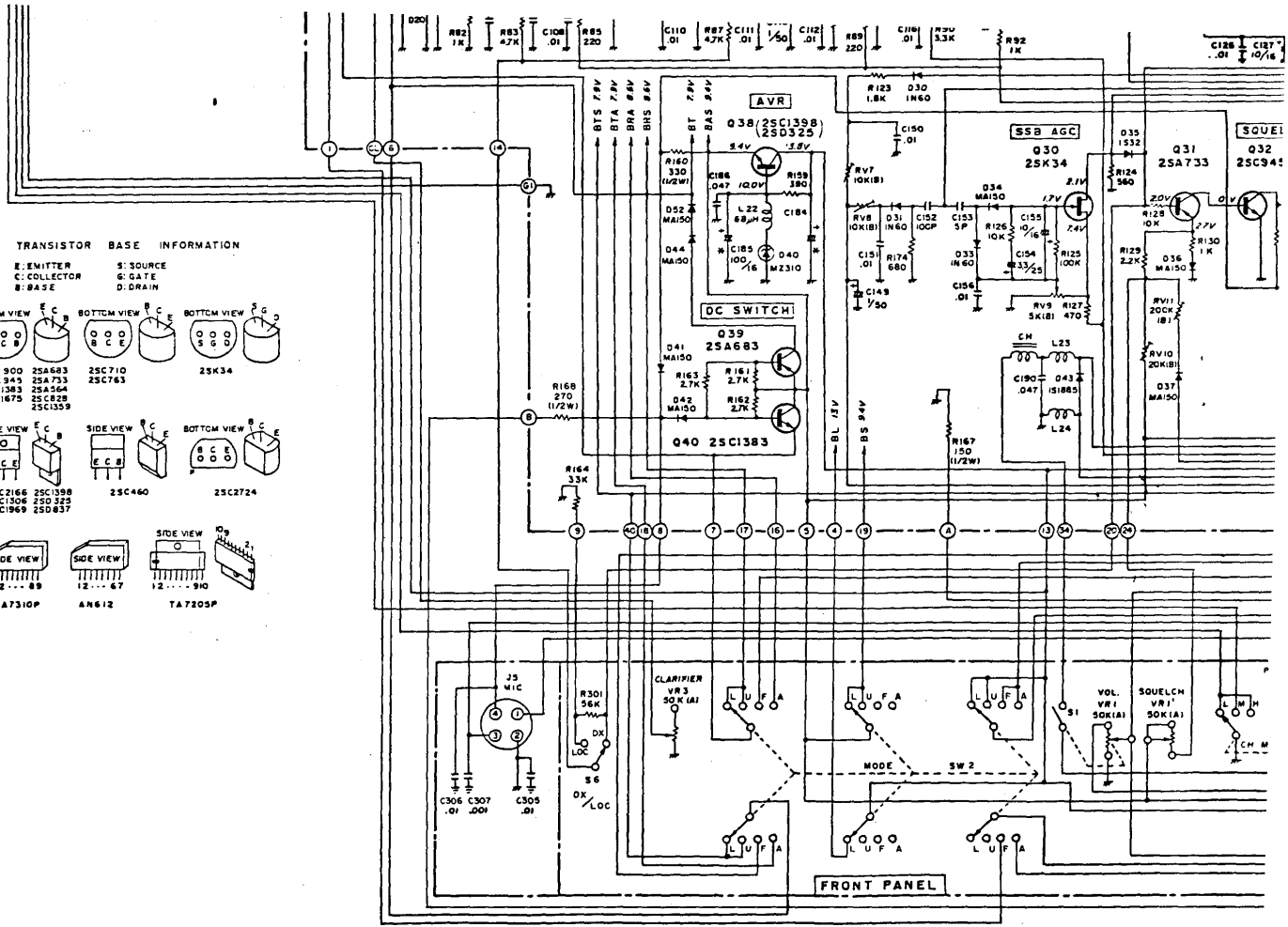
NOTE:  
 ALL VOLTAGES MEASURED FROM PC BOARD GROUND WITH D.C. VTVM AT NO SIGNAL (AT 13.8V POWER SUPPLY) IF MEASUREMENT VALUES OBTAINED ARE IN EXCESS OF 20% OF VALUES SHOWN, THEN REASON FOR DIFFERENCE SHOULD BE CORRECTED  
 \* TX : 0 LSB : 1 AM TX  
 † CHASSIS GND  
 \* PC BOARD GND  
 \* ADJUSTED (TYPICAL VALUE SHOWN)



TRANSISTOR BASE INFORMATION

E: EMITTER S: SOURCE  
 C: COLLECTOR G: GATE  
 B: BASE D: DRAIN

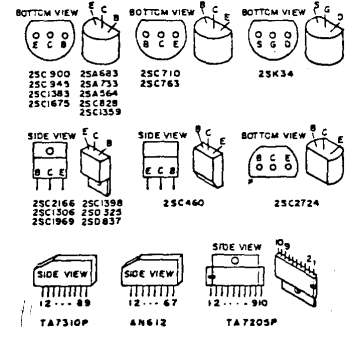




**TRANSISTOR BASE INFORMATION**

E: EMITTER  
C: COLLECTOR  
B: BASE

S: SOURCE  
G: GATE  
D: DRAIN



# PC Board Detail

Main Board

