Hi3670 V100 Application Processor

Data Sheet

Issue 01

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About This Document

Purpose

This document describes the basic functions and specifications of the Hi3670 V100.

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3670	V100

Intended Audience

This document is intended for:

- Technical support engineers
- Board hardware development engineers
- Software engineers

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
CAUTION	Alerts you to a potentially hazardous situation that could, if not avoided, result in equipment damage, data loss, performance deterioration, or unanticipated results.
NOTE	Provides additional information to emphasize or supplement important points in the main text.

Change History

Changes between document issues are cumulative. The latest document issue contains all the changes made in earlier issues.

Issue 01 (2018-03-02)

This issue is the first official release

Contents

1 Introduction

1.1 Major Features

1.1.1 Computing Capability

Core specifications of the Hi3670 computing capability are as follows:

- 8-core CPU, including four 2.36 GHz ARM Cortex-A73 MPCore high-performance cores and four 1.8 GHz ARM Cortex-A53 MPCore energy-efficient cores
- OPENGL ES3.2, OPENCL 1.2, OPENCL 2.0, Renderscript, and high-performance 3D acceleration technologies compressed by AFBC
- MMU management for all chip channels, reducing overhead of reserved memories
- 1866 MHz four-channel LPDDR4x
- AFBC compression and process optimization to reduce the DDR bandwidth
- Hardware acceleration for secure encryption and decryption using dual engines

1.1.2 Multimedia

Core specifications of the Hi3670 multimedia features are as follows:

- Built-in video hardware decoder (with the maximum rate of H.265 3840 x 2160@60 fps/H.264 3840 x 2160@30 fps)
- Built-in video hardware encoder (H.265/H.264 3840 x 2160@30 fps)
- Built-in Mali-G72 MP12 GPU
- Independent JPG codec and face detection acceleration module
- Maximum resolution of 3840 x 2400@60 Hz)
- Dual MIPI display interfaces

Table 1-1 describes the multimedia features of the Hi3670.

Table 1-1 Hi3670 multimedia features

Multimedia Feature	Description
GPU	

Multimedia Feature	Description
3D acceleration	• Supports OpenGL ES 1.1 and 2.0, OpenGL ES 3.0, OpenGL ES 3.1, and OpenGL ES 3.2. • Supports OpenCL 1.1, 1.2, and 2.0. • Renderscript • Vulkan 1.0
Camera input interface	Three MIPI CSI interfaces (D-PHY 4+4+4 lane or C-PHY 3+3+3 lane)
Image input format	1. Supports uncompressed RAW10, RAW12, and RAW14. 2. Supports RGB-IR input RAW10, RAW12, and RAW14 (2 MPs at 120 fps at most). 3. Supports phase data sensors. 4. Supports uncommon formats after storage conversion in bypass mode.
Storage format	Supports RAW10, RAW12, and RAW14. Data in these formats is stored in 2-byte alignment.
3A	Supports auto focus (AF), auto white balance (AWB), and auto exposure (AE).
Display	
Display pixel depth	RGB888 or RGB565
Display resolution	The maximum resolution is 3840 x 2400, with the refresh rate of 60 Hz.
MIPI interface	Supports dual MIPI display interfaces.
Display system	• Supports online multi-layer overlay, color key, alpha blending, and DIM. • Supports online resizing and offline resizing and rotation. • Supports the interface IFBC, IFBC and RSP integration, and VESA compression algorithms. • Supports online display post processing and color management. • Supports offline overlay for multiple layers, color key, alpha blending, and DIM. • Supports bus data compression and decompression.
Encoding and decoding	
Video encoding	Encoding format: H.265 or H.264 HD photographing: 3840 x 2400@30 fps 4 x 1080p@30 fps simultaneous HD encoding 720p 240 fps video, supporting fast recording and slow playback
Video decoding	• Supports multiple formats such as H.265 M10P@L5.1 and H.264 BP/MP/HP@L5.1. • Up to H.265 4K@60 fps and H.264 4K@30 fps
Audio	
Audio interface	Supports I^2S and PCM interfaces.
Audio sampling rate	8 kHz, 16 kHz, 32 kHz, 48 kHz, 96 kHz, or 192 kHz
Audio DSP	The HiFi3 DSP is used to process audio data.

1.1.3 Interfaces

Table 1-2 describes the peripheral interfaces of the Hi3670.

Table 1-2 Peripheral interfaces of the Hi3670

Interface Name	Description
USB interface	1. Supports the USB 3.0 over Type-C interface. 2. Supports BC1.2 battery charging.
PCIe interface	Supports PCIe1.1/x1.
Micro SD card interface	Supports SD 3.0 or SD 2.0 card.
I2C interface	Supports the high-speed I2C interface.
SPI	A maximum of 40 MHz (SPI3) is supported. For details about the frequency supported by the SPIs 0 to 4 in various scenarios, see section 8.3 SPI.
UART interface	Supports the high-speed UART interface.
GPIO interface	Supports various GPIO interfaces.

Table 1-3 describes the memory interfaces of the Hi3670.

Table 1-3 Hi3670 memory interfaces

Interface Name	Description
Flash	Supports UFS 2.0 and UFS 2.1.
DRAM	LPDDR4x: 1866 MHz

Table 1-4 describes the debugging interfaces of the Hi3670.

Table 1-4 Hi3670 debugging interfaces

Interface Name	Description
JTAG interface	The Hi3670 provides JTAG debugging interfaces that comply with IEEE Std 1149.1.

1.2 Chip Architecture

The Hi3670 uses the 10 nm fin field-effect transistor (FinFET) technology of TSMC, and features multiple cores, multiple modes, high performance, and high integration. The Hi3670 provides high-speed mobile computing capability, integrates rich multimedia processing functions and high-level communications processing functions, and adopts the industry-leading low power consumption technology, making it the core SoC chip of the Kirin 970 solution for high-end smartphones.

1.3 Typical Application

The Hi3670 is applied to products such as smartphones and tablets.

2 Description

2.1 Interrupt

2.1.1 Function Description

The ACPU uses the GIC to handle and control interrupts. Other microcontrollers and media and communication processors have their own interrupt handling logic. This section describes the basic interrupt handling functions of the GIC.

The GIC has the following basic features:

- Supports interrupt nesting.
- Manages the multi-core interrupt distribution.
- Supports security extension.
- Supports query of the states of interrupt sources.
- Provides a unique ID for each interrupt.
- Supports configurable interrupt trigger mode: high-level-triggered mode or edge-triggered mode.
- Sets the priority of each interrupt.
- Generates software interrupts.

2.1.2 Interrupt Mapping

Table 2-1 describes interrupt sources and interrupt signals of the GIC.

Table 2-1 GIC interrupt allocation

Interrupt Source	GIC Interrupt ID	Interrupt Source	GIC Interrupt ID
A73_interr	32	intr_ipc_ns_ao[1]	205
A73_exterr	33	intr_lpmcu_wdog	206
A73_pmu0	34	–CCI400_err	207
A73_pmu1	35	–&CCI400_overflow[6:0]	208
A73_pmu2	36	–CCI400_overflow[7]	209

Interrupt Source	GIC Interrupt ID	Interrupt Source	GIC Interrupt ID
A73_pmu3	37	IPC_S_int0	210
A73_cti0	38	IPC_S_int1	211
A73_cti1	39	IPC_S_int4	212
A73_cti2	40	IPC_S_mbx0	213
A73_cti3	41	IPC_S_mbx1	214
A73_COMMRX0	42	IPC_S_mbx2	215
A73_COMMRX1	43	IPC_S_mbx3	216
A73_COMMRX2	44	IPC_S_mbx4	217
A73_COMMRX3	45	IPC_S_mbx5	218
A73_COMMTX0	46	IPC_S_mbx6	219
A73_COMMTX1	47	IPC_S_mbx7	220
A73_COMMTX2	48	IPC_S_mbx8	221
A73_COMMTX3	49	IPC_S_mbx9	222
A73_COMMIRQ0	50	IPC_S_mbx18	223
A73_COMMIRQ1	51	IPC_NS_int0	224
A73_COMMIRQ2	52	IPC_NS_int1	225
A73_COMMIRQ3	53	IPC_NS_int4	226
A53_interr	54	IPC_NS_int5	227
A53_exterr	55	IPC_NS_int6	228
A53_pmu0	56	IPC_NS_mbx0	229
A53_pmu1	57	IPC_NS_mbx1	230
A53_pmu2	58	IPC_NS_mbx2	231
A53_pmu3	59	IPC_NS_mbx3	232
A53_cti0	60	IPC_NS_mbx4	233
A53_cti1	61	IPC_NS_mbx5	234
A53_cti2	62	IPC_NS_mbx6	235
A53_cti3	63	IPC_NS_mbx7	236
A53_COMMRX0	64	IPC_NS_mbx8	237
A53_COMMRX1	65	IPC_NS_mbx9	238
A53_COMMRX2	66	IPC_NS_mbx18	239

Interrupt Source	GIC Interrupt ID	Interrupt Source	GIC Interrupt ID
A53_COMMRX3	67	Reserved	240
A53_COMMTX0	68	Reserved	241
A53_COMMTX1	69	ASP-IPC-ARM	242
A53_COMMTX2	70	Reserved	243
A53_COMMTX3	71	Reserved	244
A53_COMMIRQ0	72	intr_asp_watchdog	245
A53_COMMIRQ1	73	ASP_AXI_DLOCK	246
A53_COMMIRQ2	74	Reserved	247
A53_COMMIRQ3	75	Reserved	248

2.2 Memory Mapping

Table 2-2 lists the address ranges of the ACPU of the Hi3670.

Table 2-2 Space and address allocation

Address	Space Capacity (byte)	Applicable Module
0xFFFF0000–0xFFFFFFFF	64K	Reserved
0xFFFE0000–0xFFFEFFFF	64K	Reserved
0xFFFC0000–0xFFFDFFFF	128K	DMSS
0xFFFB0000–0xFFFBFFFF	64K	Reserved
0xFFFA0000–0xFFFAFFFF	64K	Reserved
0xFFF80000–0xFFF9FFFF	128K	Reserved
0xFFF7E000–0xFFF7FFFF	8K	Reserved
0xFFF62000–0xFFF7DFFF	112K	Reserved
0xFFF50000–0xFFF61FFF	72K	Reserved
0xFFF40000–0xFFF4FFFF	64K	Reserved
0xFFF3F000–0xFFF3FFFF	4K	Reserved
0xFFF3E000–0xFFF3EFFF	4K	LP_TIMER
0xFFF3D000–0xFFF3DFFF	4K	LP_WDG
0xFFF3A000–0xFFF3CFFF	12K	Reserved

Address	Space Capacity (byte)	Applicable Module
0xFFF39000–0xFFF39FFF	4K	Reserved
0xFFF38000–0xFFF38FFF	4K	Reserved
0xFFF37000–0xFFF37FFF	4K	Reserved
0xFFF36000–0xFFF36FFF	4K	PMU_I2C1
0xFFF35000–0xFFF35FFF	4K	PERI_CRG
0xFFF34000–0xFFF34FFF	4K	PMU_SSI0
0xFFF33000–0xFFF33FFF	4K	PMU_I2C0
0xFFF32000–0xFFF32FFF	4K	UART6
0xFFF31000–0xFFF31FFF	4K	PMC
0xFFF30000–0xFFF30FFF	4K	TSENSORC
0xFFF2F000–0xFFF2FFFF	4K	Reserved
0xFFF2B000–0xFFF2EFFF	16K	Reserved
0xFFF2A000–0xFFF2AFFF	4K	SPI3
0xFFF29000–0xFFF29FFF	4K	GPIO19
0xFFF28000–0xFFF28FFF	4K	GPIO18
0xFFF24000–0xFFF27FFF	16K	SPMI
0xFFF23000–0xFFF23FFF	4K	Reserved
0xFFF22000–0xFFF22FFF	4K	AO_IPC_NS
0xFFF21000–0xFFF21FFF	4K	Reserved
0xFFF20000–0xFFF20FFF	4K	Reserved
0xFFF1F000–0xFFF1FFFF	4K	Reserved
0xFFF1E000–0xFFF1EFFF	4K	Reserved
0xFFF1D000–0xFFF1DFFF	4K	GPIO28
0xFFF1C000–0xFFF1CFFF	4K	TIMER8
0xFFF1B000–0xFFF1BFFF	4K	TIMER7
0xFFF1A000–0xFFF1AFFF	4K	TIMER6
0xFFF19000–0xFFF19FFF	4K	TIMER5
0xFFF18000–0xFFF18FFF	4K	TIMER4
0xFFF17000–0xFFF17FFF	4K	TIMER3
0xFFF16000–0xFFF16FFF	4K	TIMER2
0xFFF15000–0xFFF15FFF	4K	TIMER1

Address	Space Capacity (byte)	Applicable Module
0xFFF14000–0xFFF14FFF	4K	TIMER0
0xFFF12000–0xFFF13FFF	8K	BB_DRX
0xFFF11000–0xFFF11FFF	4K	AO_IOC
0xFFF10000–0xFFF10FFF	4K	GPIO27
0xFFF0F000–0xFFF0FFFF	4K	GPIO26
0xFFF0E000–0xFFF0EFFF	4K	GPIO25
0xFFF0D000–0xFFF0DFFF	4K	GPIO24
0xFFF0C000–0xFFF0CFFF	4K	GPIO23
0xFFF0B000–0xFFF0BFFF	4K	GPIO22
0xFFF0A000–0xFFF0AFFF	4K	SCTRL
0xFFF08000–0xFFF09FFF	8K	SYS_CNT
0xFFF07000–0xFFF07FFF	4K	Reserved
0xFFF06000–0xFFF06FFF	4K	Reserved
0xFFF05000–0xFFF05FFF	4K	RTC1
0xFFF04000–0xFFF04FFF	4K	RTC0
0xFFF03000–0xFFF03FFF	4K	Reserved
0xFFF02000–0xFFF02FFF	4K	Reserved
0xFFF01000–0xFFF01FFF	4K	Reserved
0xFFF00000–0xFFF00FFF	4K	Reserved
0xFFE00000–0xFFEFFFFF	1M	Reserved
0xFFD80000–0xFFDFFFFF	512K	Reserved
0xFFD7F000–0xFFD7FFFF	4K	Reserved
0xFFD7E000–0xFFD7EFFF	4K	Reserved
0xFFD7D000–0xFFD7DFFF	4K	Reserved
0xFFD7C000–0xFFD7CFFF	4K	Reserved
0xFFD7B000–0xFFD7BFFF	4K	IOMCU_GPIO3
0xFFD7A000–0xFFD7AFFF	4K	IOMCU_GPIO2
0xFFD79000–0xFFD79FFF	4K	IOMCU_GPIO1
0xFFD78000–0xFFD78FFF	4K	IOMCU_GPIO0
0xFFD77000–0xFFD77FFF	4K	IOMCU_DMAC
0xFFD76000–0xFFD76FFF	4K	IOMCU_UART7

Address	Space Capacity (byte)	Applicable Module
0xFFD75000–0xFFD75FFF	4K	IOMCU_BLPWM
0xFFD74000–0xFFD74FFF	4K	IOMCU_UART3
0xFFD73000–0xFFD73FFF	4K	IOMCU_I2C2
0xFFD72000–0xFFD72FFF	4K	IOMCU_I2C1
0xFFD71000–0xFFD71FFF	4K	IOMCU_I2C0
0xFFD70000–0xFFD70FFF	4K	IOMCU_SPI0
0xFFD6F000–0xFFD6FFFF	4K	Reserved
0xFFD6E000–0xFFD6EFFF	4K	Reserved
0xFFD6C000–0xFFD6DFFF	8K	Reserved
0xFFD6B000–0xFFD6BFFF	4K	Reserved
0xFFD6A000–0xFFD6AFFF	4K	IOMCU_I2C3
0xFFD69000–0xFFD69FFF	4K	IOMCU_UART8
0xFFD68000–0xFFD68FFF	4K	IOMCU_SPI2
0xFFD67000–0xFFD67FFF	4K	Reserved
0xFFD66000–0xFFD66FFF	4K	IOMCU_TIMER2
0xFFD65000–0xFFD65FFF	4K	IOMCU_I3C
0xFFD08000–0xFFD64FFF	372K	Reserved
0xFFD03000–0xFFD07FFF	20K	Reserved
0xFFD01000–0xFFD02FFF	8K	Reserved
0xFFD00000–0xFFD00FFF	4K	Reserved
0xFF800000–0xFFCFFFFF	5M	Reserved
0xFF400000–0xFF7FFFFF	4M	ICS
0xFF3E1000–0xFF3FFFFF	124K	Reserved
0xFF3E0000–0xFF3E0FFF	4K	UFS_SYS_CTRL
0xFF3C0000–0xFF3DFFFF	128K	UFS_CFG
0xFF380000–0xFF3BFFFF	256K	Reserved
0xFF37F000–0xFF37FFFF	4K	SD3
0xFF37E000–0xFF37EFFF	4K	IOC_MMC0
0xFF37D000–0xFF37DFFF	4K	MMC0_SYS_CTRL
0xFF360000–0xFF37CFFF	116K	Reserved
0xFF340000–0xFF35FFFF	128K	DP_CTRL

Address	Space Capacity (byte)	Applicable Module
0xFF300000–0xFF33FFFF	256K	Reserved
0xFF201000–0xFF2FFFFF	1020K	Reserved
0xFF200000–0xFF200FFF	4K	USB3OTG_BC
0xFF100000–0xFF1FFFFF	1M	USB3OTG
0xFF080000–0xFF0FFFFF	512K	Reserved
0xFF060000–0xFF07FFFF	128K	Reserved
0xFF050000–0xFF05FFFF	64K	Reserved
0xFF040000–0xFF04FFFF	64K	Reserved
0xFF038000–0xFF03FFFF	32K	Reserved
0xFF034000–0xFF037FFF	16K	Reserved
0xFF032000–0xFF033FFF	8K	Reserved
0xFF030000–0xFF031FFF	8K	Reserved
0xFF013000–0xFF02FFFF	116K	Reserved
0xFF012000–0xFF012FFF	4K	Reserved
0xFF011000–0xFF011FFF	4K	Reserved
0xFF010000–0xFF010FFF	4K	Reserved
0xFF00F000–0xFF00FFFF	4K	Reserved
0xFF000000–0xFF00EFFF	60K	Reserved
0xFE000000–0xFEFFFFFF	16M	CS_STM
0xFDF31000–0xFDFFFFFF	828K	Reserved
0xFDF30000–0xFDF30FFF	4K	PERI_DMAC
0xFDF20000–0xFDF2FFFF	64K	Reserved
0xFDF18000–0xFDF1FFFF	32K	Reserved
0xFDF14000–0xFDF17FFF	16K	Reserved
0xFDF12000–0xFDF13FFF	8K	Reserved
0xFDF11000–0xFDF11FFF	4K	Reserved
0xFDF10000–0xFDF10FFF	4K	PERF_STAT
0xFDF0F000–0xFDF0FFFF	4K	Reserved
0xFDF0E000–0xFDF0EFFF	4K	Reserved
0xFDF0D000–0xFDF0DFFF	4K	I2C4
0xFDF0C000–0xFDF0CFFF	4K	I2C3

Address	Space Capacity (byte)	Applicable Module
0xFDF0B000–0xFDF0BFFF	4K	I2C7
0xFDF09000–0xFDF0AFFF	8K	Reserved
0xFDF08000–0xFDF08FFF	4K	SPI1
0xFDF07000–0xFDF07FFF	4K	Reserved
0xFDF06000–0xFDF06FFF	4K	SPI4
0xFDF05000–0xFDF05FFF	4K	UART5
0xFDF04000–0xFDF04FFF	4K	Reserved
0xFDF03000–0xFDF03FFF	4K	UART2
0xFDF02000–0xFDF02FFF	4K	UART0
0xFDF01000–0xFDF01FFF	4K	UART4
0xFDF00000–0xFDF00FFF	4K	UART1
0xFC200000–0xFDEFFFFF	29M	Reserved
0xFC186000–0xFC1FFFFF	488K	Reserved
0xFC185000–0xFC185FFF	4K	Reserved
0xFC184000–0xFC184FFF	4K	Reserved
0xFC183000–0xFC183FFF	4K	SDIO0
0xFC182000–0xFC182FFF	4K	IOC_MMC1
0xFC181000–0xFC181FFF	4K	Reserved
0xFC180000–0xFC180FFF	4K	PCIE0_APB_CFG
0xFC100000–0xFC17FFFF	512K	Reserved
0xFC080000–0xFC0FFFFF	512K	Reserved
0xFC000000–0xFC07FFFF	512K	PCIEPHY0
0xF8000000–0xFBFFFFFF	64M	Reserved
0xF4000000–0xF7FFFFFF	64M	PCIECtrl0
0xF3F00000–0xF3FFFFFF	1024K	Reserved
0xF1300000–0xF3EFFFFF	44M	Reserved
0xF12F0000–0xF12FFFFF	64K	Reserved
0xF1110000–0xF12EFFFF	1920K	Reserved
0xF110F000–0xF110FFFF	4K	Reserved
0xF110E000–0xF110EFFF	4K	Reserved
0xF110D000–0xF110DFFF	4K	Reserved

Address	Space Capacity (byte)	Applicable Module
0xF110C000–0xF110CFFF	4K	Reserved
0xF110B000–0xF110BFFF	4K	Reserved
0xF110A000–0xF110AFFF	4K	Reserved
0xF1109000–0xF1109FFF	4K	Reserved
0xF1108000–0xF1108FFF	4K	Reserved
0xF1104000–0xF1107FFF	16K	Reserved
0xF1100000–0xF1103FFF	16K	Reserved
0xF1000000–0xF10FFFFF	1M	Reserved
0xF0E31000–0xF0FFFFFF	1852K	Reserved
0xF0E30000–0xF0E30FFF	4K	Reserved
0xF0E24000–0xF0E2FFFF	48K	Reserved
0xF0E20000–0xF0E23FFF	16K	Reserved
0xF0E00000–0xF0E1FFFF	128K	Reserved
0xF0C00000–0xF0DFFFFF	2M	Reserved
0xF0000000–0xF0BFFFFF	12M	Reserved
0xED800000–0xEFFFFFFF	40M	Reserved
0xEC000000–0xED7FFFFF	24M	CSSYS_APB
0xEAC00000–0xEBFFFFFF	20M	Reserved
0xEA980000–0xEABFFFFF	2560K	Reserved
0xEA960000–0xEA97FFFF	128K	Reserved
0xEA940000–0xEA95FFFF	128K	Reserved
0xEA920000–0xEA93FFFF	128K	Reserved
0xEA900000–0xEA91FFFF	128K	Reserved
0xEA600000–0xEA8FFFFF	3M	Reserved
0xEA400000–0xEA5FFFFF	2M	Reserved
0xEA000000–0xEA3FFFFF	4M	Reserved
0xE9900000–0xE9FFFFFF	7M	Reserved
0xE98A0000–0xE98FFFFF	384K	Reserved
0xE9890000–0xE989FFFF	64K	MMC0_NOC_Service_Target
0xE9880000–0xE988FFFF	64K	MMC1_NOC_Service_Target
0xE9870000–0xE987FFFF	64K	AOBUS_Service_Target

Address	Space Capacity (byte)	Applicable Module
0xE9860000–0xE986FFFF	64K	DMA_NOC_Service_Target
0xE9850000–0xE985FFFF	64K	Reserved
0xE9840000–0xE984FFFF	64K	SYS_BUS_Service_Target
0xE9830000–0xE983FFFF	64K	ASP_Service_Target
0xE9820000–0xE982FFFF	64K	Reserved
0xE9810000–0xE981FFFF	64K	Reserved
0xE9800000–0xE980FFFF	64K	CFGBUS_Service_Target
0xE8E00000–0xE97FFFFF	10M	Reserved
0xE8DD0000–0xE8DFFFFF	192K	Reserved
0xE8DC0000–0xE8DCFFFF	64K	Reserved
0xE8D86000–0xE8DBFFFF	232K	Reserved
0xE8D85000–0xE8D85FFF	4K	Reserved
0xE8D84000–0xE8D84FFF	4K	Reserved
0xE8D83000–0xE8D83FFF	4K	Reserved
0xE8D82000–0xE8D82FFF	4K	Reserved
0xE8D81000–0xE8D81FFF	4K	Reserved
0xE8D80000–0xE8D80FFF	4K	Reserved
0xE8D08000–0xE8D7FFFF	480K	Reserved
0xE8D00000–0xE8D07FFF	32K	Reserved
0xE8CB0000–0xE8CFFFFF	320K	Reserved
0xE8C80000–0xE8CAFFFF	192K	Reserved
0xE8C30000–0xE8C7FFFF	320K	Reserved
0xE8C00000–0xE8C2FFFF	192K	Reserved
0xE8B00000–0xE8BFFFFF	1M	Reserved
0xE8A24000–0xE8AFFFFF	880K	Reserved
0xE8A23000–0xE8A23FFF	4K	Reserved
0xE8A22000–0xE8A22FFF	4K	Reserved
0xE8A21000–0xE8A21FFF	4K	Reserved
0xE8A20000–0xE8A20FFF	4K	GPIO21
0xE8A1F000–0xE8A1FFFF	4K	GPIO20
0xE8A1E000–0xE8A1EFFF	4K	Reserved

Address	Space Capacity (byte)	Applicable Module
0xE8A1D000–0xE8A1DFFF	4K	Reserved
0xE8A1C000–0xE8A1CFFF	4K	GPIO17
0xE8A1B000–0xE8A1BFFF	4K	GPIO16
0xE8A1A000–0xE8A1AFFF	4K	GPIO15
0xE8A19000–0xE8A19FFF	4K	GPIO14
0xE8A18000–0xE8A18FFF	4K	GPIO13
0xE8A17000–0xE8A17FFF	4K	GPIO12
0xE8A16000–0xE8A16FFF	4K	GPIO11
0xE8A15000–0xE8A15FFF	4K	GPIO10
0xE8A14000–0xE8A14FFF	4K	GPIO9
0xE8A13000–0xE8A13FFF	4K	GPIO8
0xE8A12000–0xE8A12FFF	4K	GPIO7
0xE8A11000–0xE8A11FFF	4K	GPIO6
0xE8A10000–0xE8A10FFF	4K	GPIO5
0xE8A0F000–0xE8A0FFFF	4K	GPIO4
0xE8A0E000–0xE8A0EFFF	4K	GPIO3
0xE8A0D000–0xE8A0DFFF	4K	GPIO2
0xE8A0C000–0xE8A0CFFF	4K	GPIO1
0xE8A0B000–0xE8A0BFFF	4K	GPIO0
0xE8A0A000–0xE8A0AFFF	4K	Reserved
0xE8A09000–0xE8A09FFF	4K	PCTRL
0xE8A08000–0xE8A08FFF	4K	Reserved
0xE8A07000–0xE8A07FFF	4K	WD1
0xE8A06000–0xE8A06FFF	4K	WD0
0xE8A05000–0xE8A05FFF	4K	Reserved
0xE8A04000–0xE8A04FFF	4K	PWM
0xE8A03000–0xE8A03FFF	4K	TIMER12
0xE8A02000–0xE8A02FFF	4K	TIMER11
0xE8A01000–0xE8A01FFF	4K	TIMER10
0xE8A00000–0xE8A00FFF	4K	TIMER9
0xE8970000–0xE89FFFFF	576K	Reserved

Address	Space Capacity (byte)	Applicable Module
0xE896D000–0xE896FFFF	12K	Reserved
0xE896C000–0xE896CFFF	4K	IOC
0xE896B000–0xE896BFFF	4K	IPC_NS
0xE896A000–0xE896AFFF	4K	Reserved
0xE8960000–0xE8969FFF	40K	Reserved
0xE8950000–0xE895FFFF	64K	Reserved
0xE8940000–0xE894FFFF	64K	NOC_VENC_Service_Target
0xE8930000–0xE893FFFF	64K	NOC_VDEC_Service_Target
0xE8920000–0xE892FFFF	64K	NOC_VCODECBUS_Service_Target
0xE8901000–0xE891FFFF	124K	Reserved
0xE8900000–0xE8900FFF	4K	MEDIA2_CRG
0xE88C0000–0xE88FFFFF	256K	Reserved
0xE8880000–0xE88BFFFF	256K	VENC
0xE8840000–0xE887FFFF	256K	Reserved
0xE8800000–0xE883FFFF	256K	VDEC
0xE87FF000–0xE87FFFFF	4K	MEDIA1_CRG
0xE87A0000–0xE87FEFFF	380K	Reserved
0xE8700000–0xE879FFFF	640K	MEDIA_COMMON
0xE86F0000–0xE86FFFFF	64K	Reserved
0xE86E0000–0xE86EFFFF	64K	Reserved
0xE86D0000–0xE86DFFFF	64K	Reserved
0xE86C0000–0xE86CFFFF	64K	Reserved
0xE86A0000–0xE86BFFFF	128K	Reserved
0xE8690000–0xE869FFFF	64K	Reserved
0xE8680000–0xE868FFFF	64K	DBCU0_SMMU
0xE867F000–0xE867FFFF	4K	Reserved
0xE867E000–0xE867EFFF	4K	LDI1
0xE867DC00–0xE867DFFF	1K	DSC
0xE867D800–0xE867DBFF	1K	IFBC
0xE867D400–0xE867D7FF	1K	Reserved

Address	Space Capacity (byte)	Applicable Module
0xE867D000–0xE867D3FF	1K	LDI0
0xE867C000–0xE867CFFF	4K	DPP_SBL
0xE8670000–0xE867BFFF	48K	DPP
0xE866F000–0xE866FFFF	4K	DPE
0xE866E000–0xE866EFFF	4K	DBUF1
0xE866D000–0xE866DFFF	4K	DBUF0
0xE8661000–0xE866CFFF	48K	Reserved
0xE8660C00–0xE8660FFF	1K	Reserved
0xE8660800–0xE8660BFF	1K	Reserved
0xE8660400–0xE86607FF	1K	Reserved
0xE8660000–0xE86603FF	1K	Reserved
0xE865C000–0xE865FFFF	16K	Reserved
0xE865B000–0xE865BFFF	4K	Reserved
0xE865A000–0xE865AFFF	4K	Reserved
0xE8654000–0xE8659FFF	24K	Reserved
0xE8653000–0xE8653FFF	4K	Reserved
0xE8652000–0xE8652FFF	4K	Reserved
0xE8651000–0xE8651FFF	4K	Reserved
0xE8650000–0xE8650FFF	4K	Reserved
0xE8648000–0xE864FFFF	32K	Reserved
0xE8640000–0xE8647FFF	32K	Reserved
0xE8638000–0xE863FFFF	32K	Reserved
0xE8630000–0xE8637FFF	32K	Reserved
0xE8628000–0xE862FFFF	32K	Reserved
0xE8620000–0xE8627FFF	32K	Reserved
0xE8613000–0xE861FFFF	52K	Reserved
0xE8612000–0xE8612FFF	4K	Reserved
0xE8611000–0xE8611FFF	4K	DBUG
0xE8610800–0xE8610FFF	2K	Reserved
0xE8610000–0xE86107FF	2K	Reserved
0xE860B000–0xE860FFFF	20K	Reserved

Address	Space Capacity (byte)	Applicable Module
0xE860A000–0xE860AFFF	4K	Reserved
0xE8609000–0xE8609FFF	4K	Reserved
0xE8608000–0xE8608FFF	4K	Reserved
0xE8607000–0xE8607FFF	4K	Reserved
0xE8603400–0xE8606FFF	15K	Reserved
0xE8602000–0xE86033FF	5K	Reserved
0xE8601C00–0xE8601FFF	1K	Reserved
0xE8601800–0xE8601BFF	1K	Reserved
0xE8601600–0xE86017FF	0.5K	Reserved
0xE8601400–0xE86015FF	0.5K	DSI1
0xE8601200–0xE86013FF	0.5K	Reserved
0xE8601000–0xE86011FF	0.5K	DSI0
0xE8600000–0xE8600FFF	4K	MMBUF_CFG
0xE85E0000–0xE85FFFFF	128K	Reserved
0xE85D0000–0xE85DFFFF	64K	Reserved
0xE85C0000–0xE85CFFFF	64K	Reserved
0xE85B0000–0xE85BFFFF	64K	SMMUv500_CFG
0xE8592000–0xE85AFFFF	120K	Reserved
0xE8590000–0xE8591FFF	8K	Reserved
0xE8584000–0xE858FFFF	48K	Reserved
0xE8583000–0xE8583FFF	4K	Reserved
0xE8582000–0xE8582FFF	4K	Reserved
0xE8581000–0xE8581FFF	4K	Reserved
0xE8580000–0xE8580FFF	4K	Reserved
0xE8560000–0xE857FFFF	128K	Reserved
0xE8520000–0xE855FFFF	256K	Reserved
0xE8500000–0xE851FFFF	128K	Reserved
0xE8400000–0xE84FFFFF	1M	Reserved
0xE8380000–0xE83FFFFF	512K	Reserved
0xE8360000–0xE837FFFF	128K	Reserved
0xE8340000–0xE835FFFF	128K	JPG_FD

Address	Space Capacity (byte)	Applicable Module
0xE8320000–0xE833FFFF	128K	JPG_SMMU
0xE8310000–0xE831FFFF	64K	Reserved
0xE8305000–0xE830FFFF	44K	Reserved
0xE8304000–0xE8304FFF	4K	JPG_TOP
0xE8303000–0xE8303FFF	4K	JPG_SMMU_MASTER
0xE8302000–0xE8302FFF	4K	JPG_CVDR
0xE8301000–0xE8301FFF	4K	JPG_DEC
0xE8300000–0xE8300FFF	4K	JPG_ENC
0xE82D0000–0xE82FFFFF	192K	Reserved
0xE82C0000–0xE82CFFFF	64K	G3D
0xE82BA000–0xE82BFFFF	24K	Reserved
0xE82B9000–0xE82B9FFF	4K	CODEC_SSI
0xE82B8000–0xE82B8FFF	4K	Reserved
0xE82B0000–0xE82B7FFF	32K	GIC400
0xE8200000–0xE82AFFFF	704K	Reserved
0xE8100000–0xE81FFFFF	1M	CCI_CFG
0xE808C000–0xE80FFFFF	464K	Reserved
0xE8080000–0xE808BFFF	48K	DSP_ITCM
0xE8058000–0xE807FFFF	160K	DSP_DTCM
0xE8054000–0xE8057FFF	16K	Reserved
0xE8052000–0xE8053FFF	8K	Reserved
0xE8050000–0xE8051FFF	8K	Reserved
0xE804FC00–0xE804FFFF	1K	DSD
0xE804F800–0xE804FBFF	1K	SIO_BT
0xE804F400–0xE804F7FF	1K	Reserved
0xE804F000–0xE804F3FF	1K	SIO_AUDIO
0xE804EC00–0xE804EFFF	1K	ASP_HDMI_SPDIF
0xE804E800–0xE804EBFF	1K	ASP_HDMI_SIO
0xE804E400–0xE804E7FF	1K	ASP_HDMI_ASP
0xE804E000–0xE804E3FF	1K	ASP_CFG
0xE804D000–0xE804DFFF	4K	ASP_WD

Address	Space Capacity (byte)	Applicable Module
0xE804C000–0xE804CFFF	4K	ASP_IPC
0xE804B000–0xE804BFFF	4K	ASP_DMAC
0xE804A000–0xE804AFFF	4K	ASP_TIMER1
0xE8049000–0xE8049FFF	4K	ASP_TIMER0
0xE8048000–0xE8048FFF	4K	ASP_GPIO
0xE8047000–0xE8047FFF	4K	Reserved
0xE8040000–0xE8046FFF	28K	Reserved
0xE8028000–0xE803FFFF	96K	Reserved
0xE8000000–0xE8027FFF	160K	Reserved
0xE7FC0000–0xE7FFFFFF	256K	Reserved
0xE7F80000–0xE7FBFFFF	256K	Reserved
0xE7F00000–0xE7F7FFFF	512K	USB_AUDIO
0xE4000000–0xE7EFFFFF	63M	Reserved
0xE3C00000–0xE3FFFFFF	4M	Reserved
0xE3A03000–0xE3BFFFFF	2036K	Reserved
0xE3A02000–0xE3A02FFF	4K	Reserved
0xE3A00000–0xE3A01FFF	8K	Reserved
0xE39D8000–0xE39FFFFF	160K	Reserved
0xE3940000–0xE39D7FFF	608K	Reserved
0xE38D8000–0xE393FFFF	416K	Reserved
0xE3840000–0xE38D7FFF	608K	Reserved
0xE3800000–0xE383FFFF	256K	Reserved
0xE36C0000–0xE37FFFFF	1M1.25M	Reserved
0xE3600000–0xE36BFFFF	768K	Reserved
0xE3580000–0xE35FFFFF	512K	Reserved
0xE3500000–0xE357FFFF	512K	Reserved
0xE3480000–0xE34FFFFF	512K	Reserved
0xE3400000–0xE347FFFF	512K	Reserved
0xE3200000–0xE33FFFFF	2M	Reserved
0xE3100000–0xE31FFFFF	1M	Reserved
0xE3000000–0xE30FFFFF	1M	Reserved

Address	Space Capacity (byte)	Applicable Module
0xE2400000–0xE2FFFFFF	12M	Reserved
0xE2000000–0xE23FFFFF	4M	Reserved
0xE1000000–0xE1FFFFFF	16M	Reserved
0xE0840000–0xE0FFFFFF	7936K	Reserved
0xE0800000–0xE083FFFF	256K	Reserved
0xE0780000–0xE07FFFFF	512K	Reserved
0xE0764000–0xE077FFFF	112K	Reserved
0xE0760000–0xE0763FFF	16K	Reserved
0xE0748000–0xE075FFFF	96K	Reserved
0xE0740000–0xE0747FFF	32K	Reserved
0xE0724000–0xE073FFFF	96K	Reserved
0xE0720000–0xE0723FFF	32K	Reserved
0xE0708000–0xE071FFFF	96K	Reserved
0xE0700000–0xE0707FFF	32K	Reserved
0xE0524000–0xE06FFFFF	1904K	Reserved
0xE0520000–0xE0523FFF	16K	Reserved
0xE0510000–0xE051FFFF	64K	Reserved
0xE0500000–0xE050FFFF	64K	NOC_SERVICE
0xE045C000–0xE04FFFFF	656K	Reserved
0xE0458000–0xE045BFFF	16K	Reserved
0xE0457000–0xE0457FFF	4K	Reserved
0xE0456000–0xE0456FFF	4K	Reserved
0xE0455000–0xE0455FFF	4K	Reserved
0xE0454000–0xE0454FFF	4K	Reserved
0xE0453000–0xE0453FFF	4K	Reserved
0xE0452000–0xE0452FFF	4K	Reserved
0xE0445000–0xE0451FFF	52K	Reserved
0xE0444000–0xE0444FFF	4k	Reserved
0xE0443000–0xE0443FFF	4k	Reserved
0xE0442000–0xE0442FFF	4k	Reserved
0xE0441000–0xE0441FFF	4K	Reserved

Address	Space Capacity (byte)	Applicable Module
0xE0440000–0xE0440FFF	4K	Reserved
0xE0400000–0xE043FFFF	256K	Reserved
0xE0300000–0xE03FFFFF	1024K	Reserved
0xE0224000–0xE02FFFFF	880K	Reserved
0xE0223000–0xE0223FFF	4K	Reserved
0xE0222000–0xE0222FFF	4K	Reserved
0xE0220000–0xE0221FFF	8K	Reserved
0xE0218000–0xE021FFFF	32K	Reserved
0xE0217000–0xE0217FFF	4K	Reserved
0xE0216000–0xE0216FFF	4K	Reserved
0xE0215000–0xE0215FFF	4K	Reserved
0xE0214000–0xE0214FFF	4K	Reserved
0xE0213000–0xE0213FFF	4K	Reserved
0xE0212000–0xE0212FFF	4K	Reserved
0xE0211000–0xE0211FFF	4K	Reserved
0xE0210000–0xE0210FFF	4K	Reserved
0xE020F000–0xE020FFFF	4K	Reserved
0xE020E000–0xE020EFFF	4K	Reserved
0xE020D000–0xE020DFFF	4K	Reserved
0xE020C000–0xE020CFFF	4K	Reserved
0xE020B000–0xE020BFFF	4K	Reserved
0xE020A000–0xE020AFFF	4K	Reserved
0xE0209000–0xE0209FFF	4K	Reserved
0xE0208000–0xE0208FFF	4K	Reserved
0xE0207000–0xE0207FFF	4K	Reserved
0xE0206000–0xE0206FFF	4K	Reserved
0xE0205000–0xE0205FFF	4K	Reserved
0xE0204000–0xE0204FFF	4K	Reserved
0xE0203000–0xE0203FFF	4K	Reserved
0xE0202000–0xE0202FFF	4K	Reserved
0xE0201000–0xE0201FFF	4K	Reserved

Address	Space Capacity (byte)	Applicable Module
0xE0200000–0xE0200FFF	4K	Reserved
0xE0100000–0xE01FFFFF	1M	Reserved
0xE0000000–0xE00FFFFF	1M	Reserved
0x00000000–0xDFFFFFFF	3584M	DRAM

3 Mobile Processing Module

3.1 CPU

3.1.1 Overview

The main processor is a big.LITTLE heterogeneous CPU subsystem that consists of the Cortex-A73 MP and Cortex-A53 MP processors. The Cortex-A73 MP and Cortex-A53 MP processors are based on the ARMv8-A architecture.

The Cortex-A73 MP processor has the following features:

- Processing performance of 3.66 DMIPS/MHz
- Superscaler, variable-length, and out-or-order pipeline
- Dynamic branch prediction with the branch target buffer (BTB), global history buffer (GHB), return address stack, and indirect predictor
- Fully-associative L1 instruction translation lookaside buffer (TLB) with 32 entries, supporting the page entry size of 4 KB, 16 KB, 64 KB, or 1 MB
- Fully-associative L1 data TLB with 48 entries, supporting the page entry size of 4 KB, 16 KB, 64 KB, or 1 MB
- 4-channel set-associative L2 TLB with 1024 entries
- Fixed size of 64 KB for the L1 instruction cache and 64 KB for the L1 data cache
- 2 MB L2 cache shared by the data and instruction
- ACE bus interface
- VFP and NEON units
- ARMv8-based Cryptography extended instruction
- External GIC
- Internal 64-bit universal counter for each CPU
- Independent power-off for the CPU core

The Cortex-A53 MP processor has the following features:

- Processing performance of 2.3 DMIPS/MHz
- In-order pipeline, supporting dual-instruction execution
- Direct and indirect branch prediction
- Two independent fully-associative L1 TLBs (with each having 10 entries) for instructions and data read/write, respectively.

- 2-channel set-associative L2 TLB with 256 entries
- 32 KB L1 data cache and 32 KB L1 instruction cache
- 1MB L2 cache shared by the data and instruction
- ACE bus interface
- ETM trace debugging
- CTI multi-core debugging
- Performance statistics unit with the PMUv3 architecture
- VFP and NEON units
- ARMv8-based Cryptography extended instruction
- External GIC
- Internal 64-bit universal counter for each CPU
- Independent power-off for the CPU core

The Cortex-A73 MP and Cortex-A53 MP processors use the CCI-550 to implement consistency of cache data, GIC-400 for interrupt virtualization, system counter for timer virtualization, and event interface for event interaction.

3.1.2 Operating Mode

3.1.2.1 Operating States

The Cortex-A73 MP and Cortex-A53 MP processors have the following four operating states, which are determined by the ARMv8-A architecture:

- Architecture state: AArch32 or AArch64
- Instruction set state: determined by the supported instruction set. The instruction set states include A32, T32, and A64.
- Exception level state: There are four exception level states, as described in Table 3-1.
- Security state: non-secure state or secure state

3.1.2.2 Exception Level

Table 3-1 lists the ARMv8-A exception levels.

Table 3-1 ARMv8-A exception levels

Exception Level of the Processor	Description
EL0	Execution mode of the user program, non-privileged, one mode for the Secure World and one mode for the Non-Secure World
EL1	Running mode of the operating system, privileged, one mode for the Secure World and one mode for the Non-Secure World
EL2	Mode used for virtualization extension, used only in the Non-Secure World
EL3	Mode used to switch between the Secure World and Non-Secure World

3.2 GPU

3.2.1 Overview

The GPU is used to process three-dimensional images and special effects.The key technologies include polygon conversion, illuminant processing, cubic environment material textures and vertex blending, texture compression, and bump mapping as well as rendering.

3.2.2 Operating Mode

The GPU mainly processes the 3D graphics in the SoC system. It has the following features:

- Integrated with the latest ARM Heimdall MP12 GPU and configured with two 512 KB L2 caches, effectively saving bus bandwidth. Each core integrates three arithmetic logic units (ALUs) to provide powerful floating-point computing capabilities.
- Power-off in idle hours. Each module of the GPU has a multi-level clock gating structure, which effectively reduces the GPU standby power consumption.
- Dynamic voltage frequency switch (DVFS) and AVS policies to dynamically adjust or monitor the working voltage and frequency of the GPU, effectively reducing the GPU power consumption.
- 23 texture compression formats, as shown in Table 3-2.

Table 3-2 Texture compression formats supported by the GPU

No.	Compression Format
1	AFBC
2	ETC2
3	EAC, 1 component
4	ETC2 + EAC
5	EAC, 2 components
6	NXR
7	BC1_UNORM (DXT1)
8	BC2_UNORM (DXT3)
9	BC3_UNORM (DXT5)
10	BC4_UNORM (RGTC1_UNORM)
11	BC4_SNORM (RGTC1_SNORM)
12	BC5_UNORM (RGTC2_UNORM)
13	BC5_SNORM (RGTC2_SNORM)
14	BC6H_UF16
15	BC6H_SF16
16	BC7_UNORM

No.	Compression Format
17	EAC_SNORM, 1 component
18	EAC_SNORM, 2 components
19	ETC2 + punch-through alpha
20	ASTC 3D LDR
21	ASTC 3D HDR
22	ASTC 2D LDR
23	ASTC 2D HDR

3.3 I/O Processor

The internal processor of the I/O processor (IOMCU) is Cortex-M7. It provides one AXI master interface (shared by Cortex-M7 and DMA), one AHB master interface, and two AHB slave interfaces for external communication. The processor also supports delivery of instructions through ETM trace and debug AHB interfaces for debugging.

In addition, the IOMCU has common peripheral intellectual properties (IPs), including:

- Two SPI modules
- Three UART interface modules
- One BLPWM interface module
- Four I^2C interface modules
- One DMA module
- One 32 kHz clock timer and one high frequency clock timer (FTimer)
- One watch dog
- Four groups of GPIOs
- One RTC module
- One task coprocessor TCP module

4 Media Processing

4.1 Overview

The Hi3670 integrates a powerful multimedia processing subsystem. This subsystem is used for applications such as picture capturing and processing, LCD control and display post processing, video encoding/decoding acceleration and image post processing, 2D/3D graphics acceleration, intelligent computing, and audio capturing/output processing.

4.2 VENC

4.2.1.1.1 Introduction

The Hi3670 integrates the H.264 and H.265 hardware video encoders (VENCs), which support the H.264 standard and H.265 standard, respectively.

The VENC has the following features:

- One H.264 encoder
  - Tool for the H.264 baseline profile

    I-slice and P-slice

    The 4 x 4 and 16 x 16 intra-frame division methods support the DC, V, and H prediction modes.

    The 8 x 8 and 16 x 16 inter-frame division methods are supported.

    The MB-level bit rate control is supported.

    The inter-frame prediction is supported for the 1/2 and 1/4 pixels.

    The cosine transform supports Hadamard transform.

    De-blocking is supported.
  - New tool for the H.264 baseline profile

    The context-adaptive binary arithmetic coding (CABAC) is supported.
  - New tool for the H.264 high profile

    Apart from the 4 x 4 transform, the 8 x 8 transform is also supported.

    The 8 x 8 intra-frame prediction is supported.
  - Input data formats

planar YUV 4:2:0

planar YUV 4:2:2

semi-planar YUV 4:2:0

semi-planar YVU 4:2:0

package UYVY4:2:2, VYUY4:2:2

package YUYV4:2:2, YVYU4:2:2

ARGB/BGRA8888

- ABGR/RGBA8888
- Output data formats: raw streams in the preceding formats
- Maximum resolution: 3840×2160; 2-pixel horizontal/vertical step
- Maximum frame rate: 720p@240 fps
- Maximum bit rate: 80 Mbit/s
- Frame storage format: linear
- Minimum resolution: 176x144

- One H.265 encoder
  - Tool for the H.265 main profile

    I-slice and P-slice

    The 4 x 4, 8x 8, 16 x 16, and 32 x 32 intra-frame division methods are supported. The 4 x 4, 8x 8, and 16 x 16 division methods support 35 prediction modes. The 32 x 32 division supports the DC/Planar prediction mode.

    The 8x 8, 16 x 16, 32 x 32, and 64 x 64 inter-frame division methods are supported.

    The CU-level bit rate control is supported.

    The ±512 horizontal integer search and ±144 vertical integer search are supported.

    The inter-frame prediction is supported for the 1/2 and 1/4 pixels.

    DCT4/8/16/32 and DST4 are supported.

    Merge and MergeSkip are supported.

    TMV is supported.

    De-blocking and sample adaptive offset (SAO) are supported.
  - Input data formats:

    planar YUV 4:2:0

    planar YUV 4:2:2

    semi-planar YUV 4:2:0

    semi-planar YVU 4:2:0
  - package UYVY4:2:2, VYUY4:2:2
  - package YUYV4:2:2, YVYU4:2:2

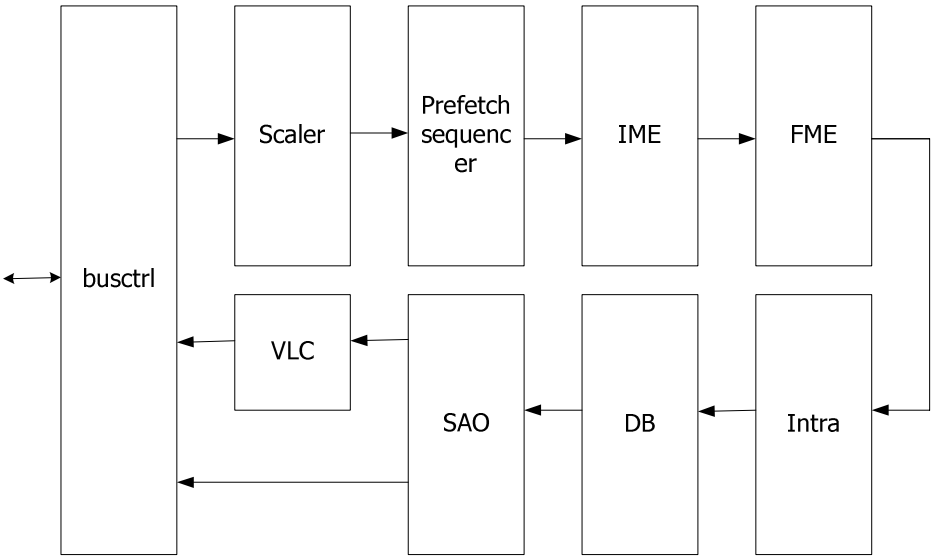
    ARGB/BGRA8888
  - ABGR/RGBA8888
  - Output data formats: raw streams in the preceding formats
  - Maximum resolution: 3840×2160; 2-pixel horizontal/vertical step
  - Maximum frame rate: 720p@240 fps
  - Maximum bit rate: 60 Mbit/s
  - Frame storage format: linear

- Minimum resolution: 176x144

4.2.1.1.2 Functional Block Diagram

Figure 4-1 shows the architecture of the VENC core. The frames to be encoded are directly read to the sequencer through the busctrl, and the subsequent encoding is started. After the encoding is complete, the frames are output to the bus through the busctrl.

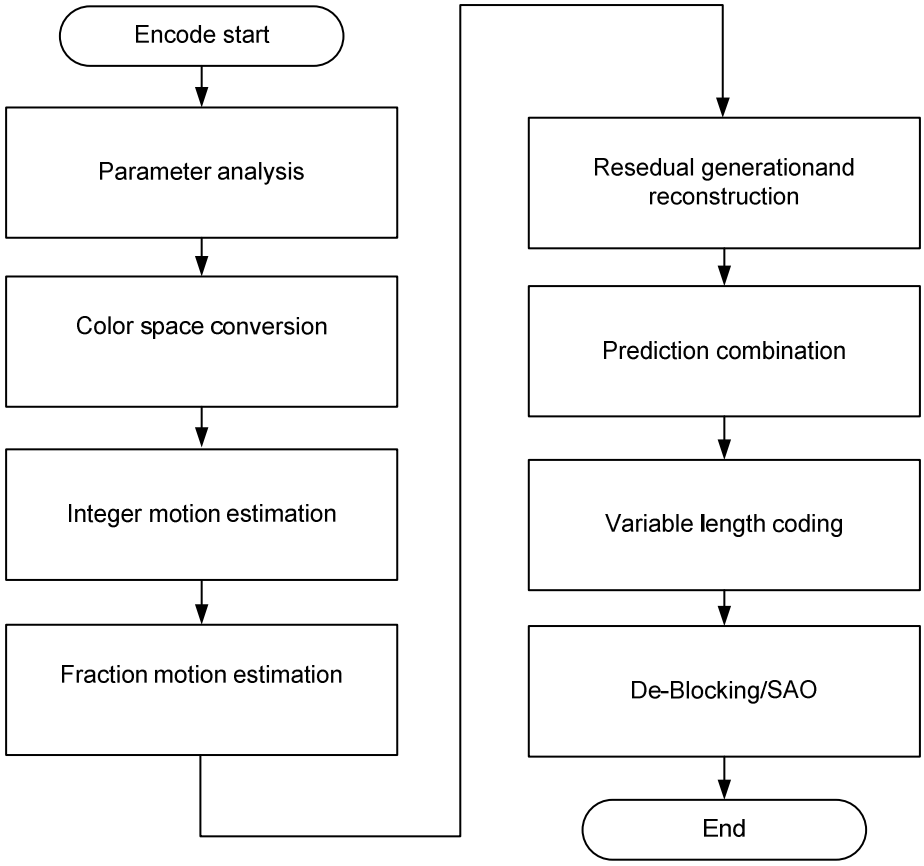
Figure 4-1 Functional architecture of the VENC core



4.2.1.1.3 Encoding Process

Figure 4-2 shows the encoding process of the VENC. After the encoding starts, the VENC performs parameter analysis and calculation. Then, it uses Colour Space Conversion to convert the color space of the input video source, searches for the integer motion vector in Integer motion estimation (IME), and then searches for the subpixel motion vector in Fraction motion estimation (FME). Finally, the reconstructed image is input to the DB/SAO, and the residual code stream input is put into the VLC for encoding.

Figure 4-2 VENC encoding workflow



4.3 VDEC

4.3.1 Function Description

4.3.1.1.1 Introduction

The Hi3670 integrates a VDEC that supports the VP9, H.265, H.264, MPEG1, MPEG2, MPEG4, VC1 (including WMV9), VP6, and VP8 protocols.

The VDEC consists of the video firmware (VFMW) running on the ARM processor and an embedded hardware video decoding engine. The VFMW obtains streams from the upper-layer software, parses the streams, and calls the video decoding engine to generate the image decoding sequences.

The sequences are under the control of the upper-layer software and output by the downstream module to a monitor or other devices. The VDEC has the following features:

- VP9 Profile2 (10 bits or less)
  - Maximum video resolution: 4K x 2K (3840 x 2160)
  - Maximum decoding rate: 100 Mbit/s or 4K x 2K@60 fps

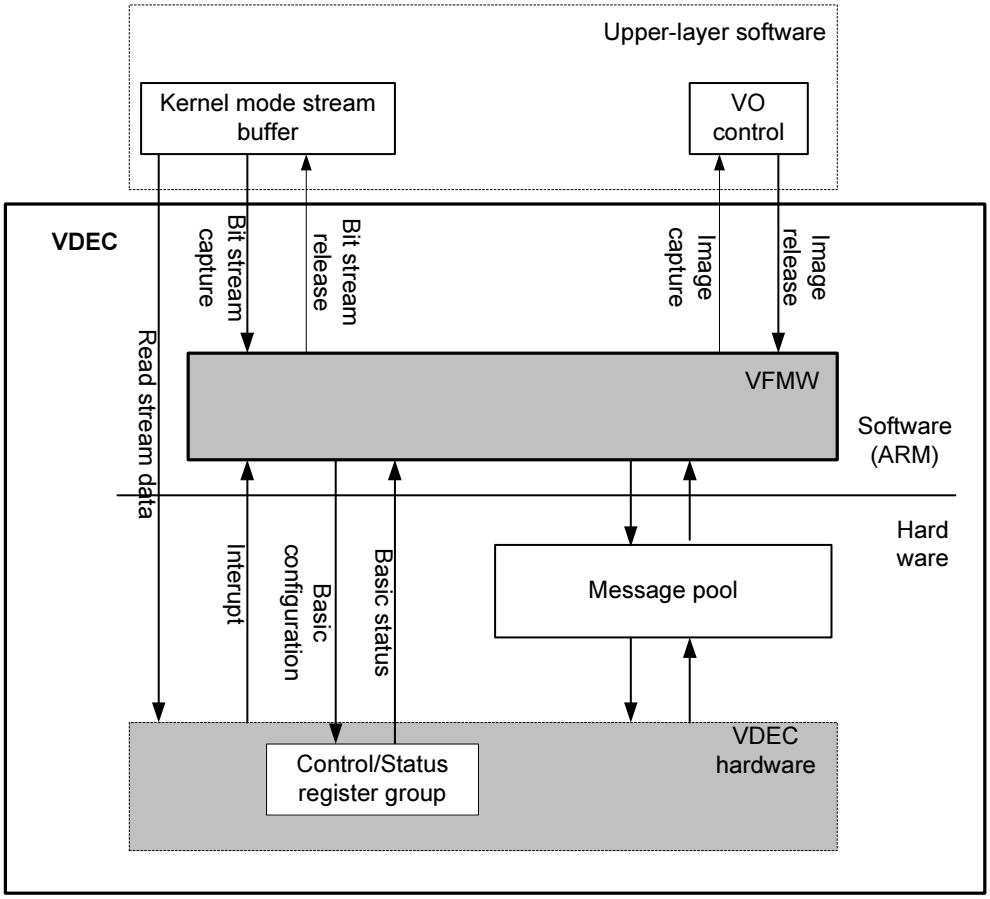
- ITU-T H.265 Main Profile 10@Level 5.1 High-tier (and lower levels)
  - Maximum video resolution: 4K x 2K (3840 x 2160)
  - Maximum decoding rate: 160 Mbit/s or 4K x 2K@60 fps
- ITU-T H.264 High Profile@Level 5.0 (and lower levels)
  - Maximum video resolution: 4K x 2K (3840 x 2160)
  - Maximum decoding rate: 135 Mbit/s or 4K x 2K@30 fps
- ISO/IEC 13818-2 (MPEG2) Main Profile@high level and backward-compatible with MP@ML, MP@LL, SP@ML, and ISO/IEC 11172-2 (MPEG1)
  - Maximum video resolution: 1080p (1920 x 1080)
  - Maximum decoding rate: 80 Mbit/s or 60 fps
- ISO/IEC 14496-2 (MPEG4) Advanced Simple Profile@L0–5, compatible with the short header format and ISO/IEC 14496-2 Simple Profile@L0–3
  - Maximum video resolution: 1080p (1920 x 1080)
  - Maximum decoding rate: 50 Mbit/s or 60 fps
- VC1 SP@ML, MP@HL, and AP@L3
  - Maximum video resolution: 1080p (1920 x 1080)
  - Maximum decoding rate: 45 Mbit/s or 60 fps
- VP6
  - Maximum video resolution: 1080p (1920 x 1080)
  - Maximum decoding rate: 50 Mbit/s or 60 fps
- VP8
  - Maximum video resolution: 1080p (1920 x 1080)
  - Maximum decoding rate: 50 Mbit/s or 60 fps
- Maximum decoding capability

  Maximum 8-bit 4K x 2K@60 fps + 1920 x 1080@30 fps

4.3.1.1.2 Functional Block Diagram

Figure 4-3 shows the VDEC architecture.

Figure 4-3 VDEC architecture



- VDEC: multi-protocol video decoding engine
- VFMW: a software component running on the master processor for scheduling the VDEC for high-definition (VDH)
- Message pool: a memory located in the external SDRAM for exchanging the messages between the VFMW and the VDEC. It can be read and written by both the VDEC and VFMW.

The VDEC and VFMW interact with each other in the following two modes:

- The VDEC and VFMW interact with each other to decode streams by slices. Specifically, the VFMW decodes the slice header and the streams before the slice header, and the VDEC decodes the slice data and the streams after the slice data.
- To support multi-channel decoding, the VFMW enables the VDEC by frames in time-division multiplexing (TDM) mode.

4.3.2 Clock and Reset

4.3.2.1.1 Clock

The VDEC supports three input clocks. For details, see Table 4-1.

Table 4-1 VDEC clock signals

Name	Description
clk_vdec	VDEC working clock, with the maximum frequency of 480 MHz
clk_axi	AXI bus clock, with the maximum frequency of 480 MHz
clk_apb	APB bus clock, with the maximum frequency of 237 MHz

4.3.2.1.2 Reset

The VDEC uses one reset signal. For details, see Table 4-2.

Table 4-2 VDEC reset signal

Name	Description
reset_vdec	Asynchronous reset signal, active low

4.4 ICS

4.4.1 Function Description

4.4.1.1.1 Introduction

The Hi3670 integrates an intelligent computing subsystem for deep learning to support all existing neural network algorithms, which include but are not limited to CNN, DNN, RNN, LSTM, MLP, SOM, and DBN. The subsystem supports various intelligent terminal processing tasks, such as image recognition, facial recognition, voice recognition, and natural language processing.

The intelligent computing subsystem has the following features:

- 256 MAC/cycle
- In the 960 MHz dominant frequency, the AlexNet network is used. The ICS module can process about 51 frames in the non-sparse mode. A sparse algorithm that does not support the batch function can process about 119 frames per second, while a sparse algorithm supporting the batch function can improve the processing capability by up to three times.
- Sparseness
- Batch function
- 1-bit weight
- The vector input and output support the following data formats:
  - 8-bit fixed-point
  - 16-bit integer (short type)
  - 16-bit floating point

  - 32-bit floating point
- Energy efficiency improvement by nearly 100 times in comparison with traditional CPUs or GPUs
- Deep learning performance 100 times higher that of traditional CPUs
- Network algorithms, including but not limited to CNN, DNN, RNN, LSTM, MLP, SOM, and DBN
- Support for highly optimized class cuDNN library programming
- Caffe for programming
- Tensorflow programming support
- Maintainability and testability
- Low-power processing
- MMU

4.4.2 Clock and Reset

4.4.2.1.1 Clock

The ICS supports three input clocks. For details, see Table 4-3.

Table 4-3 ICS clock signals

Name	Description
clk_ics	ICS core working clock, with the maximum frequency of 960 MHz
clk_axi	AXI bus clock, with the maximum frequency of 480 MHz
clk_apb	APB bus clock, with the maximum frequency of 237 MHz

4.4.2.1.2 Reset

The ICS uses three reset signals. For details, see Table 4-4.

Table 4-4 ICS reset signals

Name	Description
reset_ics_n	Asynchronous reset signal of the ICS core, active low
reset_axi_n	Asynchronous reset signal of the AXI bus, active low
reset_apb_n	Asynchronous reset signal of the APB bus, active low

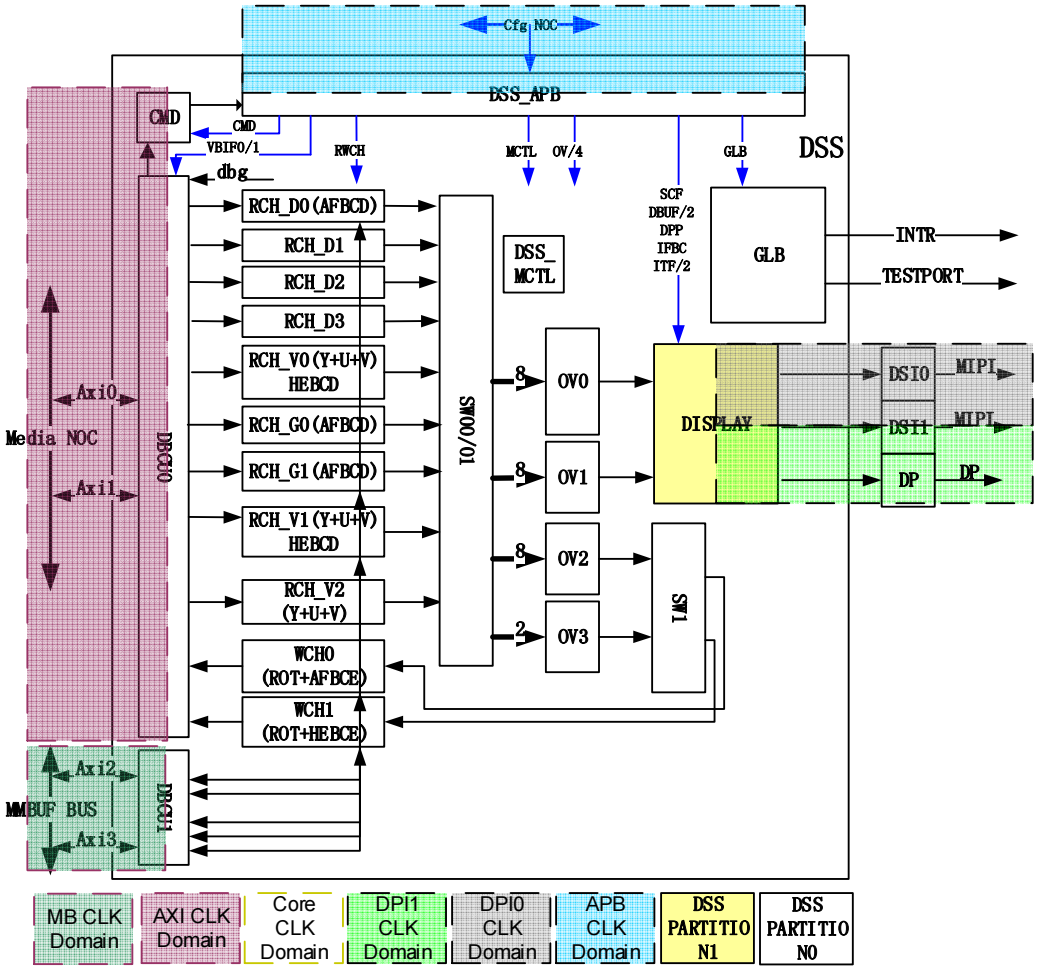
4.5 DSS

4.5.1 Function Description

The display subsystem (DSS) implements overlaying and 3D synthesis for multiple graphics layers such as the Base, Video, and Graphic, and sends the overlaid or synthesized pixels to the Display Serial Interface (DSI) or HDMI for displaying.

Figure 4-4 shows the DSS architecture.

Figure 4-4 DSS architecture



- Read channel (layer)

  The DSS has nine read channels: Three video channels (RCH_V0, RCH_V1, and RCH_V2), two graphic channels (RCH_G0 and RCH_G1), and four DMA channels (RCH_D0 to RCH_D3). Each graphics layer is read to one channel.

  - Video channel: In addition to the RGB format, the video channel can read YUV video images, and supports scaling, sharpening, and YUV2RGB conversion. The RCH_V0 channel supports deinterlacing.
  - Graphic channel: The Graphic channel reads RGB images and supports scaling.

- DMA channel: The DMA channel reads RGB images.

  The video, graphic channel, and RCH_D0 channels can directly read the RGB images compressed by the GPU, saving bus bandwidth.

- OV

  The DSS provides four OVs. OV0 is used for online composing on the primary and secondary screens and supports base+8 layer image overlay. OV1 is used for online composing only on the secondary screen and supports base+8 layer image overlay. OV2 and OV3 are used for offline composing. OV2 supports base+6 layer image overlay. OV3 supports base+8 layer image overlay. A read channel can choose to send the read images to any of the four OV for image overlay.

- Display post-processing

  After online composing, OV0 supports post-processing operations such as intelligent backlight contrast adjustment (SBL), super-resolution rendering (ARSR), adaptive color management (ACM), display device color adaptation, and adaptive contrast enhancement (ACE), cross color elimination, gamma correction, and dither.

- Primary screen display

  The primary screen supports IFBC lossy compression of images before output to save stream bandwidth and reduce power consumption. It supports single-MIPI output or dual-MIPI concurrent output. The DSI supports the MIPI protocols DSI v2.0 and DCS v1.3. The Combo-PHY supports the DPHY and CPHY modes. In DPHY mode, the DPHY protocol v1.2 is supported, the maximum PLL frequency is 2.5 GHz, and four lanes (lanes 1 to 4) can be configured. In CPHY mode, the CPHY protocol v1.0 is supported, the maximum PLL frequency is 1.5GHz, and three lanes (lanes 1 to 3) can be configured. In decompression mode, the dual-DPHY or single-CPHY can be used to output 3840x2400 @60 fps or 4096x2160 @60 fps.

- Secondary screen display

  The data to be displayed on the secondary screen can be the data on which OV0 performs display postprocessing or the data output by the OV1.

  The images composed by OV1 are sent to the secondary screen for display. The post-processing function is not supported. A maximum of 3840x2160@60 fps is supported. The data to be displayed on an external secondary screen is output by the DP or DSI1. When data is output through the secondary screen DSI1, the main screen cannot use dual MIPI output.

- Offline write back
  - The images composed by OV2 can be written back to the DDR through the write-back channel WCH0. WCH0 supports rotation.

    Application scenario:

    1. Image rotation
    2. The online overlay capability is insufficient (the number of overlay layers exceeds that supported by OV0, or the online channel resources are insufficient). The composed images can be written back to the DDR through multiple times of offline overlay. Then one DMA channel is used to send data for online display.
  - The images composed by OV2 are written back through the write-back channels WCH0 and WCH1.

    Application scenario:

    After the composed images are written back to the DDR through one channel, one DMA channel is used to read and display the images online. After the composed

images are written back to the DDR through the other channel, the images are displayed on the secondary screen in Wi-Fi display mode.

Before the overlay processing, the video graphics layer can be rotated by 90, 180, or 270 degrees, scaled, and converted from YUV to RGB. The luminance, saturation, and color temperature can be adjusted and gamma correction can be performed after overlay.

- DP

  The DP supports 3840x2160@60 fps video output, up to eight channels of audio output, software audio and video synchronization, and HDCP 1.3 and HDCP 2.2 security solutions. DPTX and HDCP+TRNG interrupts are sent to the ACPU for processing.

4.5.2 Clock and Reset

4.5.2.1.1 Clock

The DSS supports six clocks. For details, see Table 4-5.

Table 4-5 DSS clock signals

Name	Description
clk_dss_axi	AXI clock input from the peripheral CRG. The maximum frequency is 600 MHz.
pclk_dss	APB clock input from the peripheral CRG. The maximum frequency is 118.57 MHz.
clk_dss_core	Core clock input from the peripheral CRG. The maximum frequency is 553.33 MHz.
clk_dss_pxl0	Pixel 0 clock input from the peripheral CRG. The maximum frequency is 645 MHz.
clk_dss_pxl1	Pixel 1 clock input from the peripheral CRG. The maximum frequency is 594 MHz.
clk_dss_axi_mm	MMBUF clock input from the AO area. The maximum frequency is 480 MHz.

4.5.2.1.2 Reset

The DSS uses three external reset signals. For details, see Table 4-6.

Table 4-6 DSS reset signals

Name	Description
reset_dss_n	Asynchronous reset signal input by the peripheral CRG, active low
preset_dss_n	APB asynchronous reset signal input by the peripheral CRG, active low. The asynchronous reset is deasserted in the APB clock domain.

Name	Description
areset_dss_n	AXI asynchronous reset signal input by the peripheral CRG, active low. The asynchronous reset is deasserted in the AXI clock domain.

4.5.3 Application

4.5.3.1 CMDLIST Configuration

4.5.3.1.1 Video Screen

The video screen performs vertical sync by 16.66 ms. It refreshes frames regardless of whether a new task is delivered.

If a new task is delivered to the video screen, it executes the new task is executed; otherwise, it repeats existing tasks.

If the software delivers a new task, the new task must be configured within a single frame.

4.5.3.1.2 CMD Screen

A CMD screen supports both on-demand and partial frame refresh.

4.5.3.1.3 Dual Screens

There are three modes for dual screens:

- Wi-Fi display
- DSI signals converted to MHL signals; channel wired transmission
- Data on the secondary screen is displayed through the DP.

DSS dual-screen strategies:

Enable overlay for one screen and offline composing for the other one, and write data back to the buffers of the primary and secondary screens.

- Wi-Fi display:

  The primary screen uses a single channel to online display data of the primary screen buffer.

  The secondary screen uses the VENC and displays data of the secondary screen buffer through Wi-Fi.
- Wired mode:

  The primary screen uses a single channel to online display data of the primary screen buffer.

  The secondary screen uses a single channel to online display data of the secondary screen buffer.

NOTE

In Wi-Fi mode, the VENC does not support the rotation function. Therefore, the DSS needs to rotate data of the secondary screen buffer based on TV display requirements. The two scenarios are as follows:

- The source image is in landscape mode, the mobile phone screen is in portrait mode, and the TV screen is landscape mode.

- Requirements:

  The primary screen needs to be rotated.

  The secondary screen does not need to be rotated.
- Resource allocation:

  OV2 composes data offline.

  Data is written back to the buffer of the primary screen through WCH0.

  Data is written back to the buffer of the secondary screen through WCH1.
- Constraints:

  The flip register cannot be configured for the read channel (RCH) used during offline composing, and WCH0 requires rotation (ROT) configuration.

  The flip register is configured for the RCH used for online display on the primary screen.

- The source image is in portrait mode, the mobile phone screen is in landscape mode, and the TV screen is in portrait mode.
  - Requirements:

    The primary screen does not need to be rotated.

    The secondary screen needs to be rotated.
  - Resource allocation:

    OV2 composes data offline.

    Data is written back to the buffer of the primary screen through WCH0.

    Data is written back to the buffer of the secondary screen through WCH1.
  - Constraints:

    RCH used during offline composing does not require flip configuration, and WCH1 requires ROT configuration.

    The flip register is configured for the RCH used for online display of the primary screen.
- The write channel has no scaling. When data is written back, data needs to be written back based on the large size. For example, if the size of the primary screen is small, the output of a single channel must support SCF down. If the secondary screen is small, in Wi-Fi, the encoder needs to be scaled down. In wired mode, the primary screen that uses a single channel for display supports SCF down.
- When the secondary screen is connected to the DP for display, the dedicated PLL7 is selected to provide the PXL clock (media_CRG).

4.5.3.1.4 Offline

- One-time offline composing
- Multiple offline composing: The next composing requires the write-back result of the previous composing. Therefore, after the buffer is ready, that is, after data is written back through the WCH, the RCH can be started to read buffer data, and the next composing starts.

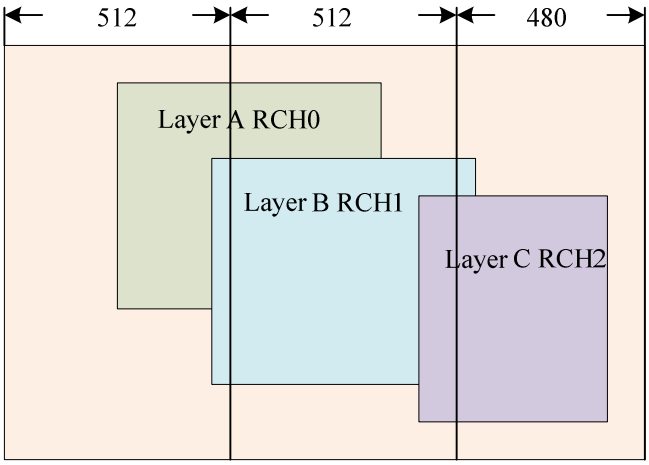
  Multiple offline composings can be regarded as the accumulation of single composing.

4.5.3.1.5 Offline Vertical Block Partition

As shown in Figure 4-5, the WCH_SCF output size is divided into vertical blocks by 512 pixels. Each time an OV block is processed offline, the RCH is started to read the layer blocks in the block. The reference coordinates of the upper left corner of each OV block are [0, 0].

When an OV block is processed, the input and output widths of the WCH_scf, WCH_post clip, rch_post_clip, arsr_pre, rch_scf, rdfc, and rdma modules need to be calculated for each layer block in the block.

Figure 4-5 Offline vertical block partition



4.5.3.1.6 Block Division Process

[Online OV block partition]

Step 1 Check whether the channel resources are sufficient for online display.

- Adjust the upper and lower boundary coordinates [Y0, Y1] of the layer. The adjusted coordinates are used only for determining whether the channel resources are sufficient. The actually displayed coordinates remain unchanged.
- Determine whether the number of overlaid layers exceeds the number of layers of the OV based on the coordinates {[X0, Y0], [X1, Y1]} of each layer. If yes, choose offline display.
- Determine whether the number of specific overlaid feature channels exceeds the number of idle feature channels based on the adjusted coordinate {Y0_adj, Y1_adj} of each layer. If yes, choose offline partition.
- If ROT or AFBCD+ scaling is performed on a graphics layer (the down scaling is greater than two times), choose offline display.

Step 2 RCH channel allocation:

In the Y direction (adjusted T coordinate), the non-overlaid layers of the same feature can be allocated to the same RCH.

Step 3 Preliminary block partition for OVs:

Excluding the base layer, OV0, OV1, and OV2 support a maximum of eight layers, and

OV3 supports a maximum of two layers.

The division principle is based on the maximum number of layers supported by OVs (OV0, OV1, and OV2 are used as an example).

- The divided blocks are added to the OV layer according to the start point Y0 of the layer. If multiple OV layers multiplex the same RCH, Y0-1 of the second multiplexing OV layer is used as the block height of the first OV block. Otherwise, Y0-1 of the ninth layer is used as the block height of the first OV block.
- Adjust the Y0 coordinate of the first OV block layer to block_height + 1 of the first OV block.
- Repeat the preceding two steps to obtain block_height of the second to the last OV block.

Step 4 Check excessively small blocks.

If the height of an OV block is less than 64 and is not the last one, choose offline display. If this OV block is the last block, choose online display. The reason is that some nodes are removed after each task is complete. Therefore, to ensure that the CMDLIST is configured, the minimum size of the last layer in offline mode must be 16x16. Regardless of the online or offline mode, the width and height of the input image of each OV layer must be greater than or equal to 4.

----End

[Offline OV block partition]

In offline mode, vertical blocks can be divided only for large images after OV overlay, and vertical blocks cannot be divided into small OV blocks.

Step 5 Pre-determine the OV layer overlay from bottom to top by the OV layer number until the number of channels or OV layers is used up (including the base layer). Then, write back the data to the frame buffer and record the number (N) of the current uppermost layer.

Step 6 Pre-determine the OV layer overlay from layer N+1 in bottom up mode until the number of channels or OV layers is used up (The frame buffer in step 1 needs to be added to layer 0). In the overlay, the data read from the frame buffer is the coordinate data of the pre-determined image in the window after overlay (excluding layer 0).

Step 7 Repeat step 2 until all layers are overlaid.

----End

4.5.3.2 Partial Refresh

4.5.3.2.1 Partial Refresh for a Non-Compressed Screen

- CMD screen configured for the CPU
- CMD screen configured for the CMDLIST

4.5.3.2.2 Partial Refresh for a Compressed Screen

- RSP 3x
  - A window to be refreshed must contain the complete 32x2 block.

- When the transmission rate is 1Gbit/s per lane, the window address (SC, EC) meets the following requirements:

Horizontal resolution	SC	EC
1600RGB	'h0 - 'h1B0	'h48F – 'h63F
1440RGB	'h0 – 'h1D0	'h3CF – 'h59F
1536RGB	'h0 – 'h200	'h3FF – 'h5FF

- Column address: 2Ah
- The value of SC must be smaller than or equal to that of EC. The SC and EC values cannot exceed the screen size. The value of SC is a multiple of 16, the value of EC is subtracting a multiple of 16 by 1, and the calculation result of (EC – SC) is a multiple of 32. After data of the previous frame is sent, wait for 15 us to send the next **Set column addr** command.
- Page address: 2Bh
- The value of SP must be less than or equal to that of EP. The SP and EP values cannot exceed the screen size. The value of SP is a multiple of two, the value of EP is subtracting a multiple of 2 by 1, and calculation result of (EP – SP) is greater than or equal to 6. After data of the previous frame is sent, wait for 15 us to send the next **Set page addr** command.
- The constraints are as follows based on whether a single MIPI or dual MIPIs are used for transmission:
- If a single MIPI is used, there is no constraints.
- If dual MIPIs are used, it is found that the driver IC divides the entire screen (frame buffer) into two parts, which use two MIPIs to implement data transmission, respectively. When an image whose refresh is controlled by set_column_addr is displayed on the left half screen, all data must be transferred through MIPI port0. Otherwise, MIPI port1 is used for transmission. When the rectangular area covers both the left and right half screens, the two MIPIs transmit data of their own half screens.
- To avoid the preceding constraints, refresh the entire line directly or refresh the image to be symmetric by the central line of the screen.

- VESA DSC 3x
  - Divide the image into panel_w*slice_h blocks based on the configured slice_h. The area to be refreshed must contain an integer number of such blocks.
  - The screen height can be divided by slice_h.
  - Slice_w*slice_h ≥ 15000

4.5.3.3 Configuration Restrictions for the DSS Blanking Region

NOTE

HSW: line sync pulse width

HBP: horizontal back porch (in pixel clock)

HFP: horizontal front porch (in pixel clock)

VSW: frame sync signal pulse width (in the number of scanned lines)

VBP: vertical back porch (in the number of scanned lines)

VFP: vertical front porch (in the number of scanned lines)

Table 4-7 describes VBP+VSW requirements for different resolutions.

Table 4-7 Configuration restrictions on the blanking and synchronization regions in typical resolutions

Resolution	VBP+VSW
1080p mobile phone (1080x1920)	67
1080p tablet (1920x1200)	55
2K mobile phone (1440x2560)	87
2K tablet (2560x1600)	84
4K mobile phone (2160x3840)	100
4K tablet (3840x2400)	94

Table 4-8 describes the restrictions on the 1080x2160 resolution of the DSS on the Hi3670 application platform.

Table 4-8 Restrictions of the DSS on the 1080x2160 resolution

Item	Unit	Min	Max
VSW+VBP	Line	63	127
VSW+VBP+VFP	Line	67	300
HSW+HBP+HFP	DSI byteclk	12	122
HTOTAL	us	6.775	7.484
FrameRate	Hz	60	-
MIPI clk	MHz	-	1000

4.5.3.3.2 Command Sending Restrictions on MIPIs

The number of accumulated headers cannot exceed 10.

The accumulated payload in the MIPI commands delivered by the APB interface does not exceed 800 bytes.

In actual application, the software must determine whether to deliver a new command based on the FIFO full status indicator in the register.

4.5.3.4 DSI AutoUlps

A DSI can be configured to automatically enter the ULPS state after it stays at the LP for a specified time (configurable). The DSI automatically exits the ULPS state when receiving an image sending request again.

The AutoUlps has the following restrictions on the MIPI clock: A higher MIPI clock frequency is preferred. The clock frequency should be greater than 860 MHz in CPHY mode and 960 MHz in DPHY mode.

4.5.4 DP (DSS)

4.5.4.1 Function Description

DisplayPort (DP) is an HD digital display interface standard defined by the video electronics standards association (VESA). DP interfaces can be connected to a computer and a monitor, aiming to replace the VGA, DVI, and LVDS interfaces and provide high-performance video transmission channels. This project supports DisplayPort 1.3.

4.5.4.2 Clock and Reset

4.5.4.2.1 Clock

The DP (DSS) supports seven clocks. For details, see Table 4-9.

Table 4-9 DP (DSS) clock signals

Name	Description
pixel_clk	Pixel clock input by the DSS; frequency: 25–594 MHz
i2s_clk	I^2S clock input by the ASP; frequency: 98.3 MHz
spdif_clk	SPDIF clock input by the ASP; frequency: 393.2 MHz
phy_clk	PHY clock input by USB/DP Combo PHY; frequency: 40.5–405 MHz
aux16mhz_clk	Aux clock input by the clock and reset generator (CRG); frequency: 16 MHz
apb_clk	APB clock input by the CRG; frequency: MMC0 bus frequency/2
axi_clk	AXI clock input by CRG; frequency: 200 MHz

4.5.4.2.2 Reset

The defect pixel correction (DPC) module inputs one reset signal vcc_rst_n and synchronizes the signal to each internal clock domain.

4.5.4.3 Application

4.5.4.3.1 Video

DP supports output of 4K 60 fps videos. As an external interface, the defect pixel correction (DPC) module receives video data processed by the DSS, converts the video data into a packet format specified by DP, and outputs the data to the peer monitor. As an interface module, the DPC does not process video data. Instead, it converts only the data format to adapt to the DP protocol.

4.5.4.3.2 Audio

DP supports a maximum of 8-channel audio data. It connects to the AUDIO module through a single-bit I^2S interface or 4-bit SPDIF interface.

According to the DP protocol, audio data is transmitted in a blanking region in secondary data packet (SDP) mode after each video data frame is transmitted.

4.5.4.3.3 AV Synchronization

The audio and video (AV) solution is a software solution. The software obtains the delay information from sink device's DisplayPort configuration data (DPCD) through an aux channel and then compensates the delay accordingly.

4.5.4.3.4 PHY

- Type-C PHY

  According to the DP protocol, the DPC and USB 3.0 can share the same Type-C PHY. The DPC connects to the PHY through the DP 4-lane main link interface.
- AUX PHY

  DP needs to work together with the AUX PHY to read information about the peer device and configure the peer device. The AUX PHY is a group of differential pair outputs. It uses the SBU1 and SBU2 pins of Type-C PHY. The AUX PHY is mainly used for information configuration. Therefore, it requires low bandwidth. According to the protocol, the operating frequency of the AUX PHY is 1 MHz.

4.5.4.3.5 Interrupt

The DPC outputs two interrupt signals. One is the DPTX interrupt and the other is the HDCP+TRNG interrupt. Both interrupts are sent to the ACPU for processing.

4.6 ASP

CAUTION

The description in this section applies only to the audio signal processor (ASP).

4.6.1 DSP

4.6.1.1 Function Description

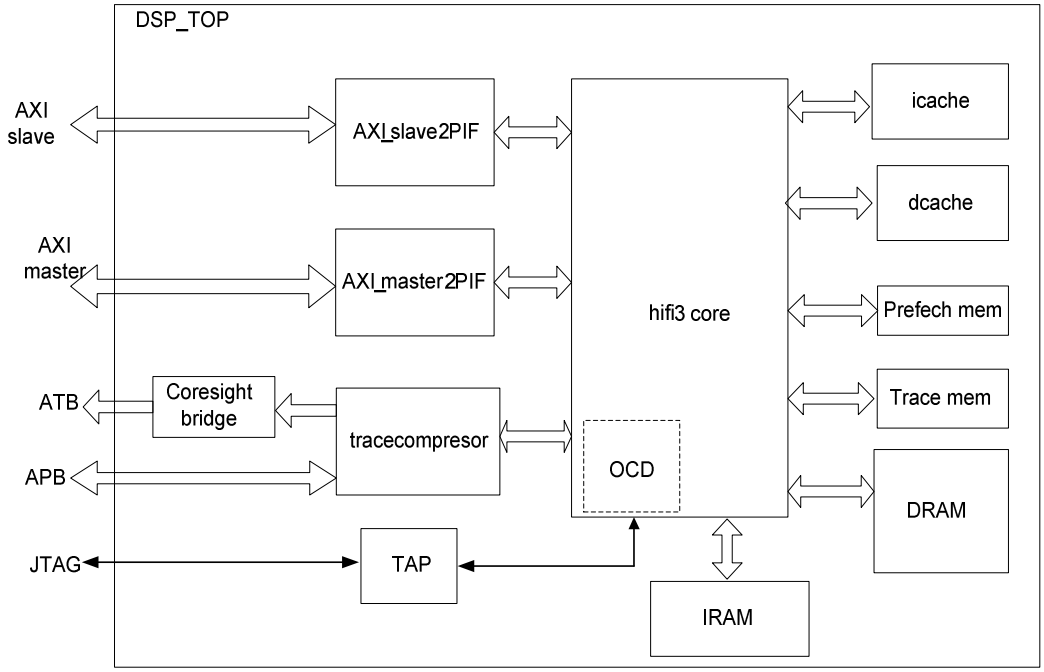
The digital signal processor (DSP) functions are described as follows:

- The audio DSP uses the Tensilica Hi-Fi 3.0 processor, and implements HD video sound decoding (such as DTS) and post-processing as well as common audio decoding (such as MP3) of the dedicated player.
- Cache organization mode: 4-way set associative cache
- Bus interface: one 64-bit AXI master interface for reading external data and instructions and one 64-bit AXI slave interface. The external processor can access the IRAM and DRAM of the DSP through the AXI slave interface.
- Trace interface: Two types of debug interfaces, coresight and JTAG, are supported.

- Operation unit: The MUL and MAC operations are supported, but the division operation is not supported.

Figure 4-6 shows the DSP architecture.

Figure 4-6 DSP structure



Some modules in the figure are described as follows:

- The DSP reads external data or instructions through the AXI master interface.
- The AXI slave interface can be used to access the IRAM and DRAM of the DSP.
- The JTAG interface can be used to debug the processor online.

4.6.1.2 Clock and Reset

4.6.1.2.1 Clock

The DSP module supports four clock signals, as shown in Table 4-10.

Table 4-10 DSP clock signals

Name	Description
dsp_clk	DSP core clock signal. The maximum frequency is 553 MHz.
JTCK	JTAG interface clock. The maximum frequency is 30 MHz.

4.6.1.2.2 Reset

The DSP module uses five reset signals. For details, see Table 4-11.

Table 4-11 DSP reset signals

Name	Description
BReset	DSP core reset signal
JTRST	JTAG interface reset signal
DebugReset	Debug reset signal, which is used to reset the debug logic.

4.6.1.3 Application

CAUTION

- When loading programs to the TCM in the DSP, pay attention to the following restrictions:
- The instruction tightly-coupled memory ITCM supports only 32-bit or 64-bit data access modes. When the data width is 32 bits, the start address must be word-aligned. When the data width is 64 bits, the start address must be aligned by double word. The DTCM supports 8-bit, 16-bit, 32-bit, and 64-bit data access modes.

The DSP has 32 interrupts, as shown in Table 4-12.

Table 4-12 DSP-supported interrupts

Interrupt ID	Interrupt Name	Interrupt Description	Interrupt Type/Priority	Corresponding Bit
0	NMI	Non-maskable interrupt, which is generated CFG R_DSP_NMI bit[15: 0] by bitwise or.	NMI/6	0
/	Debug	Interrupt that is not occupied by the debug function	Debug/5	/
1	Software interrupt	Interrupt triggered by HiFi internal software configuration	Software/3	/
2	AP IPC0	Inter-core interrupt 0 from the non-secure IPC to the DSP	Extlevel/3	1
3	AP IPC1	Inter-core interrupt 1 from the non-secure IPC to the DSP	Extlevel/3	2

Interrupt ID	Interrupt Name	Interrupt Description	Interrupt Type/Priority	Corresponding Bit
4	AP IPC2	Inter-core interrupt 2 from the secure IPC to the DSP	Extlevel/3	3
5	HiFi Timer0	HiFi internal timer 0 interrupt	timer/3	/
6	HiFi Timer1	HiFi internal timer 1 interrupt	timer/4	/
7	AP IPC3	Inter-core interrupt 3 from the secure IPC to the DSP	Extlevel/3	4
8	Audio Timer0_0	Timer 0_0 interrupt of the audio subsystem	Extlevel/2	5
9	Audio Timer0_1	Timer 0_1 interrupt of the audio subsystem	Extlevel/2	6
10	Audio Timer1_0	Timer 1_0 interrupt of the audio subsystem	Extlevel/2	7
11	Audio Timer1_1	Timer 1_1 interrupt of the audio subsystem	Extlevel/2	8
12	hisee2hifi_fast0/hisee2hifi_fast1/hisee2hfii_comm	Combined interrupt from the HiSEE security subsystem to the HiFi	Extlevel/1	9
13	intr_dsd	Interrupt generated by the DSD for the HiFi	Extlevel/1	10
14	intr_dfc2hifi_intr	Security interrupt from the DFC module to the HiFi	Extlevel/1	11
15	usb_audio_intr/usb_ctrl_intr	Combined interrupt of usb_audio and usb_ctrl	Extlevel/1	12
16	asp_hdmi	Combined interrupt of asp_hdmi secure and non-secure interrupts	Extlevel/1	13
17	Audio DMAC_S	Combined secure interrupt of the audio DMAC	Extlevel/1	14
18	Audio DMAC_NS	Non-secure combined interrupt of the audio DMAC	Extlevel/1	15

Interrupt ID	Interrupt Name	Interrupt Description	Interrupt Type/Priority	Corresponding Bit
19	profiling	HiFi internal performance monitoring interrupt	Extlevel/1	/
20	ldrx2hifi_time_int /l2drx2hifi_time_int	Time interrupt from the modem LDRX to the HiFi DSP	Extlevel/1	16
21	addr_moni_intr	Memory monitoring module interrupt	Extlevel/1	17
22	Audio Watchdog	Watchdog combined interrupt	Extlevel/1	18
23	Audio IPC	IPC interrupt of the audio subsystem	Extlevel/1	19
24	Slimbus	SLIMbus combined interrupt	Extlevel/1	20
25	mcpu_hifi_intr_ns/ipcm2hifi_intr0_s	IPC interrupt 0 from the modem to the HiFi	Extlevel/1	21
26	bbe16_hifi_intr_ns/ipcm2hifi_intr1_s	IPC interrupt 1 from the modem to the HiFi	Extlevel/1	22
27	I2C/ Ao_ipc_fast_intr_s	I^2C interrupt/Mailbox secure interrupt from the AO IPC_S to HiFi (The AO IPC interrupt ID is 7)	Extlevel/1	23
28	GPIO/ Ao_ipc_comm_intr_s	GPIO interrupt/Common secure interrupt from the AO IPC_S to HiFi (The AO IPC interrupt ID is 3)	Extlevel/1	24
29	HiFi internal WriteErr	HiFi internal WriteErr interrupt	WriteErr/3	/
30	tds_hifi_int	Subframe interrupt of the TDS timing module	Extlevel/1	25

Interrupt ID	Interrupt Name	Interrupt Description	Interrupt Type/Priority	Corresponding Bit
31	Intr_freq_offset/intr_ics_cnn_ns	Interrupt of the frequency offset recording module/Combined interrupt from the CNN module to the HiFi	Extlevel/1	26

4.6.2 DMAC

4.6.2.1 Function Description

4.6.2.1.1 Peripheral Requests

The direct memory access controller (DMAC) supports the transfer handshake mechanism. By using the handshake interface, peripherals notify the DMAC that the AXI bus is ready to transmit or receive data.

Table 4-13 shows the peripheral requests of the DMAC.

Table 4-13 Audio DMA peripheral requests

Peripheral ID	Specific Peripheral
0	SLIMbus0
1	SLIMbus1
2	SLIMbus2
3	SLIMbus3
4	SLIMbus4
5	SLIMbus5
6	SLIMbus6
7	SLIMbus7
8	SLIMbus8
9	SLIMbus9
10	SLIMbus10
11	SLIMbus11
12	SLIMbus12
13	SLIMbus13
14	SLIMbus14

Peripheral ID	Specific Peripheral
15	SLIMbus15
16	dsd_chr_dma_req
17	dsd_chl_dma_req
18	SIO_BT_RX
19	SIO_BT_TX
20	SIO_CODEC_RX
21	SIO_CODEC_TX
22	SIO_AUDIO_RX
23	SIO_AUDIO_TX

4.6.2.1.2 Interrupt Processing

The DMAC supports integration two sets of interrupts. One set is reported to the generic interrupt controller (GIC). The other set is reported to the digital signal processor (DSP). For details, see Table 4-14.

Table 4-14 Information of DMA interrupts

DMA Interrupt Signal Name	Interrupt ID	Target Processor
dma_intr[0]	247/189	GIC(A15/A7)/LP_M3
dma_intr_ns[0]	248/189	GIC(A15/A7)/LP_M3
dma_intr[1]	17	DSP
dma_intr_ns[1]	18	DSP

NOTE
The ID of the same interrupt varies according to different processors.

4.6.2.1.3 Clock and Reset

4.6.2.1.4 Clock

The DMA supports one clock. For details, see Table 4-15.

Table 4-15 DMAC clock signals

Name	Description
aclk0	AXI bus clock ACLK after aclk0_clken gating, with frequency of 276 MHz

Name	Description
aclk1	AXI bus clock ACLK after aclk1_clken gating, with frequency of 276 MHz
aclk0_clken	ACLK 0 clock gating signal, used to connect to the EN end of the standard gating cell
aclk1_clken	ACLK 1 clock gating signal, used to connect to the EN end of the standard gating cell
pclk_en	Rising edge indicator signal of the master clock on the APB bus and ACLK clock domain signal, lasting only one ACLK clock cycle. Because PCLK and ACLK have the same frequency, they are always connected to 1.

4.6.2.1.5 Reset

The VDEC uses one reset signal. For details, see Table 4-16.

Table 4-16 DMAC reset signal

Name	Description
areset_n	DMAC AXI bus reset signal, active low. This signal is used to reset the DMAC.

4.6.3 SIO

4.6.3.1 Function Description

4.6.3.1.1 Introduction

The Sonic Input/Output (SIO) interface connects to the off-chip audio codec to play and record music (voice). The SIO transfers the digital data that complies with the I^2S or PCM protocol. The ASP integrates three SIOs: SIO1, SIO2, and SIO3. SIO1 is SIO_AUDIO, which plays and records music, and supports the input and output in the I^2S and PCM formats. SIO2 is SIO_BT, which is used to connect to the external SmartPA. SIO3 is SIO_CODEC, which is used to connect to the third-party codec.

- The SIO module supports the master and slave modes as well as playing transmit (TX) and recording receive (RX).
- The SIO module supports the I^2S and PCM interface timings. The interface signal lines in two modes are multiplexed.
- The SIO module supports only the inputs of clock and synchronization signals. In I^2S master mode, the SIO module needs to work with the CRG module that sends the clock and synchronization signals to the outside.

The SIO module in I^2S mode has the following features:

- The I^2S interface supports the 16-bit, 18-bit, 20-bit, 24-bit, and32-bit transfer modes.

- The 8–192 ksps sampling rate is supported.
- The extended module supports 2-/4-/8-/16-channel RX and 8-/16-bit transfer mode.
- The I^2S RX and TX channels have independent FIFOs. The audio-left and audio-right channels each has an independent FIFO. The FIFO depth is 16 and the width is 32 bits.
- The I^2S interface supports the function of disabling the FIFO. When a FIFO is disabled, the RX and TX data is stored in a buffer rather than the FIFO.
- The I^2S interface allows the TX and RX channels to be separately enabled. If a channel is disabled, the control unit and data storage unit of this channel are not reversed. In this way, power consumption is saved.
- For the I^2S interface in 16-bit transfer mode, the RX and TX data of the audio-left and audio-right channels can be combined into one 32-bit data segment and then stored or written into the RX/TX FIFO. In this way, the buffering capacity of the FIFO is improved. The extended module does not support this combination function.
- The RX channel supports upper-bit sign extension.
- The TX and RX audio channel selection signals can be the same, facilitating connection with the 4-wire codec.

The SIO module in PCM mode has the following features:

- The 8-bit and 16-bit transfer modes are supported.
- The extended module supports 2-/4-/8-/16-channel RX and 8-/16-bit transfer mode.
- Only the short frame synchronization mode is supported. Both the standard and customized timing modes are supported.
- The RX and TX channels have independent FIFOs. The FIFO depth is 16 and the width is 32 bits.
- The FIFO can be disabled. When a FIFO is disabled, the RX and TX data is stored in a buffer rather than the FIFO.
- The TX and RX channels can be separately enabled. If a channel is disabled, the control unit and data storage unit of this channel are not reversed. In this way, power consumption is saved.
- The RX channel supports upper-bit sign extension.

The SIO module also provides the CPU/DSP access interface, which has the following features:

- The CPU/DSP can access the SIO using the advanced high-performance bus (AHB) Slave (AMBA 2.0) interface provided by the SIO module.
- The SIO AHB interface supports only 32-bit operations.
- The SIO AHB interface supports only the OK response, and does not support the ERROR, Retry, and Split responses.
- The SIO AHB interface supports various burst operations.
- The SIO supports direct memory access (DMA) operations in burst mode.
- The SIO allows the audio-left and audio-right channels to use the same TX address to transmit data and the same RX address to receive data.

NOTE

- The master and slave modes of the SIO module differ in the sources of the clock (BCLK) and sampling rate (ADWS). In master mode, the AP side of Hi3660 generates the clock and sampling rate. In slave mode, the AUDIO_CODEC side generates the clock and sampling rate. The master and slave modes are not related to the TX and RX.
- If the data width is 24 bits or 32 bits in PCM mode, only the upper-16-bit data is transferred because the maximum bit width of the SIO is 16.

4.6.3.1.2 Interface Timing

Figures 6-7 to 6-9 show the I^2S interface timings.

Figure 4-7 I^2S interface timing

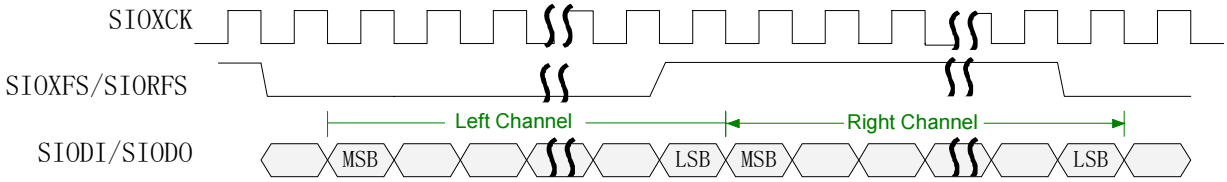


Figure 4-8 PCM timing in standard mode

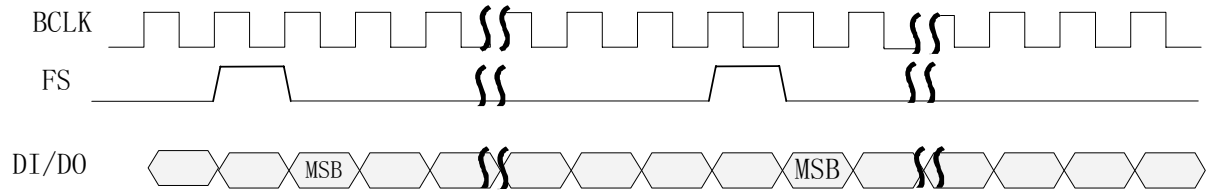
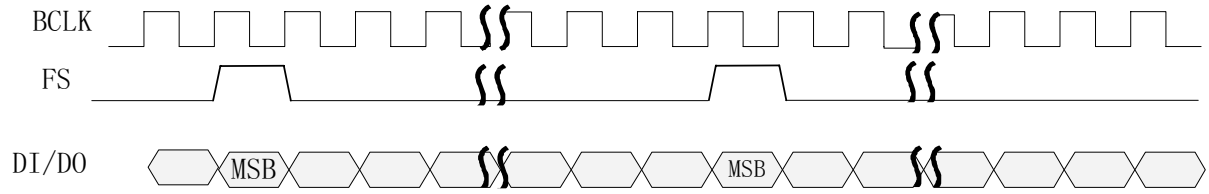


Figure 4-9 PCM timing in custom mode



4.6.3.2 Clock and Reset

4.6.3.2.1 Clock

The SIO clock source varies according to the master mode and slave mode.

The SIO supports one bus clock and two interface data clocks, as shown in Table 4-17.

Table 4-17 SIO clock signals

Name	Description
hclk	AHB bus clock signal. The frequency is 276 MHz or 9.6 MHz.
bclk_adc	This signal is used for I^2S/PCM data transfer when the SIO interface is used for communication.
bclk_dac	Not used
txws_adc	Frame sync signal during TX playback, which is used for I^2S/PCM data sampling
rxws_adc	Frame sync signal during RX recording, which is used for I^2S/PCM data sampling

The clock and sampling rate of four SIO interfaces used by the Hi3670 are different. For details, see Table 4-18.

Table 4-18 SIO clock frequency and sampling rate

Interface Type	Description	Clock	Sampling Rate
I^2S interface	Note that the clock is 64 times of the corresponding sampling rate, which is required by the I2S protocol.	12.288 MHz	0.192 MHz
		6.14 MHz	0.096 MHz
		3.072 MHz	0.048 MHz
		2.048 MHz	0.032 MHz
		1.024 MHz	0.016 MHz
		0.512 MHz	0.008 MHz
PCM interface	Note that the data width of the corresponding SIO interface is 16 bits. The ratio of the PCM clock to the sampling rate is the same as that of the PCM clock to the data width. 2.048 MHz is an exception, which is a special use. The IP core also supports the SIO interface.	2.048 MHz	0.008 MHz
		0.512 MHz	0.032 MHz
		0.256 MHz	0.016 MHz
		0.128 MHz	0.008 MHz

4.6.3.2.2 Reset

An SIO interface uses one reset signal, as shown in Table 4-19.

Table 4-19 SIO reset signal

Name	Description
hreset_n	AHB bus reset signal, active low

4.6.3.3 Signal Description

The following uses SIO1 as an example. Figure 4-10 and Figure 4-11 show the signal connections.

Figure 4-10 Signal connections of the SIO in master mode

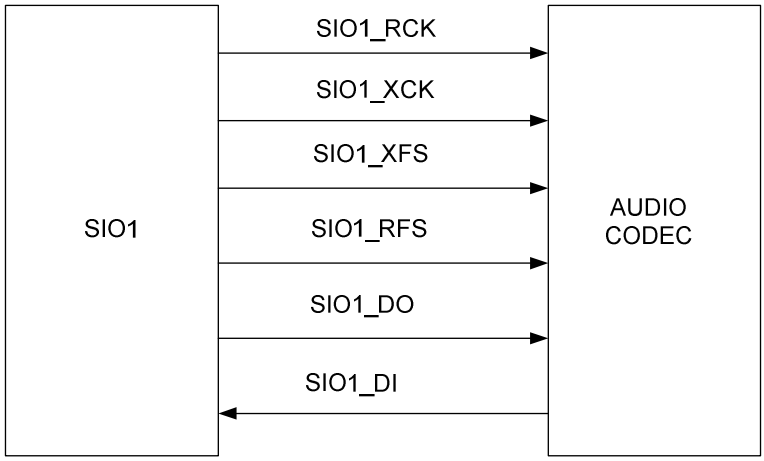
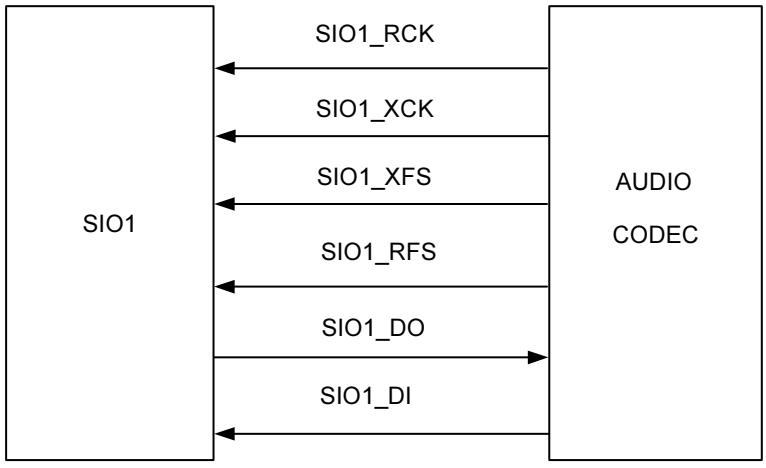


Figure 4-11 Signal connections of the SIO in slave mode



4.6.3.4 Application

4.6.3.4.1 Clock Configuration

The three SIO interfaces are independent of each other. The clock configuration modes are the same.

4.6.3.4.2 Soft Reset and Deassertion

The reset configuration modes of the three SIO interfaces are the same. They all use asynchronous reset and synchronous reset deassertion.

4.6.4 WatchDog

CAUTION

The watchdog must be disabled before the ASP enters the sleep mode.

4.6.4.1 Clock and Reset

4.6.4.1.1 Clock

Table 4-20 describes the three clocks supported by the ASP_WATCHDOG.

Table 4-20 Clock signals supported by the ASP_WATCHDOG

Name	Description
PCLK	Bus clock signal. The default value is 9.6 MHz.
WDOGCLK	Watchdog working clock signal. The default value is 9.6 MHz.
WDOGCLKEN	Watchdog timer clock signal. The default value is 32.768 kHz.

4.6.4.1.2 Reset

The reset signal of ASP_WATCHDOG is PRESETn. The watchdog uses one reset signal. For details, see Table 4-21.

Table 4-21 Watchdog reset signal

Name	Description
PRESETn	Bus reset signal. The reset is valid in the following three cases: 3. The entire chip is reset. 4. The ASP subsystem is reset. 5. The soft reset of the ASP watchdog is valid.

4.6.4.2 Application

4.6.4.2.1 Configuring the Timer Clock Frequency

The ASP supports two types of watchdog timer clocks: sleep clock (32.768 kHz) and bus clock.

The timer time of the watchdog is calculated as follows:

$T_{WDG} = Value_{WdogLoad} \times (1/f_{clk})$

$\mathbf{T_{WDG}}$ indicates the watchdog count time. $\mathbf{Value_{WdogLoad}}$ indicates the initial timer value of the watchdog. $\mathbf{f_{clk}}$ indicates the watchdog timer clock frequency.

The ranges of the count time of the watchdog under different clocks are as follows:

- When a 32.768 kHz sleep clock is used, the count time ranges from 0s to 131071s.
- When a 9.6 MHz bus clock is used, the count time ranges from 0s to 447.392s.
- When a 276 MHz bus clock is used, the count time ranges from 0s to 23.86s.

4.6.4.2.2 Watchdog Initialization

The watchdog timer stops after the power-on reset of the ASP. During ASP initialization, the watchdogs must be initialized and started.

4.6.4.2.3 Initial Value of the Watchdog Timer

The watchdog monitors the running status of the system. In normal cases, the system sets an initial timer value periodically.

If the initial timer value is not specified timely, the software is running abnormally. When the timer reaches 0, the watchdog sends an abnormal interrupt.

4.6.4.2.4 Watchdog Disabling

The watchdog must be disabled before the ASP enters the sleep mode.

4.6.5 GPIO

4.6.5.1 Function Description

The ASP has one GPOP module and provides five programmable GPIO pins that correspond to the low-level five pins of the eight pins of the GPIO. The GPIO pins are used to generate output signals or collect input signals for specific applications. The three upper bits are reserved. Therefore, five GPIO pins are actually used.

The GPIO has the following features:

- Each GPIO pin can be configured as an input or output.

  When serving as an input pin, a GPIO pin can be used as an interrupt source and supports independent interrupt control.

  When serving as an output pin, a GPIO pin can be independently set to 0 or 1.
- The statuses of initial and masked interrupts can be queried.
- The interrupt wakeup system is supported. The GPIO enable interrupt needs to be configured before the system enters the sleep state. After the system enters the sleep state,

the GPIO will generate an interrupt to wake up the system when peripheral inputs change.

- Five pins do not support independent soft reset.

4.6.5.2 Clock and Reset

4.6.5.2.1 Clock

The GPIO supports one clock. For details, see Table 4-22.

Table 4-22 GPIO clock signal

Name	Description
PCLK	Bus clock signal. The default value is 9.6 MHz.

4.6.5.2.2 Reset

The GPIO module uses the full-sync circuit of a single clock. When the reset signal is valid, the GPIO module performs the following operations:

- Clear the corresponding bit in the GPIOIE register to invalidate the interrupt.
- Clear all registers.
- Configures all pins as input pins.
- Set the interrupt triggering mode to edge-triggered.

The GPIO module supports global reset and independent reset of software configuration. The GPIO uses one reset signal, as shown in Table 4-23.

Table 4-23 GPIO reset signal

Name	Description
PRESETn	Bus reset signal. The reset is valid in the following three cases: 6. The entire chip is reset. 7. The ASP subsystem is reset. 8. The soft reset of the ASP GPIO is valid.

4.6.6 Timer

4.6.6.1 Clock and Reset

4.6.6.1.1 Clock

Timer 0 and timer 1 each support three clocks. For details, see Table 4-24.

Table 4-24 Timer clock signals

Name	Description
PCLK	Bus clock signal. The default value is 9.6 MHz.
TIMCLK	Working clock signal. The default value is 9.6 MHz.
TIMCLKEN1 and TIMCLKEN2	Clock enable signal. For example, for Timer0-1: • If the value is set to 1, the enable signal is 4.8 MHz. • If the value is set to 1,, the enable signal is the sync pulse of the 32.768 kHz clock in the TIMCLK clock domain.

4.6.6.1.2 Reset

A timer module supports global reset and independent reset of software configuration. It uses one reset signal, as shown in Table 4-25.

Table 4-25 Timer reset signal

Name	Description
PRESETn	Bus reset signal. The reset is valid in the following three cases: 9. The entire chip is reset. 10. The ASP subsystem is reset. 11. The soft reset of the ASP timer is valid.

4.6.7 IPC

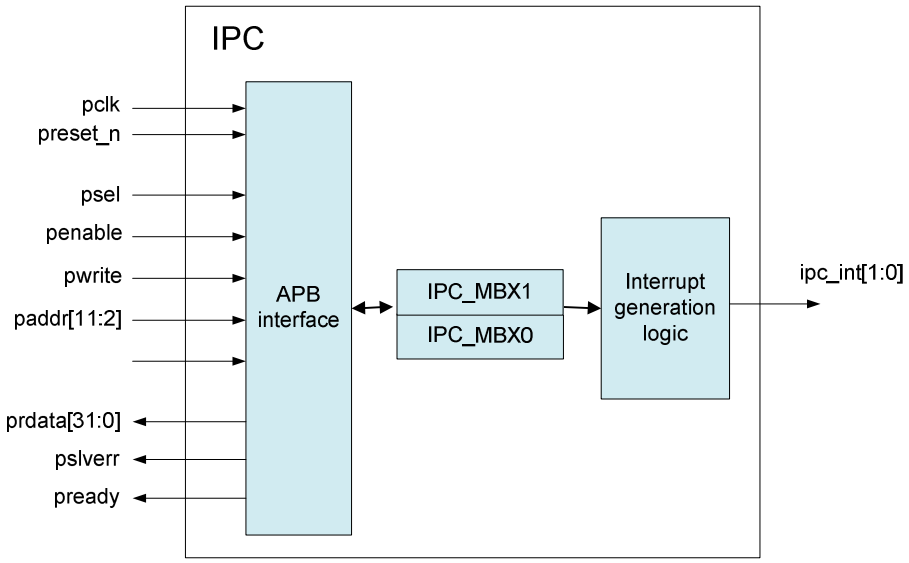
4.6.7.1 Function Description

Figure 6-17 shows the structure of the IPC module.

CAUTION

ipc_int in Figure 6-17 is a common interrupt.

Figure 4-12 IPC structure



The ASP IPC module has the following features:

- Two mailboxes are used for inter-core communication. Mailbox 0 and mailbox 1 are common mailboxes.
- Each mailbox contains two 32-bit data registers.
- Two common interrupts are supported.
- Te auto-link and auto-acknowledge modes are supported.
- Registers can be locked to prevent them from being modified incorrectly.

4.6.7.2 Clock and Reset

4.6.7.2.1 Clock

The IPC module supports one clock. For details, see Table 4-26.

Table 4-26 IPC clock signal

Name	Description
PCLK	Bus clock signal. The default value is 9.6 MHz.

4.6.7.2.2 Reset

The IPC supports one reset signal. For details, see Table 4-27.

Table 4-27 IPC reset signal

Name	Description
preset_n	Bus reset signal. The reset is valid in the following three cases: 12. The entire chip is reset. 13. The ASP subsystem is reset. 14. The soft reset of the ASP IPC_NS is valid.

4.6.8 OCRAM

4.6.8.1 Function Description

OCRAM is an internal SRAM of the ASP. Currently, there are three OCRAMs, whose sizes are 256 KB, 256 KB, and 160 KB, respectively. The total size is 672 KB. OCRAM 1 or USB audio OCRAM 2 is composed of four 64 KB SRAMs that can be powered off by block. OCRAM 3 consists of two 64 KB SRAMs and one 32 KB SRAM. The three SRAM can also be powered off by block. This provides storage space for secure operations and data and instruction storage space for the DSP. USB Audio OCRAM 2 is used by the USB audio driver, and the 128 KB space in the OCRAM is shared by the security OS.

In scenarios such as low power consumption MP3 playback, audio applications can exclusively occupy an OCRAM.

The three OCRAMs support secure access control for the memory.

In the case of low power consumption, the memory of an unused SRAM can be independently powered off through software configuration based on the application requirements.

In addition, OCRAMs support the memory repair function.

4.6.8.2 Clock and Reset

4.6.8.2.1 Clock

An OCRAM supports one clock, which uses the same frequency as the ASP interconnect bus and can be controlled independently.

4.6.8.2.2 Reset

An OCRAM supports one reset signal.

4.6.9 DP (ASP)

4.6.9.1 Function Description

DisplayPort (DP) is an HD digital display interface standard defined by the VESA. DP interfaces can be used to connect to computers and monitors, aiming to replace the VGA, DVI, and LVDS and provide high-performance video transmission channels. This project supports DisplayPort 1.3.

According to the protocol and DPTX input interface description, DP audio specifications are as follows:

- A maximum of 192 kHz sampling rate in LPCM format and 24-bit data bit width

- At most eight channels
- 768 kHz sampling rate in HBR mode
- I^2S and SPDIF interfaces
- The I^2S interface is a 4-wire interface and supports one I^2S associated clock.
- The SPDIF interface is a 4-wire interface and supports one SPDIF associated clock.
- Audio channel delay information can be read through registers.

The DP (ASP) is mainly used to connect to the DPTX, which re-assembles the audio and video data for playback.

4.6.9.2 Clock and Reset

4.6.9.2.1 Clock

The DP (ASP) supports three clocks. For details, see Table 4-28.

Table 4-28 DP (ASP) clock signals

Name	Description
asp_hclk	Configuration interface and data interface of the HDMI module. The frequency is 276 MHz, which is the same as the bus clock.
asp_hdmi_ref_clk	Working clock of the SIO module of the HDMI module. The frequency is 98.304 MHz.
asp_spdif_clk	Working clock of the SPDIF module of the HDMI. The frequency is 393.216 MHz.

4.6.9.2.2 Reset

Table 4-29 describes the reset signals of the DP (ASP) module.

Table 4-29 DP (ASP) reset signals

Name	Description
asp_hresetn	Reset signal of the configuration interface and data interface of ASP_HDMI
asp_hdmi_rstn	Reset signal of the SIO module of ASP_HDMI, which is synchronous with asp_hdmi_ref_clk
asp_spdif_rstn	Reset signal of the SPDIF module of ASP_HDMI, which is synchronous with asp_spdif_clk

5 Storage Control

5.1 Overview

The Hi3670 provides the following storage control modules:

- Universal Flash Storage (UFS) controller

  An UFS controller connects to UFS components and supports protocol versions of UFS 2.1, Unipro 1.6, and M-PHY 3.1. It supports 2-lane TX+RX channels and TX+RX channels and PWM G1–G4 and high speed (HS) G1–G3 rate A/B modes. It supports booting from the UFS and uses the UFS for non-volatile storage.
- SDIO controller

  An SDIO controller supports the SDIO3.0 protocol and is backward compatible. It is used to support extended peripherals compatible with related protocols, such as Wi-Fi chips.
- SD card controller

  An SD card controller supports the SD 3.0 protocol, and is backward compatible with the SD 2.0 protocol. The controller connects to external SD cards that comply with the default-speed, high-speed, and UHS-I specifications. The SD card controller is used to extend the non-volatile storage capacity of the system.
- DRAM controller

  A DRAM controller supports the 4-channel low-power double data rate 4X (LPDDR4X) synchronous dynamic random access memory (SDRAM). Each channel supports at most two ranks. As the major dynamic memory of the system, the LPDDR4X SDRAM provides at most 8-GB dynamic storage space and up to 29.2 GB/s theoretical access bandwidth.

5.2 Storage Solution

Table 5-1 lists the storage solution supported by the Hi3670.

Table 5-1 Storage solution

No.	Solution Description
1	LPDDR4X SDRAM + UFS + SD card (SD card is optional)

The symmetric 4-channel LPDDR4X SDRAM is supported. The data width of each channel is 16 bits. Each channel supports at most 2 chip selects. The maximum operating frequency of the LPDDR4X interface is 18xx MHz.

The UFS supports 2-lane TX+RX channels and PWM G1–G4 and HS G1–G3 rate A/B modes.

An SD card supports the 4-bit width and the highest speed level of SDR104 (200 MHz), and is backward compatible with multiple modes such as SDR50, SDR25, and SDR12.

5.3 SD/SDIO

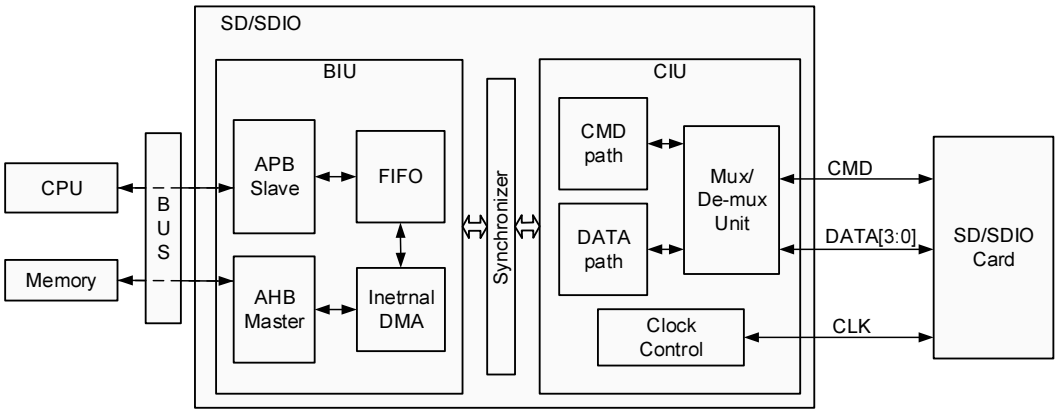
The SD/SDIO controller processes the read/write operations on the SD card, and supports extended peripherals such as Wi-Fi devices based on the secure digital input/output (SDIO) protocol. The Hi3670 provides two SD/SDIO controllers (SD and SDIO0), which are used to control the SD card and the Wi-Fi device that uses the SDIO interface, respectively.

The SD/SDIO controller controls the devices that comply with the following protocols:

- Secure Digital memory (SD mem-version 3.0, compatible with 2.0 and 1.1)
- Secure Digital I/O (SDIO-version 3.0, compatible with 2.0)

Figure 5-1 shows the functional block diagram of the SD/SDIO controller.

Figure 5-1 Functional block diagram of the SD/SDIO controller



The SD/SDIO controller connects to the system through the internal bus. It consists of the following units:

- Bus interface module: Provides the advanced microcontroller bus architecture (AMBA) AHB master and advanced peripheral bus (APB) slave interfaces. The registers are configured and the FIFO is read and written through the APB slave interface. The internal DMA can control the read and write operations on the FIFO data through the AHB master interface.
- Card interface module: Processes protocol-related content and clocks.
  - Command path: Transmits commands and receives responses.
  - Data path: Reads and writes data by working with the command path.
  - Codec unit: Encodes and decodes the input and output data based on protocols, respectively.

  - Control unit of the interface clock: Determines whether to enable or disable the interface clock, or divides the frequency of the cclk_in clock and uses the output clock as the operating clock of the SD card as required.

The SD/SDIO controller has the following features:

- Internal DMA data transmission
- 256-bit FIFO depth and 32-bit width, configurable FIFO threshold and burst size during DMA transfer
- FIFO overflow and underflow interrupt alarms to avoid errors during data transmission
- CRC generation and check for data and commands
- Configurable interface clock frequency
- Disabling of the SD/SDIO controller clock and interface clock in low-power mode
- 1-bit and 4-bit data transfer and SDIO interrupt detection
- Read and write operations on data blocks with the size ranging from 1 byte to 512 bytes
- Suspend, resume, and read wait operations on an SDIO card
- DDR50 mode not supported

5.4 UFS

The UFS controller is used to receive and transmit commands targeted for the UFS mass storage devices and process the data read and write operations on these devices. The UFS is a simple and high-performance serial interface that supports mass storage media. It is used for the mobile phone system.

The UFS controller supports the following features:

- JEDEC UFS 2.1 protocol
  - Higher speed up to HS-G3 (High-Speed Gear 3)
  - Symmetric 2RX-2TX lanes, support two lanes
  - Auto-hibernate entry and exit sequence
- JEDEC UFSHCI 2.1 protocol
  - Support up to 32 task requests
  - Support up to 8 task management requests
  - Support to pre-fetch more than one PRD entry (up to 16 PRD entries)
  - Clock gating ready design
- MIPI UniPro 1.6 and M-PHY 3.1 protocols
  - SKIP symbol insertion
  - Scrambling for EMI mitigation
  - HS-Gear3 adaption
  - Advanced granularity support

6 Interface Control

6.1 USB

The USB 3.0 module of the Hi3670 includes the USB 3.0 controller, USB 3.0 Combo PHY, and USB audio controller.

The USB 3.0 can be used either as a host or device. As a device, the USB 3.0 connects to the PC or USB host. As a host, the USB 3.0 connects to the USB flash drive or USB device.

The USB audio controller supports the xHCI and AC3 protocols.

The USB module has the following features:

- 5 Gbps super speed (SS), 480 Mbps high speed (HS), 12 Mbps full speed (FS), and 1.5 Mbps low speed (LS).

  Note: The USB 3.0 serving as a device does not support the LS mode.
- SS, HS, FS, and LS use the same programming model.
- Data flow mode
- Allocation of multiple data flows and variable data flows
- 1 to 16 bursts
- Integrated with five clock domains:
  - PIPE PHY (125/156.25/250/312.5/500/625 MHz)
  - UTMI+PHY (30/60 MHz) or ULPI PHY (60 MHz)
  - MAC (125 MHz)
  - BUS clock domain
  - RAM clock domain
- Internal DMA controller
- Low power consumption
- The LPM protocol can be applied to the U0, U1, U2, and U3 states of USB 2.0 and USB 3.0.
- Hardware-controlled LPM can be applied in host mode.
- The endpoint supports dynamic allocation of FIFO memory resources.
- The endpoint FIFO size is not changed in the power of 2.
- (Micro-) SOFs in LS or HS/FS mode support the Keep-Alive feature.
- Standard USB software control commands

- Hardware-controlled USB bus level and packet level error processing.
- Some registers in an internal RAM can be used to reduce the number of logical gates.
- Low MIPS requirements

The USB audio controller has the following features:

- USB 2.0 protocol
- xHCI protocol
- HW-LPM
- AC3 protocol
- A maximum of 32 devices
- A maximum of 16 periodic endpoints

6.2 UART

The universal asynchronous receiver transmitter (UART) performs serial-to-parallel conversion on the receive (RX) data and parallel-to-serial conversion on the transmit (TX) data.

The Hi3670 integrates nine UARTs and provides nine UART interfaces for external communication. All the UARTs except for UART7 support flow control. The UARTs described here do not include the UART used for modem debugging.

UART6 supports up to 6 M baud rate, and other UARTs support up to 9 M baud rate.

The UART module has the following features:

- Configurable data bit width and stop bit width
- The data bit width can be set to 5, 6, 7, or 8 bits.
- The stop bit width can be set to 1 or 2 bits.
- Parity check or no check bit
- Configurable programmable transfer rate, up to 9 Mbit/s
- Data transfer in direct memory access (DMA) mode (UART6 and UART7 do not support DMA.)
- RX FIFO interrupt, TX FIFO interrupt, RX timeout interrupt, and error interrupt
- TX FIFO with 64-bit depth and 8-bit width and RX FIFO with 64-bit depth and 12-bit width (The depth of the TX FIFO and RX FIFO is 16 bits for UART7 and UART8 and 64 bits for other UARTs.)
- Infrared Data Association (IrDA) serial infrared mode

6.3 SPI

The serial peripheral interface (SPI) transfers data in serial or parallel mode. In the Hi3670, the SPI is used as the master interface to implement synchronous serial communication with external devices. The SPI does not serve as a slave.

The Hi3670 provides five SPIs: SPI0 to SPI4. SPI2, SPI3, and SPI4 have four chip selects (CSs), SPI0 has two CSs, and SPI1 has one CS.

The SPI module has the following features:

- Programmable interface clock frequency
- Two separate 256 x 16-bit FIFOs: one TX FIFO and one RX FIFO
- SPI frame formats
- Programmable length of the serial data frame: 4 bits to 16 bits
- Programmable threshold of the TX FIFO and RX FIFO to request interrupts
- Programmable threshold of the TX FIFO and RX FIFO to request the DMA to implement burst transfer
- TX FIFO interrupts, RX FIFO interrupts, RX timeout interrupts, and RX FIFO overflow interrupts can be independently masked.
- Internal loopback test
- DMA operation

6.4 I²C

The I^2C controller uses the SCL and SDA signal lines to communicate with off-chip devices that provide I^2C interfaces. The I^2C interface can transmit data to and receive data from the slave device on the I^2C bus in compliance with I^2C specifications V2.1. In the Hi3670, the I^2C controller can only be used as the master device.

The Hi3670 integrates eight I^2C modules.

6.5 GPIO

The Hi3670 has 29 common GPIO modules: GPIO0–17, GPIO20–21, and GPIO22–28. The peripheral area has 20 GPIO modules (GPIO0–17 and GPIO20–21), and the always-on area (AON_SUBSYS) has nine GPIO modules (GPIO18–19 and GPIO22–28).

The Hi3670 provides two secure GPIO modules: one (GPIO0_SE) in the peripheral area and one (GPIO1_SE) in the always-on area (AON_SUBSYS).

The Hi3670 also has a GPIO module inside the independent subsystem, for example, four groups of GPIO (GPIO0_SH–GPIO3_SH) of the sensor hub.

Each GPIO module corresponds to a group of eight GPIO interfaces. Each GPIO group generates three interrupts, which are sent to the GIC, LPMCU, and CCPU, respectively. (The interrupts of GPIO0SH to GPIO3SH are sent to the GIC and IOMCU, respectively.) The source interrupts of the three index interrupts share the eight GPIO interfaces in the same group but have independent mask bits.

Table 6-1 lists related GPIO information.

Table 6-1 GPIO group information

GPIO Type	Instance	Valid GPIO Pins	Power Domain of the Connected IOC	Interrupt Registration Support
AO area	GPIO22–27	GPIO_176–GPIO_223	Always-on area	GIC, LPMCU, CCPU
	GPIO28	GPIO_224–GPIO_231	Always-on area	GIC, LPMCU, IOMCU
	GPIO1_SE	GPIO_008_SE–GPIO_015_SE	Always-on area	GIC, LPMCU
	GPIO18–19	GPIO_144–GPIO_151	Always-on area	GIC, CCPU, and LPMCU
Peripheral area	GPIO0–15	GPIO_001, GPIO_003–GPIO_027, GPIO_029–GPIO_047, GPIO_049–GPIO_096,	Power-off area	GIC and CCPU
	GPIO16–17	GPIO_128–GPIO_137	IOC_MMC1 (power-off area)	GIC and CCPU
	GPIO20–21	GPIO_160–GPIO_167, GPIO_168–GPIO_171	IOC_MMC0 (power-off area)	GIC and CCPU
	GPIO0_SE	GPIO_000_SE–GPIO_004_SE GPIO_006_SE–GPIO_007_SE	Power-off area	GIC and LPMCU
SensorHub GPIO	GPIO0_SH–GPIO3_SH	GPIO_000_SH–GPIO_031_SH	Always-on area	GIC and IOMCU
		GPIO_028_SH–GPIO_031_SH	Power-off area	GIC and IOMCU

Each GPIO group provides eight programmable I/O pins to generate output signals or collect input signals for specific applications.

The GPIO module has the following features:

- Configures each GPIO pin as the input, output, or OD output.
  - When acting as an input pin, a GPIO pin can be used as an interrupt source and supports independent interrupt control.
  - When acting as an output pin, a GPIO pin can be independently set to 0 or 1.
  - When a GPIO pin acts as the OD output, pull-up control is required on the board. The output is enabled by using the GPIODIR register to implement the "wired AND" function on the board.
- Queries the statuses of initial and masked interrupts.

- Supports the interrupt wakeup system. The GPIO enable interrupt needs to be configured before the system enters the sleep state. After the system enters the sleep state, the GPIO will generate an interrupt to wake up the system when peripheral inputs change.
- Does not support separate soft reset.

6.6 PWM

The Hi3670 integrates one pulse width modulation (PWM) module that provides two groups of independent PWM output signals. These signals are used to adjust the LCD backlight and control the keypad light brightness and ringtones.

The frequency of the two PWM output signals can be adjusted. The duty cycle is adjustable from 0%–100%. However, because the two channels use the common pre-frequency processing, the frequencies of the two groups of PWM output signals cannot be completely independently controlled.

The PWM has the following features:

- The common pre-division coefficient can be configured. The values of prescaling registers 0 and 1 of the two channels can be configured.
- The PWM output frequency can be configured. The output frequencies of the two channels can be configured separately.
  - The PWM output frequency of channel X is determined by the common pre-division coefficient and the period matching register of each channel.
  - PWM output frequency of channel X = $\frac{pclk}{(\text{pwm\_pr0}+1)\times(\text{pwm\_pr1}+1)\times(\text{pwm\_chX}+1)}$
- The duty cycle can be adjusted, and the PWM output duty cycles of the two channels can be adjusted separately.
  - PWM output duty cycle of channel X = $\frac{pwm\_chX\_mr0}{(pwm\_chX\_mr+1)}\times 100\%$
  - When **pwm_chX_mr0** is greater than **pwm_chX_mr**, the PWM output duty cycle of channel X is 100%.
- The output PWM signal of each channel can be configured as the single-edge or dual-edge PWM output.
- The phase configuration of the output PWM signal of each channel can be configured separately.
- The output signals of the two channels can be enabled through registers, respectively. When the output enable register of the corresponding channel is cleared, the output signal is 0. When the corresponding register is set to 1, the signal is output as the modulated signal.

6.7 PCIe

The Hi3670 contains one 1-lane PCIe interface module with the lane width of x1. The PCIe bus uses the serial point-to-point communication mode. The transmission rate of each channel in each direction can reach 2.5 Gbps@Gen1, 5 Gbps@Gen2, and 8 Gbps@Gen3. The PCIe bus has the protocol layer architecture. The introduced quality of service (QoS), traffic class

(TC), and virtual channel (VC) technologies enable other software to be backward compatible with the PCI software.

The PCIe interface module has the following features:

- Compliant with PCIe base specification revision 3.1 (maximum rate: Gen3 8 Gbps)
- 100 MHz differential reference clock
- One x1 link, which can work in Gen1 (2.5 Gbps) or Gen2 (5 Gbps) mode.
- One VC and eight TCs
- PCI-PM and ASPM low-power management
- L1 Substates, including L1.1 and L1.2
- Message signaled interrupt (MSI)
- Integrated with the message generator. Messages can be sent by operating the PCIeCTRL register.
- Capable of working in Root Complex (RC) mode
- Reads or writes to PCIe registers over the AXI slave through the shared data bus interface (DBI).
- The AXI slave interface supports the 32-bit address bus and 128-bit data bus.
- The AXI master interface supports the 39-bit address bus and 128-bit data bus.