![National Semiconductor logo] **National Semiconductor**

Process C3
N-Channel Power MOSFET

TL/G/10040–C9

DESCRIPTION

These dice are n-channel, enhancement mode, power MOSFETs designed especially for high power, high speed applications, such as power supplies, AC and DC motor control and high energy pulse circuits.

This process is available in the following device types:

TO-204 (Case 42)	TO-220 (Case 37)
IRF330	IRF730
IRF331	IRF731
IRF332	IRF732
IRF333	IRF733
	MTP5N35
	MTP5N40

Electrical Characteristics T_C = 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{DSS}	Drain to Source Voltage (Note 1)	I_D = 250 µA; V_{GS} = 0V	400		V
I_{DSS}	Zero Gate Voltage Drain	V_{DS} = Rated Voltage V_{GS} = 0V		250	µA
I_{GSS}	Gate Leakage Current	V_{DS} = ±20V; V_{DS} = 0V		100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	I_D = 250 µA; V_{DS} = V_{GS}	2.0	4.0	V
$R_{DS(ON)}$	Static On-Resistance (Note 2)	V_{GS} = 10V; I_D = 3A		1.0	Ω
g_{FS}	Forward Transconductance	V_{DS} = 10V; I_D = 3A	3.0		Siemens
C_{iss}	Input Capacitance	V_{DS} = 25V; V_{GS} = 0V f = 1 MHz		900	pF
C_{oss}	Output Capacitance			300	pF
C_{rss}	Reverse Transfer			80	pF
$t_{d(on)}$	Turn-On Delay Time (Note 3)	V_{DD} = 175V; I_D = 3A V_{GS} = 10V; R_{GEN} = 15Ω		30	ns
t_r	Rise Time	R_{GS} = 15Ω		35	ns
$t_{d(off)}$	Turn-Off Delay Time			55	ns
t_f	Fall Time			35	ns
Q_g	Total Gate Charge	V_{GS} = 10V; I_D = 7A V_{DD} = 180V		30	nC

Note 1: T_J = +25°C to +150°C.

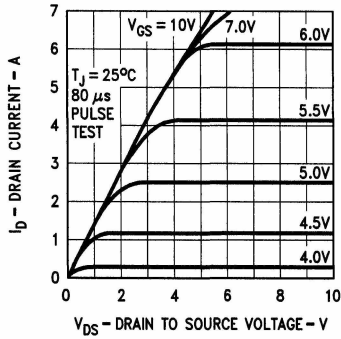**Note 2:** Pulse test: Pulse Width ≤ 80 µs, Duty Cycle ≤ 1%.

Note 3: Switching time measurements performed on LEM TR-58 test equipment.
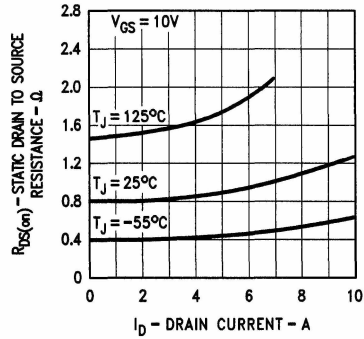
Typical Performance Characteristics
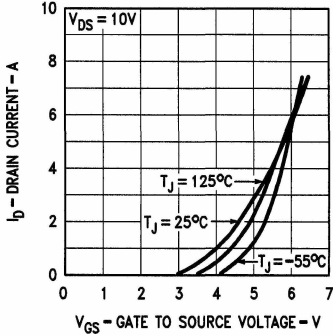
Figures 4–6 for IRF332/333/732/733 only.
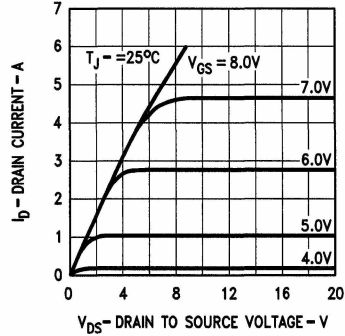

TL/G/10040–D0

FIGURE 1. Output Characteristics

TL/G/10040–D1

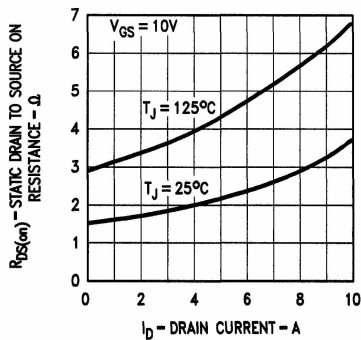**FIGURE 2. Static Drain to Source Resistance
vs Drain Current**

TL/G/10040–D2
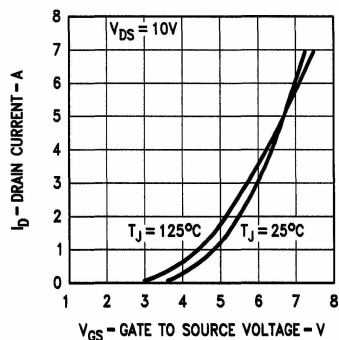
FIGURE 3. Transfer Characteristics

TL/G/10040–D3

FIGURE 4. Output Characteristics

TL/G/10040–D4

**FIGURE 5. Static Drain to Source On-Resistance
vs Drain Current**

TL/G/10040–D5

FIGURE 6. Transfer Characteristics
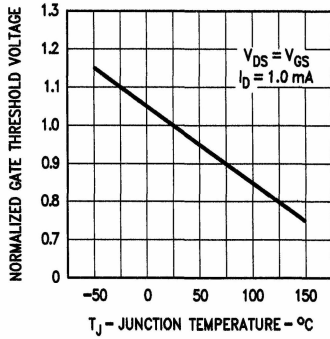
Typical Performance Characteristics (Continued)

TL/G/10040–D6

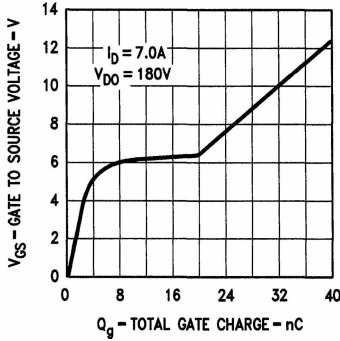**FIGURE 7. Temperature Variation of Gate to Source Threshold Voltage**

TL/G/10040–D7

FIGURE 8. Capacitance vs Drain to Source Voltage

TL/G/10040–D8

FIGURE 9. Gate to Source Voltage vs Total Gate Charge
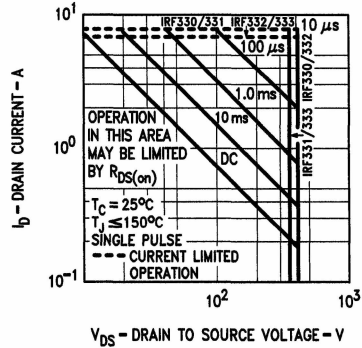
TL/G/10040–D9

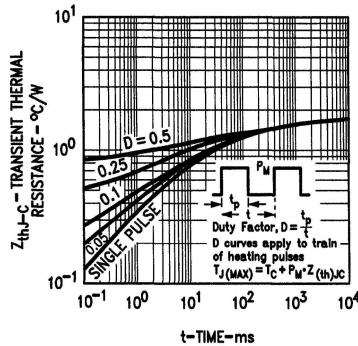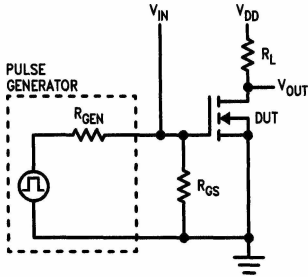**FIGURE 10. Forward Biased Safe Operating Area**

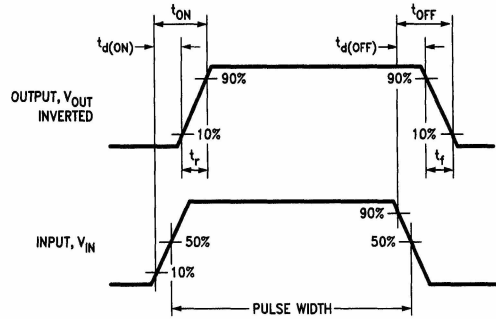TL/G/10040–E0

FIGURE 11. Transient Thermal Resistance

Typical Electrical Characteristics

TL/G/10040–E1

FIGURE 12. Switching Test Circuit

TL/G/10040–E2

FIGURE 13. Switching Waveforms