
DESCRIPTION

Process 95 is a monolithic dual JFET with a diode isolated substrate. It is intended for operational amplifier input buffer applications. Processing results in low input bias current and virtually unmeasurable offset current. Low noise voltage and high CMRR for critical 1/f applications.

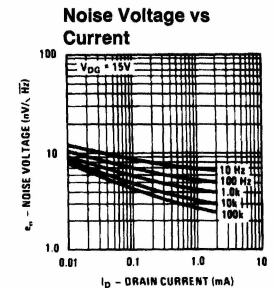
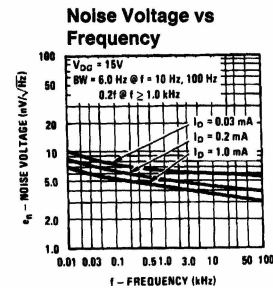
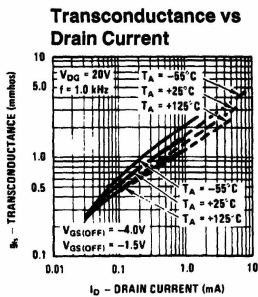
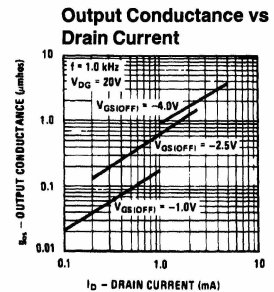
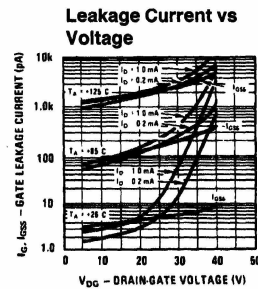
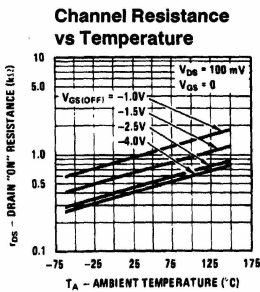
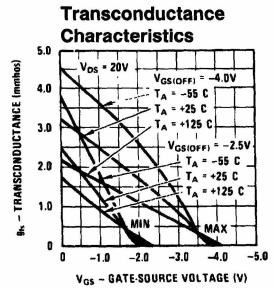
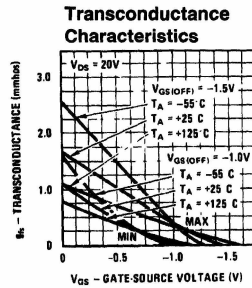
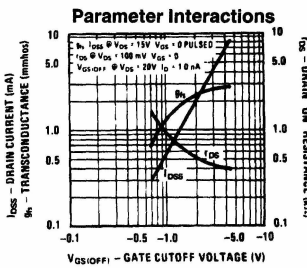
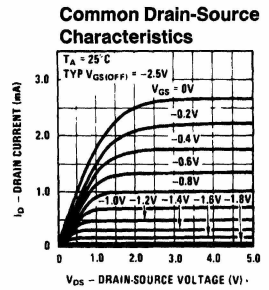
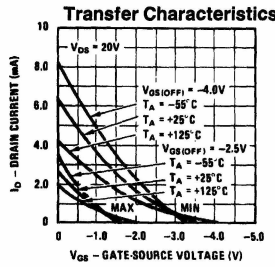
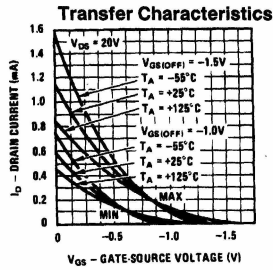
Electrical Characteristics ($T_A = 25^\circ\text{C}$)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------------------------|---------------------------------|--|------|------|------|------------------------|
| BV_{GSS} | Gate-Source Breakdown Voltage | $V_{DS} = 0V, I_G = -1 \mu A$ | -40 | -70 | | V |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 15V, V_{GS} = 0V$ | 0.5 | 3.0 | 8.0 | mA |
| g_{fs} | Forward Transconductance | $V_{DS} = 15V, V_{GS} = 0V$ | 1.0 | 2.5 | 4.0 | mmhos |
| g_{fs} | Forward Transconductance | $V_{DG} = 15V, I_D = 0.2 \text{ mA}$ | 0.5 | 0.7 | | mmhos |
| I_{GSS} | Gate Leakage | $V_{GS} = -20V, V_{DS} = 0V$ | | -5.0 | -100 | pA |
| $V_{GS(OFF)}$ | Pinch Off Voltage | $V_{DS} = 15V, I_D = 1 \text{ nA}$ | -0.5 | -2.5 | -4.0 | V |
| C_{iss} | Input Capacitance | $V_{DS} = 15V, V_{GS} = 0V, f = 1 \text{ MHz}$ | | 10 | 14 | pF |
| e_n | Noise Voltage | $V_{DS} = 15V, I_D = 0.2 \text{ mA}, f = 10 \text{ Hz}$ | | 8.0 | 30 | nV/\sqrt{Hz} |
| e_n | Noise Voltage | $V_{DS} = 15V, I_D = 0.2 \text{ mA}, f = 100 \text{ Hz}$ | | 6.0 | 10 | nV/\sqrt{Hz} |
| g_{os} | Output Conductance | $V_{DG} = 15V, I_D = 0.2 \text{ mA}$ | | 0.3 | 1.0 | μmhos |
| C_{rss} | Feedback Capacitance | $V_{DS} = 15V, V_{GS} = 0V, f = 1 \text{ MHz}$ | | 3.5 | 5.0 | pF |
| $ V_{GS1} - V_{GS2} $ | Differential Match | $V_{DG} = 20V, I_D = 0.2 \text{ mA}$ | | 6.0 | 25 | mV |
| $\Delta V_{GS1} - V_{GS2}$ | Differential Match Drift | $V_{DG} = 20V, I_D = 0.2 \text{ mA}$ | | 9.0 | 60 | $\mu V/^\circ\text{C}$ |
| CMRR | Common-Mode Rejection | $V_{DG} = 20V, I_D = 0.2 \text{ mA}$ | 86 | 115 | | dB |

This process is available in the following device types. *Denotes preferred parts.

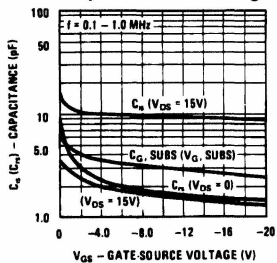
TO-71 (NS Package 12)

| | |
|---------|---------|
| 2N5515 | *2N5522 |
| 2N5516 | *2N5523 |
| 2N5517 | *2N5524 |
| 2N5518 | *2N6483 |
| 2N5519 | *2N6484 |
| *2N5520 | *2N6485 |
| *2N5521 | |

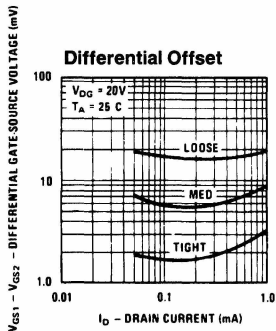


Process 95

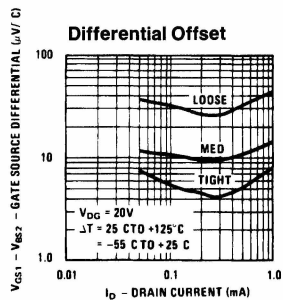
Capacitance vs Voltage



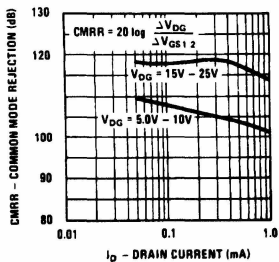
Differential Offset



Differential Offset



CMRR vs Drain Current



TL/G/10035-52