NEC

MOS INTEGRATED CIRCUIT

μPD6P9

4-BIT SINGLE-CHIP MICROCONTROLLER
FOR INFRARED REMOTE CONTROL TRANSMISSION

DESCRIPTION

The μPD6P9 is a microcontroller for infrared remote control transmitters and is provided with a one-time PROM as the program memory.

Because users can write programs for the μPD6P9, it is ideal for program evaluation and small-scale production of application systems that use the μPD67, 67A, 68, 68A, 69, or 69A.

★ The μPD6P9 has two types: μPD6P9M1 and 6P9M3. The differences between two types are as follows.

	μPD6P9M1	μPD6P9M3
Corresponding mask ROM version	μPD67, 67A, 68, 68A, 69, 69A (normal instruction execution version)	μPD69A (high-speed instruction execution version)
Instruction execution time	16 μs (f_X = 4 MHz)	8 μs (f_X = 4 MHz)

When reading this document, also refer to the following documents.

μPD67, 67A, 68, 68A, 69 Data Sheet: U14935E
μPD69A Data Sheet: U16363E

FEATURES

- Program memory (one-time PROM): 4074 × 10 bits
- Data memory (RAM): 128 × 4 bits
- On-chip carrier generator for infrared remote control: The high-level and low-level width can be set separately from 250 ns to 64 μs (@ f_X = 4 MHz operation) via modulo registers
- 9-bit programmable timer: 1 channel
- ★ Instruction execution time: 16 μs (@ f_X = 4 MHz) (μPD6P9M1)
  8 μs (@ f_X = 4 MHz) (μPD6P9M3)
- Stack level: 1 level (stack RAM is for data memory RF as well)
- I/O pins ($K_{I/O}$): 8 units
- Input pins (K_I): 4 units
- Sense input pins (S_0, S_2): 2 units
- $S_1/\overline{LED}$ pin (I/O): 1 unit (when in output mode, this is the remote control transmission display pin)
- Power supply voltage: V_{DD} = 2.2 to 3.6 V
- Operating ambient temperature: T_A = –40 to +85°C
- Oscillator frequency: f_X = 3.5 to 4.5 MHz
- On-chip POC circuit and RAM retention detector
- ★ Capacitor for oscillator: Not available

APPLICATIONS

Infrared remote control transmitters (for AV and household electric appliances)

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Document No. U15144EJ1V0DS00 (1st edition)
Date Published November 2002 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

ORDERING INFORMATION

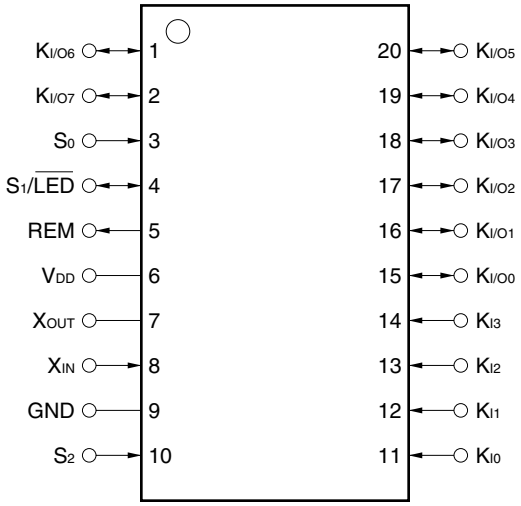
Part Number	Package
μPD6P9M1MC-5A4	20-pin plastic SSOP (7.62 mm (300))
★ μPD6P9M3MC-5A4	20-pin plastic SSOP (7.62 mm (300))

PIN CONFIGURATION (TOP VIEW)

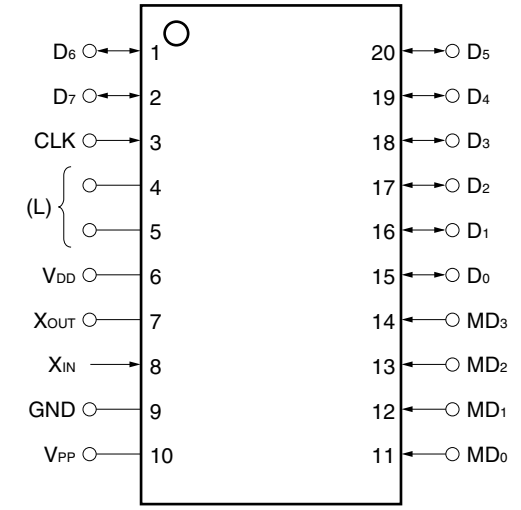
20-pin plastic SSOP (7.62 mm (300))

★ • **μPD6P9M1MC-5A4, 6P9M3MC-5A4**

(1) Normal operation mode



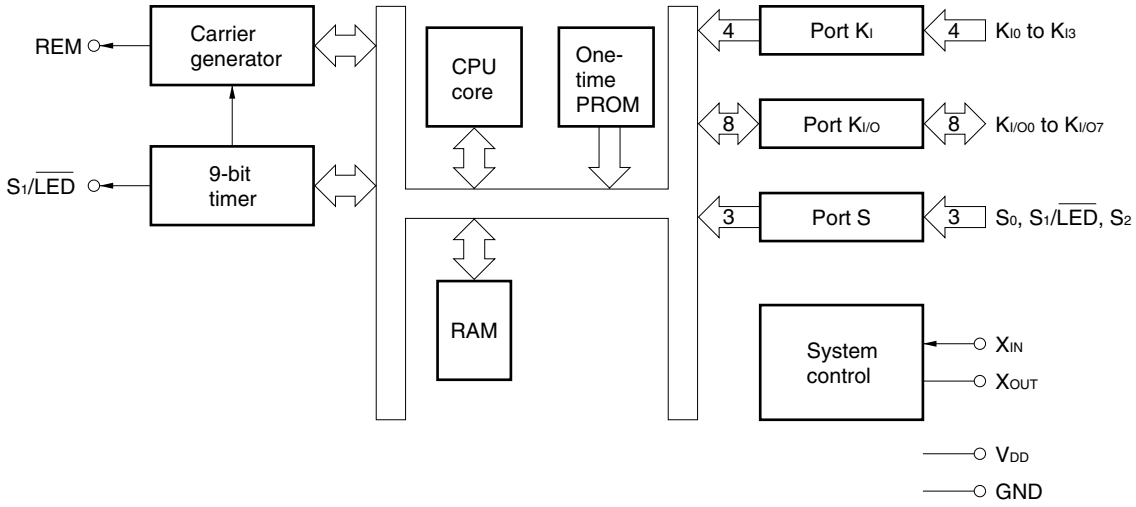
(2) PROM programming mode



Caution The item in parentheses indicates the processing of pins not used in the PROM programming mode.

L: Connect each of these pins to GND via a pull-down resistor.

BLOCK DIAGRAM



LIST OF FUNCTIONS

Item	μPD6P9	
	μPD6P9M1	μPD6P9M3
ROM capacity	4074 × 10 bits One-time PROM	
RAM capacity	128 × 4 bits	
Stack	1 level (shared with RF of RAM)	
I/O pins	Key input (K_I): 4 pins Key I/O ($K_{I/O}$): 8 pins Key expansion input (S_0, S_1, S_2): 3 pins Remote control transmission display output ($\overline{LED}$): 1 pin (shared with S_1 pin)	
Number of keys	32 keys 56 keys (when expanded by key expansion input)	
Clock frequency	Ceramic oscillation f_X = 3.5 to 4.5 MHz	
★ Instruction execution time	16 μs (@ f_X = 4 MHz)	8 μs (@ f_X = 4 MHz)
Carrier frequency	The high-level and low-level width can be set separately from 250 ns to 64 μs (@ f_X = 4 MHz operation) via modulo registers	
Timer	9-bit programmable timer: 1 channel, timer clock: f_X/64	
POC circuit	On chip	
RAM retention detector	On chip	
★ Capacitor for oscillation	Not available	
Supply voltage	V_{DD} = 2.2 to 3.6 V	
Operating ambient temperature	T_A = –40 to +85°C	
Package	20-pin plastic SSOP (7.62 mm (300))	

CONTENTS

1. PIN FUNCTIONS

1.1 Normal Operation Mode

Pin No.	Symbol	Function	Output Format	After Reset
1 2 15 to 20	$K_{I/O0}$ to $K_{I/O7}$	8-bit I/O port. I/O mode can be switched in 8-bit units. In input mode, a pull-down resistor is added. In output mode, these pins can be used as a key scan outputs from the key matrix.	CMOS Push-pull[Note 1]	High-level output
3	S_0	Input port. This pin can also be used as a key return input from the key matrix. In input mode, the use of a pull-down resistor for the S_0 and S_1 ports can be specified by software in 2-bit units. If input mode is released by software, this pin is placed in the OFF mode and enters a high-impedance state.	—	High-impedance (OFF mode)
4	$S_1/\overline{LED}$	I/O port. In input mode (S_1), this pin can also be used as a key return input from the key matrix. The use of a pull-down resistor for the S_0 and S_1 ports can be specified by software in 2-bit units. In output mode ($\overline{LED}$), this pin becomes the remote control transmission display output (active low). When the remote control carrier is output from the REM output, this pin outputs a low level from the $\overline{LED}$ output in synchronization with the REM signal.	CMOS push-pull	High-level output ($\overline{LED}$)
5	REM	Infrared remote control transmission output. The output is active high. The carrier high-level and low-level width can each be freely set in a range of 250 ns to 64 μs (@ f_X = 4 MHz) using software.	CMOS push-pull	Low-level output
6	V_{DD}	Power supply	—	—
7 8	X_{OUT} X_{IN}	These pins are connected to system clock ceramic resonators.	—	Low level (oscillation stopped)
9	GND	GND pin	—	—
10	S_2	Input port. The use of the STOP mode release of the S_2 port can be specified by software. When using this pin as a key input from the key matrix, enable the use of the STOP mode release (at this time, a pull-down resistor is connected internally.) When the STOP mode release is disabled, this pin can be used as an input port that does not release the STOP mode even if the release condition is established (at this time, a pull-down resistor is not connected internally.)	—	Input (high impedance, STOP mode release cannot be used)
11 to 14	K_{I0} to K_{I3}[Note 2]	4-bit input port. These pins can be used as key return inputs to the key matrix. The use of pull-down resistors can be specified by software in 4-bit units.	—	Input (low-level)

Notes 1. Note that the drive capability of the low-level output side is held low.

2. In order to prevent malfunction, do not input a high-level signal to pins K_{I0} to K_{I3} (leaving these pins open is possible, however, when these pins are left open, do not disconnect any connected pull-down resistors) when POC is released due to supply voltage startup.

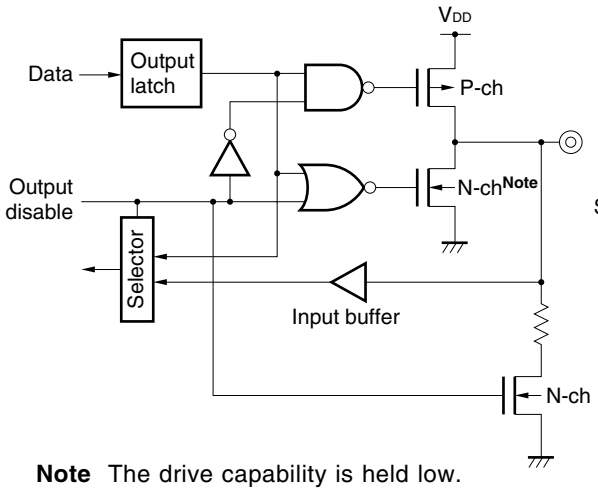
1.2 PROM Programming Mode

Pin No.	Symbol	Function	I/O
1, 2 15 to 20	D_0 to D_7	8-bit data I/O when writing/verifying program memory	I/O
3	CLK	Clock input for updating address when writing/verifying program memory	Input
6	V_{DD}	Power Supply Supply +6 V to this pin when writing/verifying program memory.	–
7	X_{OUT}	Clock necessary for writing program memory. Connect a 4 MHz ceramic resonator to these pins.	–
8	X_{IN}		Input
9	GND	GND	–
10	V_{PP}	Supplies voltage for writing/verifying program memory. Apply +12.5 V to this pin.	–
11 to 14	MD_0 to MD_3	Input for selecting operation mode when writing/verifying program memory	Input

1.3 Pins I/O Circuits

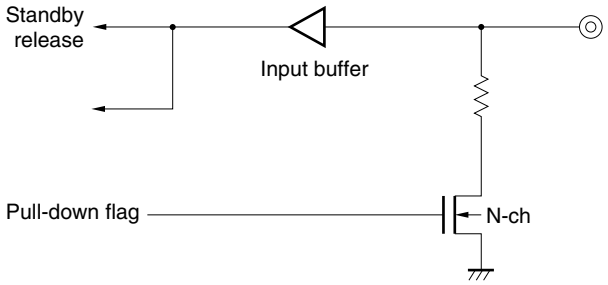
The I/O circuits of the μPD6P9 pins are shown in partially simplified forms below.

(1) $K_{I/O0}$ to $K_{I/O7}$

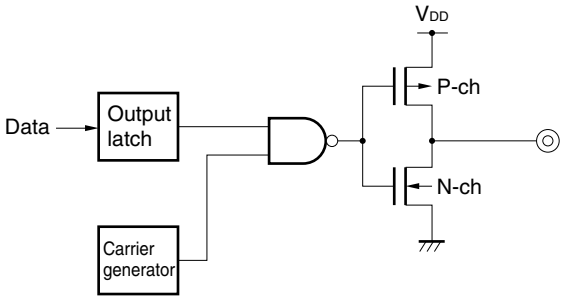


Note The drive capability is held low.

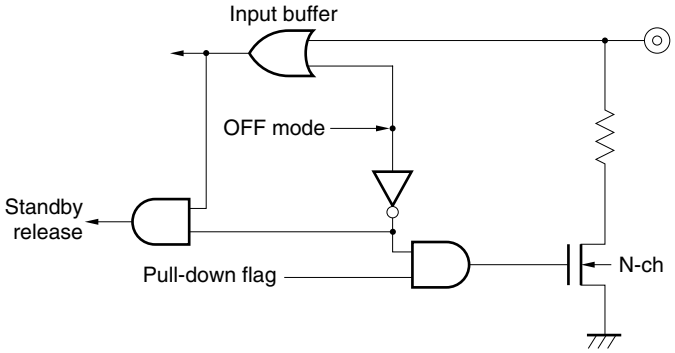
(2) K_{I0} to K_{I3}



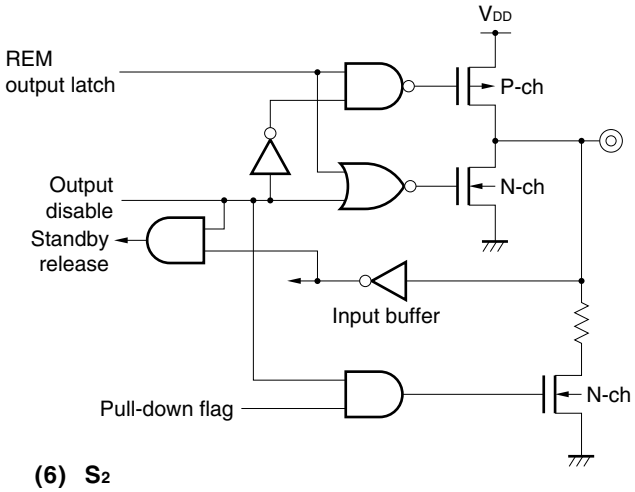
(3) REM



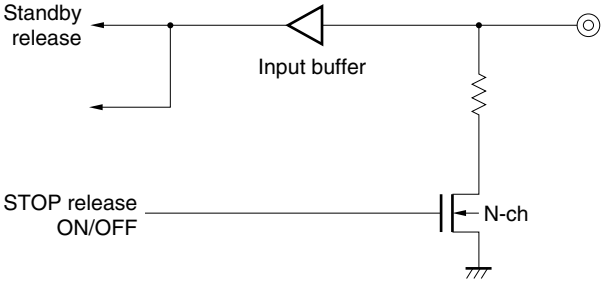
(4) S_0



(5) $S_1/\overline{LED}$



(6) S_2



1.4 Recommended Connection of Unused Pins

The following connections are recommended for unused pins in the normal operation mode.

Table 1-1. Connections for Unused Pins

Pin		Connection	
		Inside the Microcontroller	Outside the Microcontroller
$K_{I/O}$	Input mode	—	Leave open
	Output mode	High-level output	
REM		—	
$S_1/\overline{LED}$		Output mode ($\overline{LED}$) setting	
S_0		OFF mode setting	Directly connect these pins to GND
S_2		—	
K_I		—	

Caution The I/O mode and the pin output level are recommended to be fixed by setting them repeatedly in each loop of the program.

1.5 Notes on Using K_I Pin After Reset

In order to prevent malfunction, do not input a high-level signal to pins K_{I0} to K_{I3} (leaving these pins open is possible, however, when these pins are left open, do not disconnect any connected pull-down resistors) when POC is released due to supply voltage startup.

★ 2. DIFFERENCES BETWEEN μPD67, 67A, 68, 68A, 69, 69A, AND μPD6P9

Table 2-1 shows the differences between the μPD67, 67A, 68, 68A, 69, 69A, and μPD6P9.

The only differences between these models are the program memory, data memory, timer, POC detection voltage, and supply voltage; the other CPU functions and internal peripheral hardware are the same.

The electrical specifications also differ slightly. For the electrical specifications, refer to the data sheet of each model.

Table 2-1. Differences Between μPD67, 67A, 68, 68A, 69, 69A, and μPD6P9

Item		μPD6P9	μPD67	μPD67A	μPD68	μPD68A	μPD69	μPD69A
ROM		One-time PROM	Mask ROM					
		4074 × 10 bits	1002 × 10 bits		2026 × 10 bits		4074 × 10 bits	
RAM		128 × 4 bits	32 × 4 bits				128 × 4 bits	
Timer	Clock	fx/64						
	Output value	**Note 1**	**Note 2**	**Note 3**	**Note 2**	**Note 3**	**Note 2**	**Note 4**
POC detection voltage		V_{POC} = 1.85 V (TYP.)						**Note 5**
Supply voltage		V_{DD} = 2.2 to 3.6 V	V_{DD} = 2.0 to 3.6 V					**Note 6**
Electrical specifications		Some electrical specifications, such as data retention voltage and current consumption, differ. Refer to data sheet of each model for details.						

Notes 1. (Set value + 1) × 64/fx (μPD6P9M1), (set value + 0.5) × 64/fx (μPD6P9M3)

2. (Set value + 1) × 64/fx

3. (Set value + 1) × 64/fx – 4/fx

4. (Set value + 1) × 64/fx – 4/fx or (set value + 0.5) × 64/fx – 2/fx

5. V_{POC} = 1.85 V (TYP.) or V_{POC} = 1.7 V (TYP.) (mask option)

6. V_{DD} = 2.0 to 3.6 V or V_{DD} = 1.8 to 3.6 V

★ 3. INTERNAL CPU FUNCTIONS

3.1 Program Counter (PC): 12 Bits

The program counter (PC) is a binary counter that holds the address information of the program memory.

Figure 3-1. Program Counter Configuration

PC	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

The PC contains the address of the instruction that should be executed next. Normally, the counter contents are automatically incremented in accordance with the instruction length (byte count) each time an instruction is executed.

However, when executing jump instructions (JMP, JC, JNC, JF, JNF), the PC contains the jump destination address written in the operand.

When executing the subroutine call instruction (CALL), the call destination address written in the operand is entered in the PC after the PC contents at the time are saved in the address stack register (ASR). If the return instruction (RET) is executed after the CALL instruction is executed, the address saved in the ASR is restored to the PC.

After reset, the value of the PC becomes “000H”.

3.2 Stack Pointer (SP): 1 Bit

This is a 1-bit register that holds the status of the address stack register.

The stack pointer contents are incremented when the call instruction (CALL) is executed and decremented when the return instruction (RET) is executed.

When reset, the stack pointer contents are cleared to 0.

When the stack pointer overflows (stack level 2 or more) or underflows, the CPU is defined as hung up, a system reset signal is generated, and the PC becomes 000H.

As no instruction is available to set a value directly for the stack pointer, it is not possible to operate the pointer by means of a program.

3.3 Address Stack Register (ASR (RF)): 12 Bits

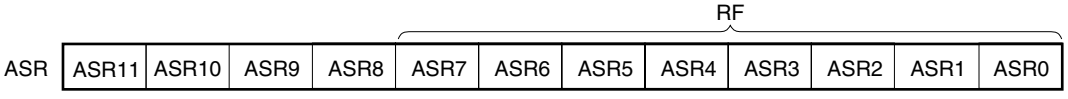
The address stack register saves the return address of the program after a subroutine call instruction is executed.

The lower 8 bits are allocated in RF of the data memory as a alternate-function RAM. The register holds the ASR value even after the RET instruction is executed.

After reset, it holds the previous data (undefined when turning on the power).

Caution If RF is accessed as the data memory, the higher 4 bits become undefined.

Figure 3-2. Address Stack Register Configuration



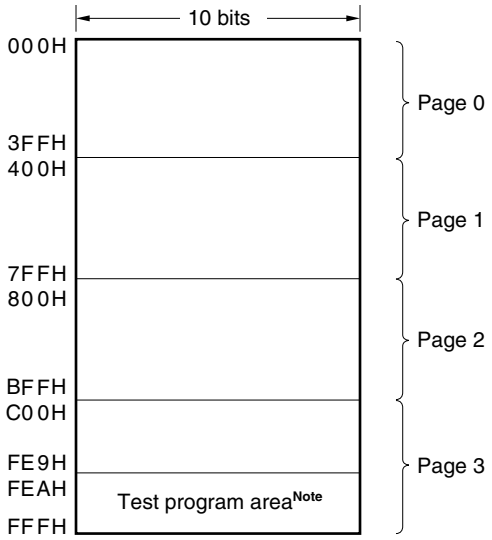
3.4 Program Memory (One-Time PROM): 4,074 Steps × 10 Bits

The one-time PROM consists of 10 bits per step, and is addressed by the program counter.

The program memory stores programs and table data, etc.

The 22 steps from FEAH to FFFH cannot be used in the test program area.

Figure 3-3. Program Memory Map



Note The unmounted area and test program area are designed so that a program or data placed in either of them by mistake is returned to the 000H address.

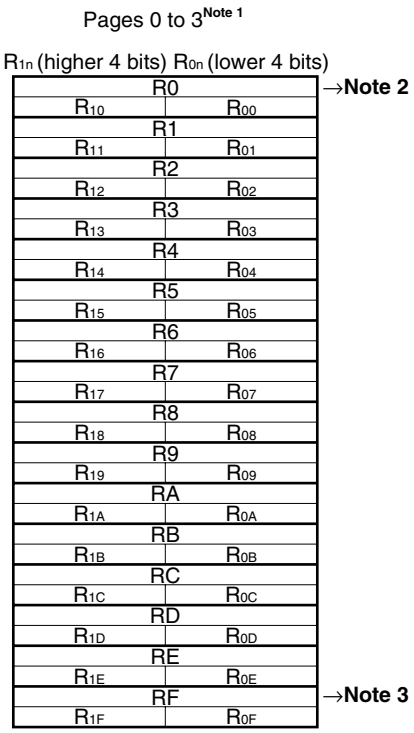
3.5 Data Memory (RAM): 128 × 4 Bits

The data memory, which is a static RAM consisting of 32 × 4 bits × 4 pages, is used to retain processed data. The data memory is sometimes processed in 8-bit units. R0 of page 0 can be used as the ROM data pointer.

RF of page 0 is also used as the ASR.

After reset, R0 of page 0 is cleared to 00H and R1 to RF of page 0 and pages 1 to 3 retain the previous data (undefined when turning on the power).

Figure 3-4. Data Memory Configuration



Notes 1. Pages 0 to 3 can be switched using bits 0 and 1 of control register 0.

2. R0 of page 0 alternately functions as the ROM data pointer (refer to **3.6 Data Pointer (DP)**).

3. RF of page 0 alternately functions as the PC address stack (refer to **3.3 Address Stack Register (ASR (RF))**.

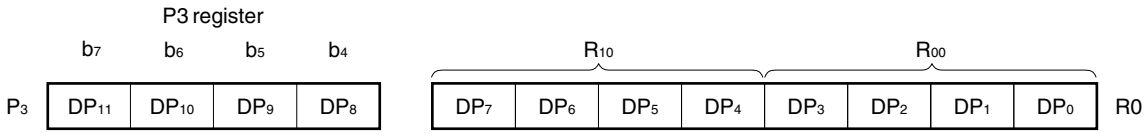
3.6 Data Pointer (DP): 12 Bits

The ROM data table can be referenced by setting the ROM address in the data pointer to call the ROM contents.

The lower 8 bits of the ROM address are specified by R0 of the data memory; and the higher 4 bits by bits 4 to 7 of the P3 register (CR0).

After reset, the pointer contents become 000H.

Figure 3-5. Data Pointer Configuration

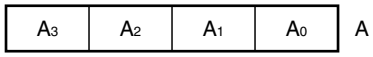


3.7 Accumulator (A): 4 Bits

The accumulator, which refers to a register consisting of 4 bits, plays a leading role in performing various operations.

After reset, the accumulator contents are left undefined.

Figure 3-6. Accumulator Configuration



3.8 Arithmetic and Logic Unit (ALU): 4 Bits

The arithmetic and logic unit (ALU), which refers to an arithmetic circuit consisting of 4 bits, executes simple (mainly logical) operations.

3.9 Flags

3.9.1 Status flag (F)

Pin and timer statuses can be checked by executing the STTS instruction to check the status flag.
The status flag is set (to 1) in the following cases.

- If the condition specified with the operand is met when the STTS instruction is executed
- When standby mode is released.
- When the release condition is met at the point of executing the HALT instruction. (In this case, the system does not enter the standby mode.)

Conversely, the status flag is cleared (to 0) in the following cases:

- If the condition specified with the operand is not met when the STTS instruction is executed.
- When the status flag has been set (to 1), the HALT instruction executed, but the release condition is not met at the point of executing the HALT instruction. (In this case, the system does not enter the standby mode.)

Table 3-1. Conditions for Status Flag (F) to Be Set by STTS Instruction

Operand Value of STTS Instruction				Condition for Status Flag (F) to Be Set
b_3	b_2	b_1	b_0	
0	0	0	0	High level is input to at least one of K_I pins.
	0	1	1	High level is input to at least one of K_I pins.
	1	1	0	High level is input to at least one of K_I pins.
	1	0	1	The down counter of the timer is 0.
1	Either of the combinations of b_2, b_1, and b_0 above.			[The following condition is added in addition to the above.] High level is input to at least one of S_0Note 1, S_1Note 1, or S_2Note 2 pins.

Notes 1. The S_0 and S_1 pins must be set to input mode (bit 2 and bit 0 of the P4 register are set to 0 and 1, respectively).

2. The use of STOP mode release for the S_2 pin must be enabled (bit 3 of the P4 register is set to 1).

3.9.2 Carry flag (CY)

The carry flag is set (to 1) in the following cases:

- If the ANL instruction or the XRL instruction is executed when bit 3 of the accumulator is 1 and bit 3 of the operand is 1.
- If the RL instruction or the RLZ instruction is executed when bit 3 of the accumulator is 1.
- If the INC instruction or the SCAF instruction is executed when the value of the accumulator is 0FH.

The carry flag is cleared (to 0) in the following cases:

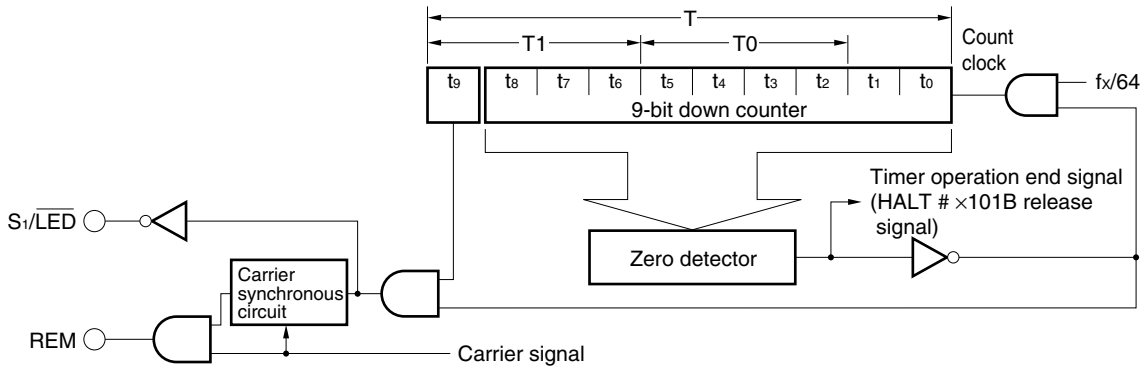
- If the ANL instruction or the XRL instruction is executed when at least either bit 3 of the accumulator or bit 3 of the operand is 0.
- If the RL instruction or the RLZ instruction is executed when bit 3 of the accumulator is 0.
- If the INC instruction or the SCAF instruction is executed when the value of the accumulator is other than 0FH.
- If the ORL instruction is executed.
- When data is written to the accumulator by the MOV instruction or the IN instruction.

★ 4. TIMER

4.1 Timer Configuration

The timer is the block used for creating a remote control transmission pattern. As shown in Figure 4-1, it consists of a 9-bit down counter (t_8 to t_0), a flag (t_9) permitting the 1-bit timer output, and a zero detector.

Figure 4-1. Timer Configuration



4.2 Timer Operation

The timer starts (counting down) when a value other than 0 is set for the down counter with a timer manipulation instruction. The timer manipulation instructions for making the timer start operation are shown below:

```
MOV T0, A
MOV T1, A
MOV T, #data10
MOV T, @R0
```

The down counter is decremented (–1) in the cycle of 64/fx. If the value of the down counter becomes 0, the zero detector generates the timer operation end signal to stop the timer operation. At this time, if the timer is in HALT mode (HALT #×101B) waiting for the timer to stop its operation, the HALT mode is released and the instruction following the HALT instruction is executed. The output of the timer operation end signal is continued while the down counter is 0 and the timer is stopped. The following relational expression applies between the timer's output time and the down counter's set value.

(a) μPD6P9M1
Timer output time = (Set value + 1) × 64/fx

(b) μPD6P9M3
Timer output time = (Set value + 0.5) × 64/fx

An example is shown below.

Example When fx = 4 MHz

```
MOV T, #3FFH
STTS #05H
HALT #05H
MOV T, #232H
STTS #05H
HALT #05H
```

In the case above, the timer output time is as follows.

(a) μPD6P9M1
(Set value + 1) × 64/fx + (Set value + 1) × 64/fx
= (511 + 1) × 64/4 + (50 + 1) × 64/4
= 9.008 ms

(b) μPD6P9M3
(Set value + 0.5) × 64/fx + (Set value + 0.5) × 64/fx
= (511 + 0.5) × 64/4 + (50 + 0.5) × 64/4
= 8.992 ms

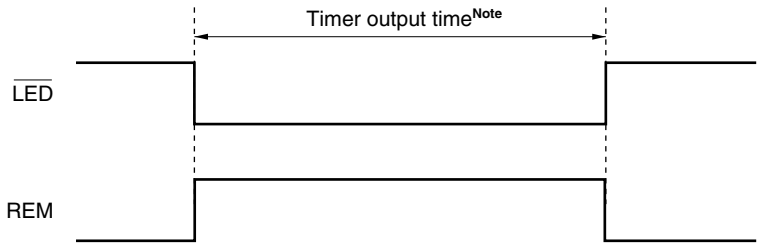
By setting the flag (t_9) that enables the timer output to 1, the timer can output its operation status from the S_1/LED pin and the REM pin. The REM pin can also output the carrier while the timer is in operation.

Table 4-1. Timer Output (at t_9 = 1)

	$S_1/\overline{LED}$ Pin	REM Pin
Timer operating	Low level	High level (or carrier output[Note])
Timer halting	High level	Low level

Note The carrier output results if bit 9 (CARY) of the high-level period setting modulo register (MOD1) is cleared (to 0).

Figure 4-2. Timer Output (When Carrier Is Not Output)



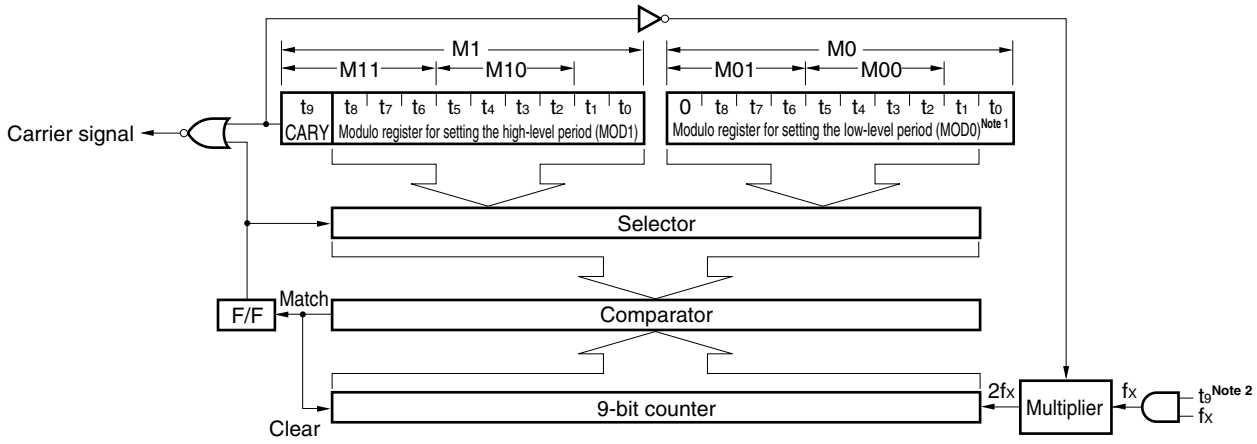
Note (Set value + 1) × 64/fx (μPD6P9M1), (set value + 0.5) × 64/fx (μPD6P9M3)

4.3 Carrier Output

4.3.1 Carrier output generator

The carrier generator consists of a 9-bit counter and two modulo registers for setting the high- and low-level periods (MOD1 and MOD0 respectively).

Figure 4-3. Configuration of Remote Controller Carrier Generator



Notes 1. Bit 9 of the modulo register for setting the low-level period (MOD0) is fixed to 0.

2. t_9: Flag that enables timer output (timer block) (see **Figure 4-1 Timer Configuration**)

The carrier duty ratio and carrier frequency can be determined by setting the high- and low-level widths using the respective modulo registers. Each of these widths can be set in a range of 250 ns to 64 μs (@ f_X = 4 MHz).

The system clock multiplied by 2 is used for the 9-bit counter input (8 MHz when f_X = 4 MHz). MOD0 and MOD1 are read and written using timer manipulation instructions.

MOV A, M00	MOV M00, A	MOV M0, #data10
MOV A, M01	MOV M01, A	MOV M1, #data10
MOV A, M10	MOV M10, A	MOV M0, @R0
MOV A, M11	MOV M11, A	MOV M1, @R0

The values of MOD0 and MOD1 can be calculated from the following expressions.

$$MOD0 = (2 \times f_X \times (1 - D) \times T) - 1$$
$$MOD1 = (2 \times f_X \times D \times T) - 1$$

Caution Be sure to input values in range of 001H to 1FFH to MOD0 and MOD1.

Remark D: Carrier duty ratio (0 < D < 1)
f_X: Input clock (MHz)
T: Carrier cycle (μs)

4.3.2 Carrier output control

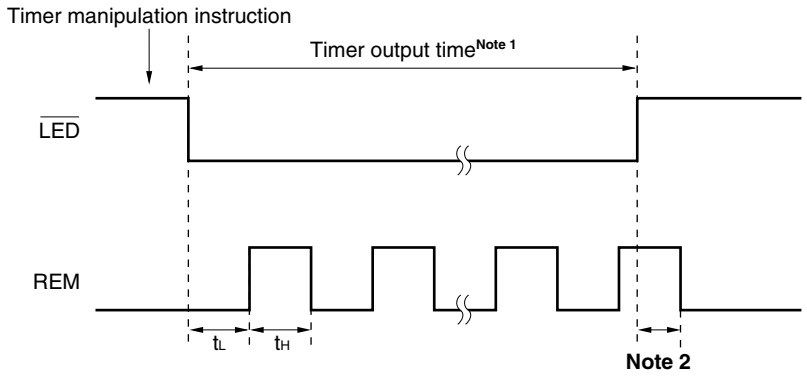
Remote controller carrier can be output from the REM pin by clearing (0) bit 9 (CARY) of the modulo register for setting the high-level period (MOD1).

When performing carrier output, be sure to set the timer operation after setting the MOD0 and MOD1 values. Note that a malfunction may occur if the values of MOD0 and MOD1 are changed while carrier is being output from the REM pin.

Executing the timer manipulation instruction starts the carrier output from the low level.

If the timer's down counter reaches 0 during carrier output, carrier output is stopped and the REM pin becomes low level. If the down counter reaches 0 while the carrier output is high level, carrier output will stop after first becoming low level following the set period of high level.

Figure 4-4. Timer Output (When Carrier Is Output)



Notes 1. (Set value + 1) × 64/fx (μPD6P9M1), (set value + 0.5) × 64/fx (μPD6P9M3)

2. If the down counter reaches 0 while the carrier output is high level, carrier output will stop after becoming low level.

Output from the REM pin is as follows, in accordance with the values set to bit 9 (CARY) of MOD1 and the timer output enable flag (t_9), and the value of the timer block's 9-bit down counter (t_0 to t_8).

Table 4-2. REM Pin Output

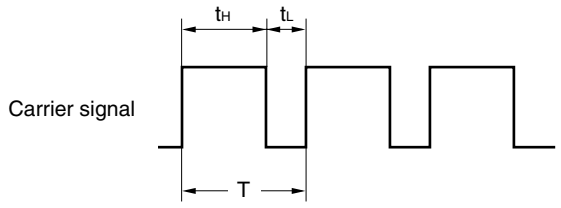
MOD1 Bit 9 (CARY)	Timer Output Enable Flag (Timer Block t_9)	9-Bit Down Counter (Timer Block t_0 to t_8)	REM Pin
—	—	0	Low-level output
—	0	Other than 0	
0	1		Carrier output[Note]
1			High-level output

Note Input values in the range of 001H to 1FFH to MOD0 and MOD1.

Caution MOD0 and MOD1 must be set while the REM pin is low level (t_9 = 0 or t_0 to t_8 = 0).

Table 4-3. Example of Carrier Frequency Settings (f_X = 4 MHz)

Setting Value		t_H (μs)	t_L (μs)	T (μs)	f_C (kHz)	Duty
MOD1	MOD0					
01H	01H	0.25	0.25	0.5	2,000	1/2
07H	0BH	1.0	1.5	2.5	400	2/5
13H	13H	2.5	2.5	5.0	200	1/2
27H	27H	5.0	5.0	10	100	1/2
41H	41H	8.25	8.25	16.5	60.6	1/2
41H	85H	8.25	16.75	25	40	1/3
45H	89H	8.75	17.25	26.0	38.5	1/3
45H	8BH	8.75	17.5	26.25	38.10	1/3
45H	8CH	8.75	17.625	26.375	37.9	1/3
47H	91H	9.0	18.25	27.25	36.7	1/3
48H	94H	9.125	18.625	27.75	36.0	1/3
69H	D5H	13.25	26.75	40.0	25	1/3
77H	77H	15.0	15.0	30.0	33.3	1/2
C7H	C7H	25.0	25.0	50.0	20	1/2
FFH	FFH	32.0	32.0	64.0	15.6	1/2

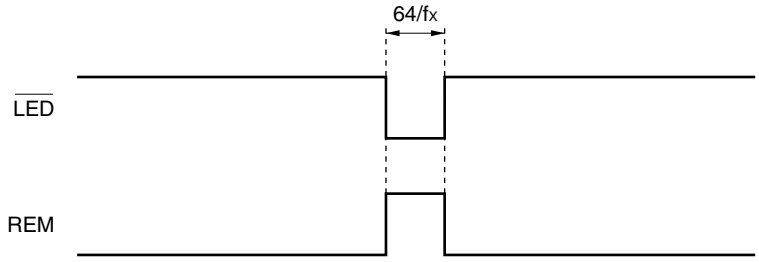


4.4 Software Control of Timer Output

The timer output can be controlled by software. As shown in Figure 4-5, a pulse with a minimum width of one instruction cycle 64/fx can be output.

Figure 4-5. Output of Pulse of 1-Instruction Cycle Width

```
      .
      .
      .
MOV   T, #0000000000B; low-level output from the REM pin
      .
      .
      .
MOV   T, #1000000000B; high-level output from the REM pin
MOV   T, #0000000000B; low-level output from the REM pin
      .
      .
      .
```



5. WRITING AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The program memory of the μPD6P9 is a one-time PROM of 4074 × 10 bits.

To write or verify this one-time PROM, the pins shown in Table 5-1 are used. Note that no address input pin is used. Instead, the address is updated by using the clock input from the CLK pin.

Table 5-1. Pins Used to Write/Verify Program Memory

Pin Name	Function
V_{PP}	Supplies voltage when writing/verifying program memory. Apply +12.5 V to this pin.
V_{DD}	Power supply. Supply +6 V to this pin when writing/verifying program memory.
CLK	Inputs clock to update address when writing/verifying program memory. By inputting a pulse four times to the CLK pin, the address of the program memory is updated.
MD_0 to MD_3	Input to select the operation mode when writing/verifying program memory.
D_0 to D_7	Inputs/outputs 8-bit data when writing/verifying program memory.
X_{IN}, X_{OUT}	Clock necessary for writing program memory. Connect a 4 MHz ceramic resonator to this pin.

5.1 Operating Mode When Writing/Verifying Program Memory

The μPD6P9 is set in the program memory write/verify mode when +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after the μPD6P9 has been in the reset status (V_{DD} = 5 V, V_{PP} = 0 V) for a specific time. In this mode, the operating modes shown in Table 5-2 can be set by setting the MD_0 through MD_3 pins. Connect all the pins other than those shown in Table 5-1 to GND via pull-down resistors.

Table 5-2. Setting Operating Mode

Setting of Operating Mode						Operating Mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Clear program memory address to 0
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

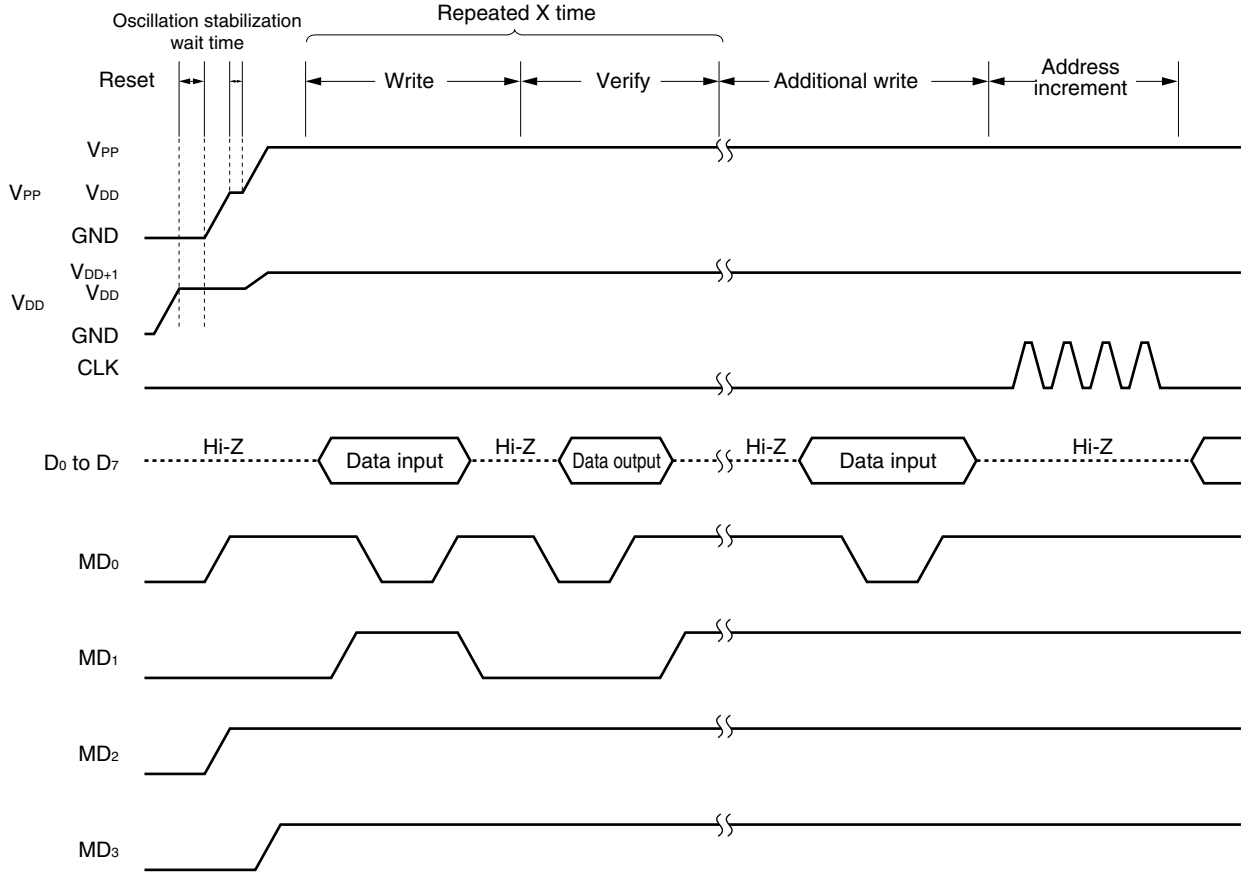
×: don't care (L or H)

5.2 Program Memory Writing Procedure

The program memory is written at high speed by the following procedure.

(1) Pull down the pins not used to GND via a resistor. Keep the CLK pin low.
(2) Supply 5 V to the V_{DD} pin. Keep the V_{PP} pin low.
(3) Supply 5 V to the V_{PP} pin after waiting for 10 μs.
(4) Wait for 2 ms until oscillation of the ceramic resonator connected across the X_{IN} and X_{OUT} pins stabilizes.
(5) Set the program memory address 0 clear mode by using the mode setting pins.
(6) Supply 6 V to V_{DD} and 12.5 V to V_{PP}.
(7) Set the program inhibit mode.
(8) Write data to the program memory in the 1 ms write mode.
(9) Set the program inhibit mode.
(10) Set the verify mode. If the data have been written to the program memory, proceed to (11). If not, repeat steps (8) through (10).
(11) Additional writing of (number of times of writing in (8) through (10): X) × 1 ms.
(12) Set the program inhibit mode.
(13) Input a pulse to the CLK pin four times to update the program memory address (+1).
(14) Repeat steps (8) through (13) up to the last address.
(15) Set the 0 clear mode of the program memory address.
(16) Change the voltages on the V_{DD} and V_{PP} pins to 5 V.
(17) Turn off the power.

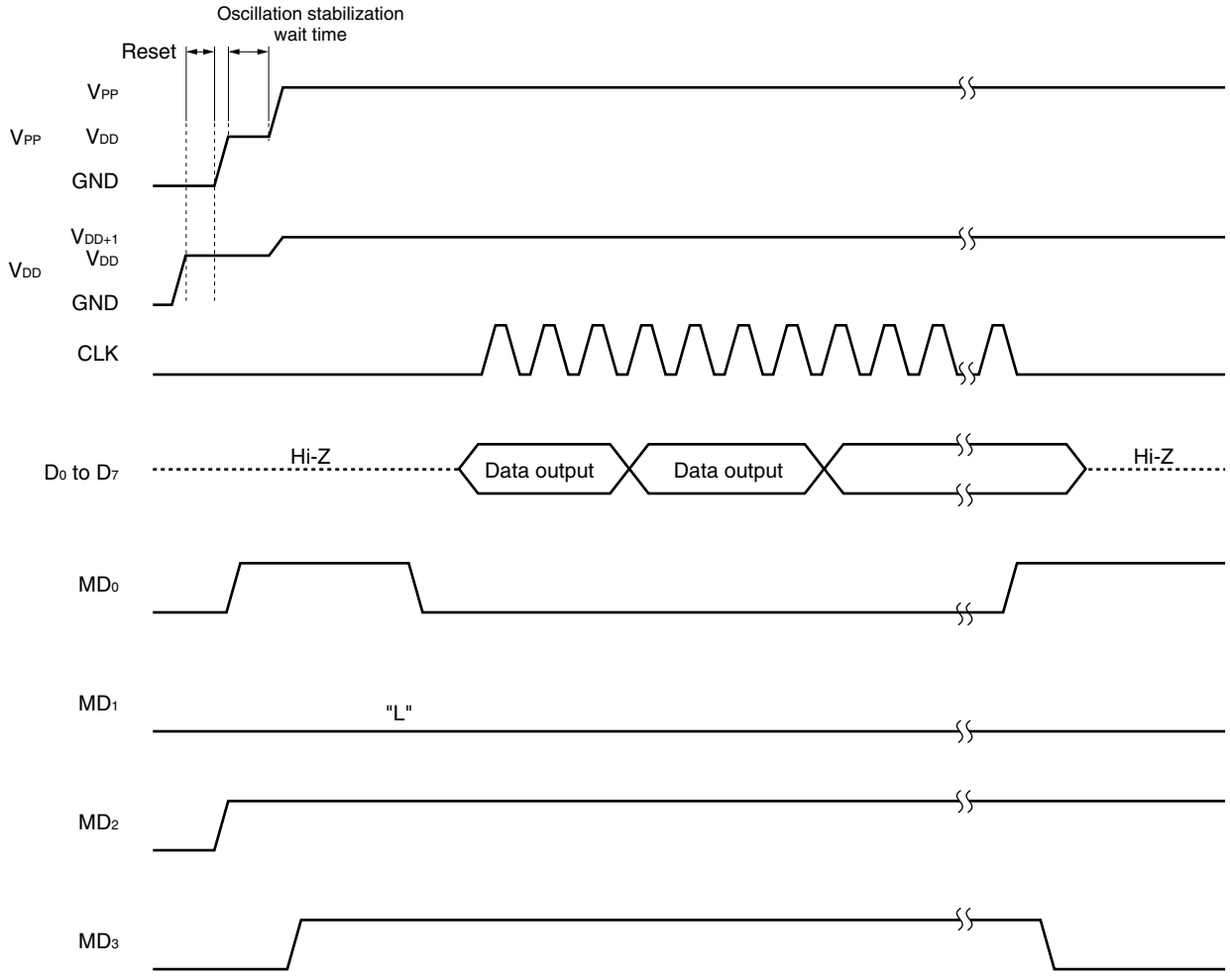
The following figure illustrates steps (2) through (13) above.



5.3 Program Memory Reading Procedure

(1) Pull down the pins not used to GND via a resistor. Keep the CLK pin low.
(2) Supply 5 V to the V_{DD} pin. Keep the V_{PP} pin low.
(3) Supply 5 V to the V_{PP} pin after waiting for 10 μs.
(4) Wait for 2 ms until oscillation of the ceramic resonator connected across the X_{IN} and X_{OUT} pins stabilizes.
(5) Set the program memory address 0 clear mode by using the mode setting pins.
(6) Supply 6 V to V_{DD} and 12.5 V to V_{PP}.
(7) Set the program inhibit mode.
(8) Set the verify mode. Data of each address is output sequentially each time the clock pulse is input to the CLK pin four times.
(9) Set the program inhibit mode.
(10) Set the program memory address 0 clear mode.
(11) Change the voltage on the V_{DD} and V_{PP} pins to 5 V.
(12) Turn off the power.

The following figure illustrates steps (2) through (10) above.



6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = +25°C)

Parameter	Symbol	Conditions		Rating	Unit
Power supply voltage	V_{DD}			–0.3 to +7.0	V
	V_{PP}			–0.3 to +13.5	V
Input voltage	V_I	$K_{I/O}$, K_I, S_0, S_1, S_2		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH} **Note**	REM	Peak value	–30	mA
			rms	–20	mA
		$\overline{LED}$	Peak value	–7.5	mA
			rms	–5	mA
		Per $K_{I/O}$ pin	Peak value	–13.5	mA
			rms	–9	mA
		Total for $\overline{LED}$ and $K_{I/O}$ pins	Peak value	–18	mA
			rms	–12	mA
Output current, low	I_{OL} **Note**	REM	Peak value	7.5	mA
			rms	5	mA
		$\overline{LED}$	Peak value	7.5	mA
			rms	5	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note Calculate the rms with: [rms] = [Peak value] × $\sqrt{\text{Duty}}$.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Power Supply Voltage Range (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	f_X = 3.5 to 4.5 MHz	2.2	3.0	3.6	V

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.2 to 3.6 V)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	$K_{I/O}$		0.7V_{DD}		V_{DD}	V
	V_{IH2}	K_I, S_0, S_1, S_2		0.65V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	$K_{I/O}$		0		0.3V_{DD}	V
	V_{IL2}	K_I, S_0, S_1, S_2		0		0.15V_{DD}	V
Input leakage current, high	I_{LIH1}	K_I $V_I = V_{DD}$, pull-down resistor not incorporated				3	μA
	I_{LIH2}	S_0, S_1, S_2 $V_I = V_{DD}$, pull-down resistor not incorporated				3	μA
Input leakage current, low	I_{LIL1}	K_I V_I = 0 V				–3	μA
	I_{LIL2}	$K_{I/O}$ V_I = 0 V				–3	μA
	I_{LIL3}	S_0, S_1, S_2 V_I = 0 V				–3	μA
Output voltage, high	V_{OH1}	REM, $\overline{LED}$, $K_{I/O}$	I_{OH} = –0.3 mA	0.8V_{DD}			V
Output voltage, low	V_{OL1}	REM, $\overline{LED}$	I_{OL} = 0.3 mA			0.3	V
	V_{OL2}	$K_{I/O}$	I_{OL} = 15 μA			0.4	V
Output current, high	I_{OH1}	REM	V_{DD} = 3.0 V, V_{OH} = 1.0 V	–5	–9		mA
	I_{OH2}	$K_{I/O}$	V_{DD} = 3.0 V, V_{OH} = 2.2 V	–2.5	–5		mA
Output current, low	I_{OL1}	$K_{I/O}$	V_{DD} = 3.0 V, V_{OL} = 0.4 V	30	70		μA
			V_{DD} = 3.0 V, V_{OL} = 2.2 V	100	220		μA
On-chip pull-down resistor	R_1	K_I, S_0, S_1, S_2		75	150	300	kΩ
	R_2	$K_{I/O}$		130	250	500	kΩ
Data retention power supply voltage	V_{DDOR}	In STOP mode		1.2		3.6	V
RAM retention detection voltage	V_{ID}				1.7	1.8	V
Supply current	I_{DD1}	Operation mode	f_X = 4.0 MHz, V_{DD} = 3 V ±10%		1.1	2.2	mA
	I_{DD2}	HALT mode	f_X = 4.0 MHz, V_{DD} = 3 V ±10%		1.0	2.0	mA
	I_{DD3}	STOP mode	V_{DD} = 3 V ±10%		2.2	9.5	μA
			V_{DD} = 3 V ±10%, T_A = 25°C		2.2	3.5	μA

AC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.2 to 3.6 V)

	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
★	Instruction execution time	t_{CY}	μPD6P9M1		14	16	18.5	μs
★			μPD6P9M3		7	8	9.25	μs
	K_I, S_0, S_1 high-level width	t_H			10			μs
			When releasing standby mode	In HALT mode	10			μs
				In STOP mode	**Note**			μs
	$\overline{RESET}$ low-level width	t_{RSL}			10			μs

★ **Note** 10 + 284/fx + oscillation growth time (μPD6P9M1), 10 + 270/fx + oscillation growth time (μPD6P9M3)

★ **Remark** t_{CY} = 64/fx (μPD6P9M1), t_{CY} = 32/fx (μPD6P9M3) (fx: System clock oscillation frequency)

POC Circuit (T_A = –40 to +85°C)

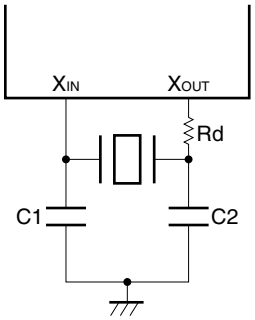
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
POC detection voltage[Note]	V_{POC}			2.0	2.2	V

Note Refers to the voltage with which the POC circuit releases an internal reset. If $V_{POC} < V_{DD}$, the internal reset is released.
From the time of $V_{POC} \geq V_{DD}$ until the internal reset takes effect, lag of up to 1 ms occurs. When the period of $V_{POC} \geq V_{DD}$ lasts less than 1 ms, the internal reset may not take effect.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.2 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency (ceramic resonator)	fx		3.5	4.0	4.5	MHz

★ **External circuit example**



Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

PROM Programming Mode

DC programming characteristics (T_A = 25°C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Other than CLK	$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	CLK	V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	Other than CLK	0		$0.3V_{DD}$	V
	V_{IL2}	CLK	0		0.4	V
Input leakage current	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
Output voltage, high	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Output voltage, low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	$MD_0 = V_{IL}$, $MD_1 = V_{IH}$			30	mA

Cautions 1. Keep V_{PP} to within +13.5 V including overshoot.

2. Apply V_{DD} before V_{PP} and turns it off after V_{PP}.

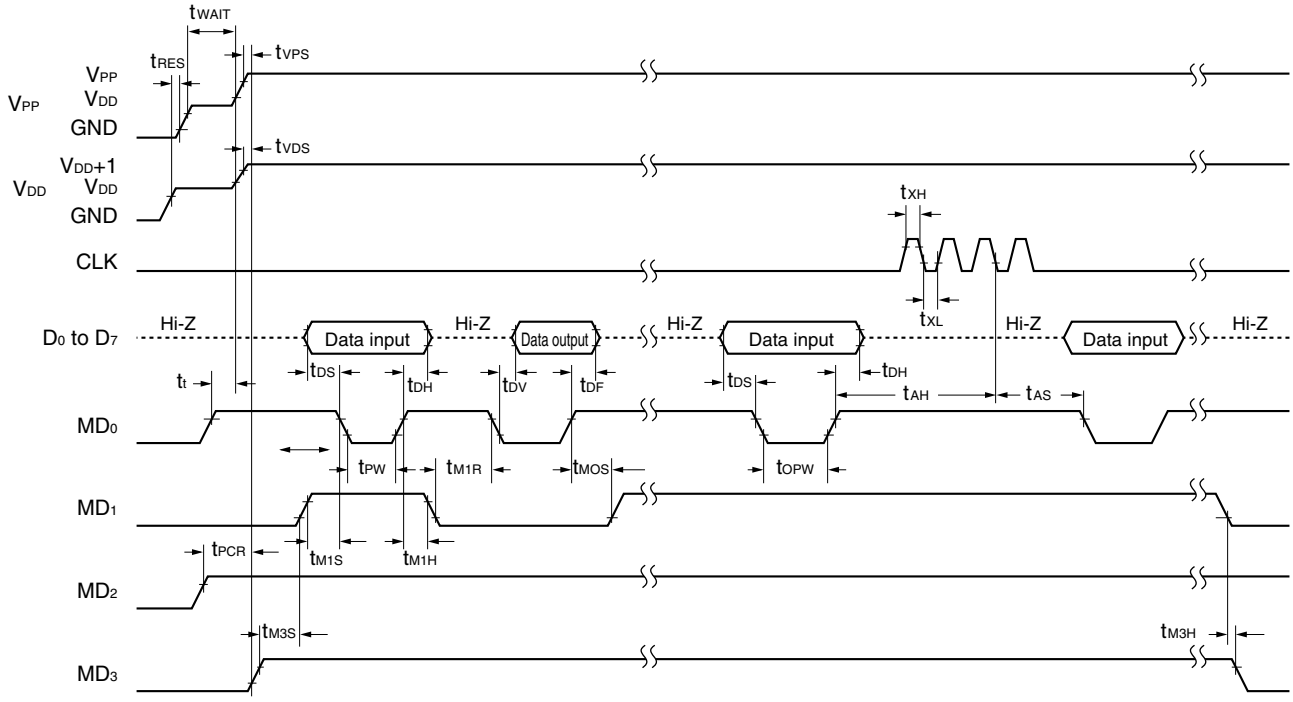
AC programming characteristics (T_A = 25°C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time[Note 1] (to MD_0↓)	t_{AS}		2			μs
MD_1 setup time (to MD_0↓)	t_{M1S}		2			μs
Data setup time (to MD_0↓)	t_{DS}		2			μs
Address hold time[Note 1] (from MD_0↑)	t_{AH}		2			μs
Data hold time (from MD_0↑)	t_{DH}		2			μs
Delay time from MD_0↑ to data output float	t_{DF}		0		130	ns
V_{PP} setup time (to MD_3↑)	t_{VPS}		2			μs
V_{DD} setup time (to MD_3↑)	t_{VDS}		2			μs
Initial program pulse width	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}		0.95		21.0	ms
MD_0 setup time (to MD_1↑)	t_{MOS}		2			μs
Delay time from MD_0↓ to data output	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD_1 hold time (from MD_0↑)	t_{M1H}	$t_{M1H}+t_{M1R} \geq 50$ μs	2			μs
MD_1 recovery time (to MD_0↓)	t_{M1R}		2			μs
Program counter reset time	t_{PCR}		10			μs
CLK input high-/low-level width	t_{XH}, t_{XL}		0.125			μs
CLK input frequency	f_X				4.19	MHz
Initial mode set time	t_I		2			μs
MD_3 setup time (to MD_1↑)	t_{M3S}		2			μs
MD_3 hold time (from MD_1↓)	t_{M3H}		2			μs
MD_3 setup time (to MD_0↓)	t_{M3SR}	When program memory is read	2			μs
Delay time from address[Note 1] to data output	t_{OAD}	When program memory is read			2	μs
Hold time from address[Note 1] to data output	t_{HAD}	When program memory is read	0		130	ns
MD_3 hold time (from MD_0↑)	t_{M3HR}	When program memory is read	2			μs
Delay time from MD_3↓ to data output float	t_{DFR}	When program memory is read			2	μs
Reset setup time	t_{RES}		10			μs
Oscillation stabilization wait time[Note 2]	t_{WAIT}		2			ms

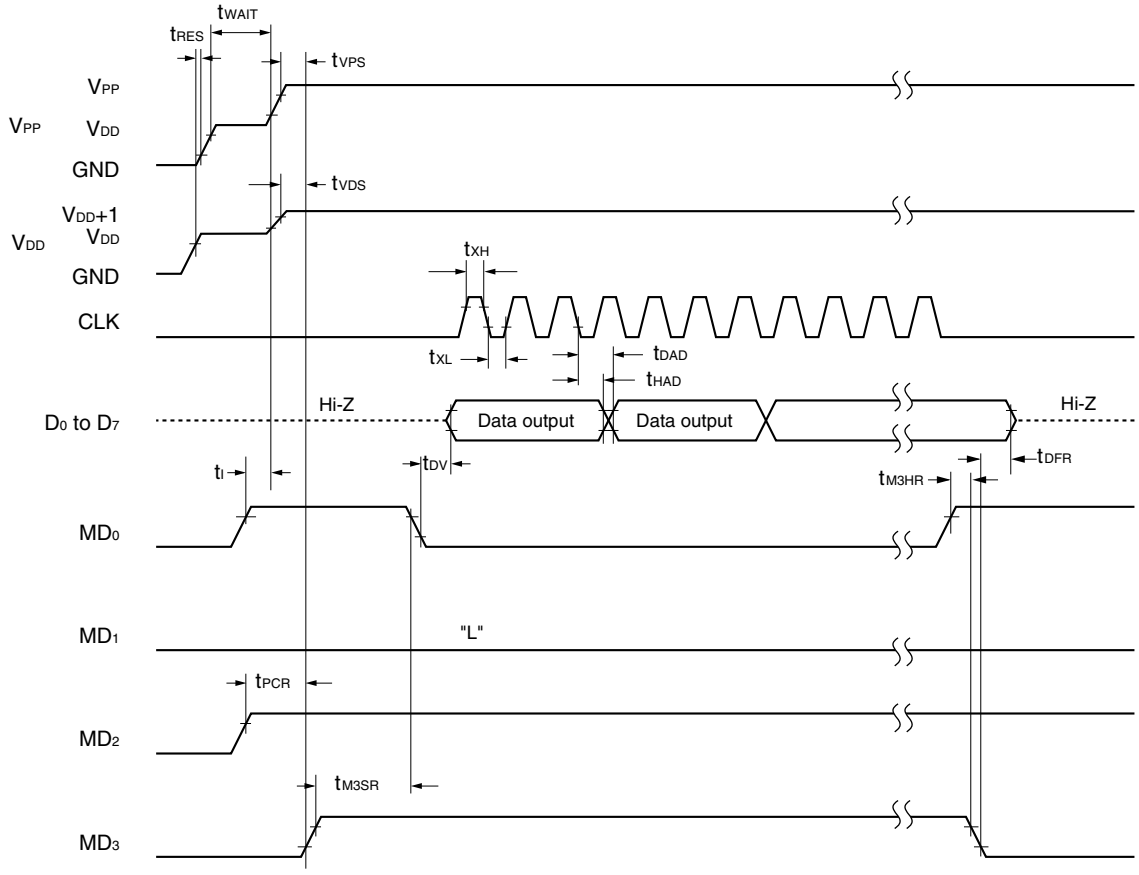
Notes 1. The internal address signal is incremented at the falling edge of the third clock of CLK.

2. Connect a 4 MHz ceramic resonator between the X_{IN} and X_{OUT} pins.

Program Memory Write Timing

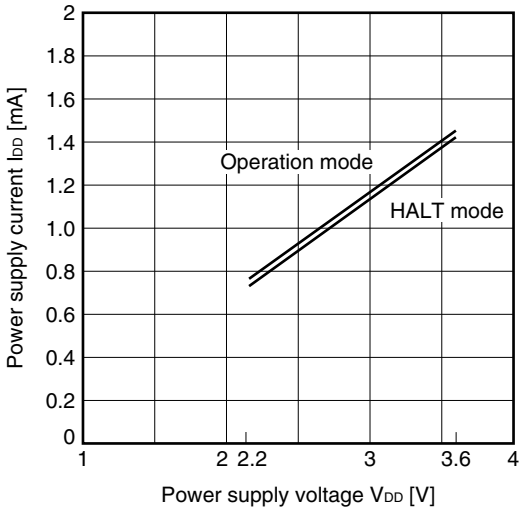


Program Memory Read Timing

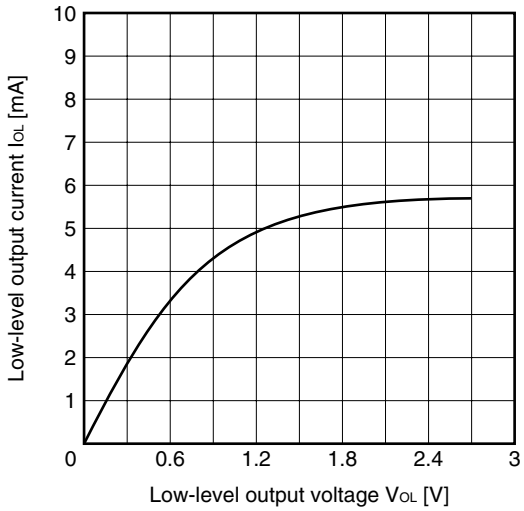


7. CHARACTERISTIC CURVES (REFERENCE VALUES) (μPD6P9M1)

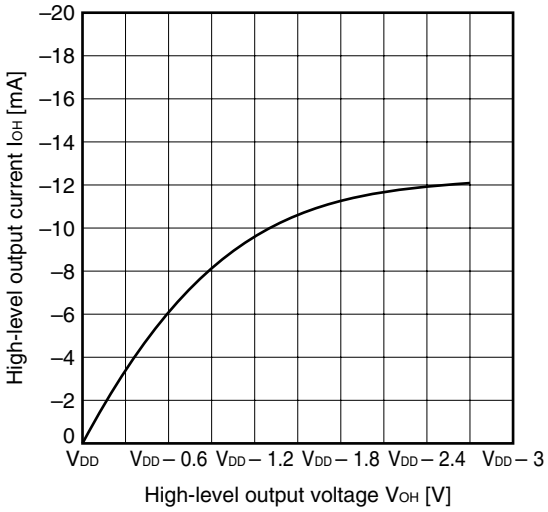
I_{DD} vs V_{DD} (f_X = 4 MHz)
(T_A = 25°C)



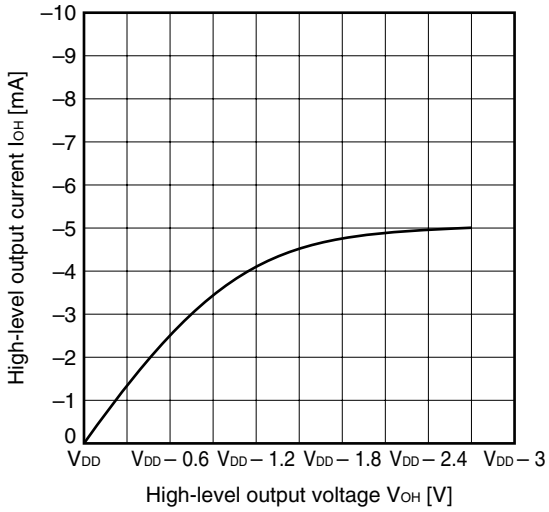
I_{OL} vs V_{OL} (REM, $\overline{LED}$)
(T_A = 25°C, V_{DD} = 3.0 V)



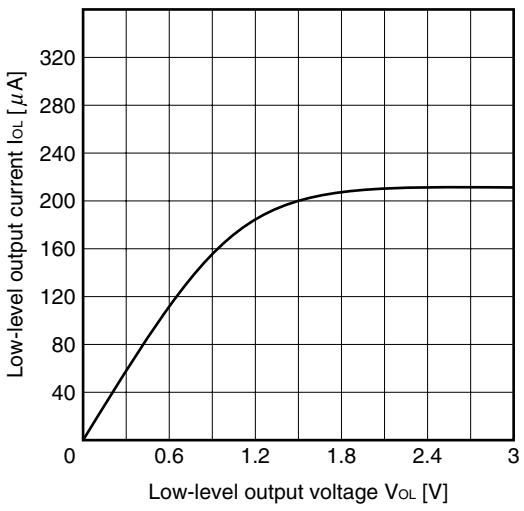
I_{OH} vs V_{OH} (REM)
(T_A = 25°C , V_{DD} = 3.0 V)



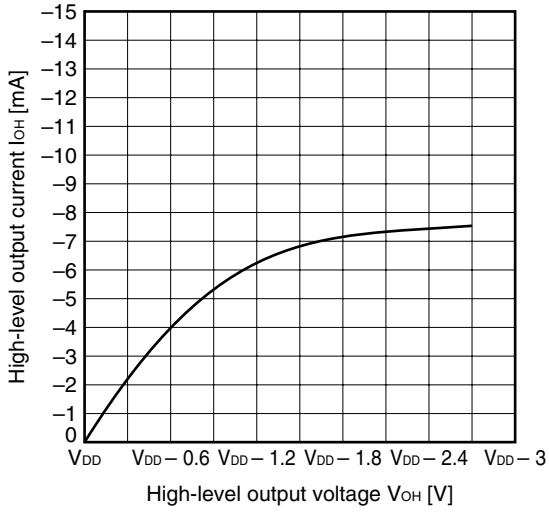
I_{OH} vs V_{OH} ($\overline{LED}$)
(T_A = 25°C , V_{DD} = 3.0 V)



I_{OL} vs V_{OL} ($K_{I/O}$)
(T_A = 25°C, V_{DD} = 3.0 V)



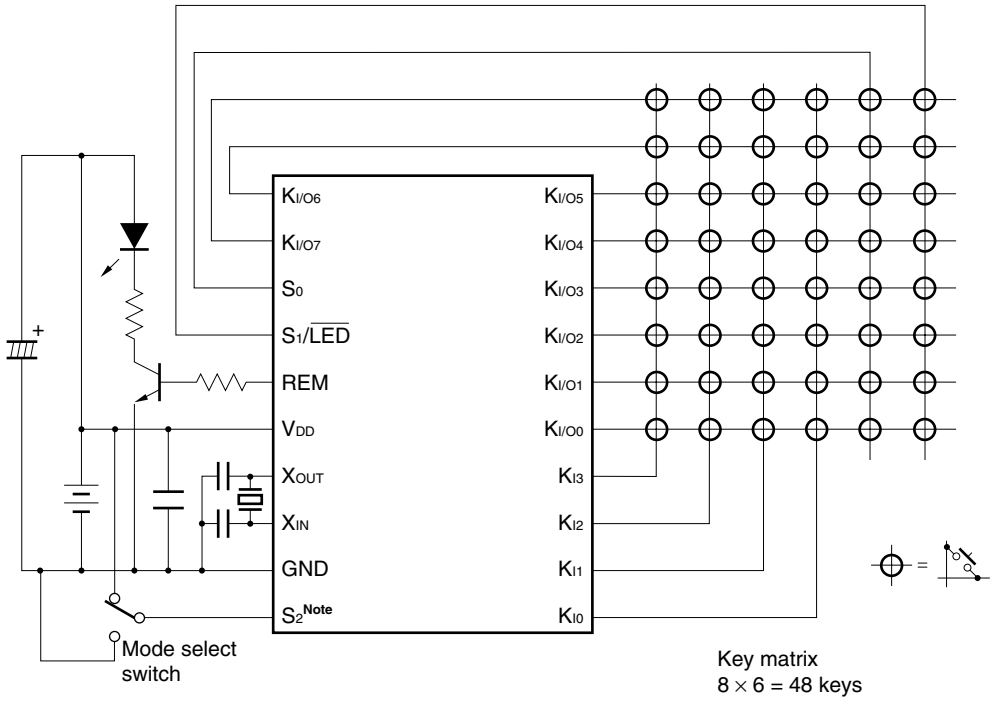
I_{OH} vs V_{OH} ($K_{I/O}$)
(T_A = 25°C, V_{DD} = 3.0 V)



8. APPLICATION CIRCUIT EXAMPLE

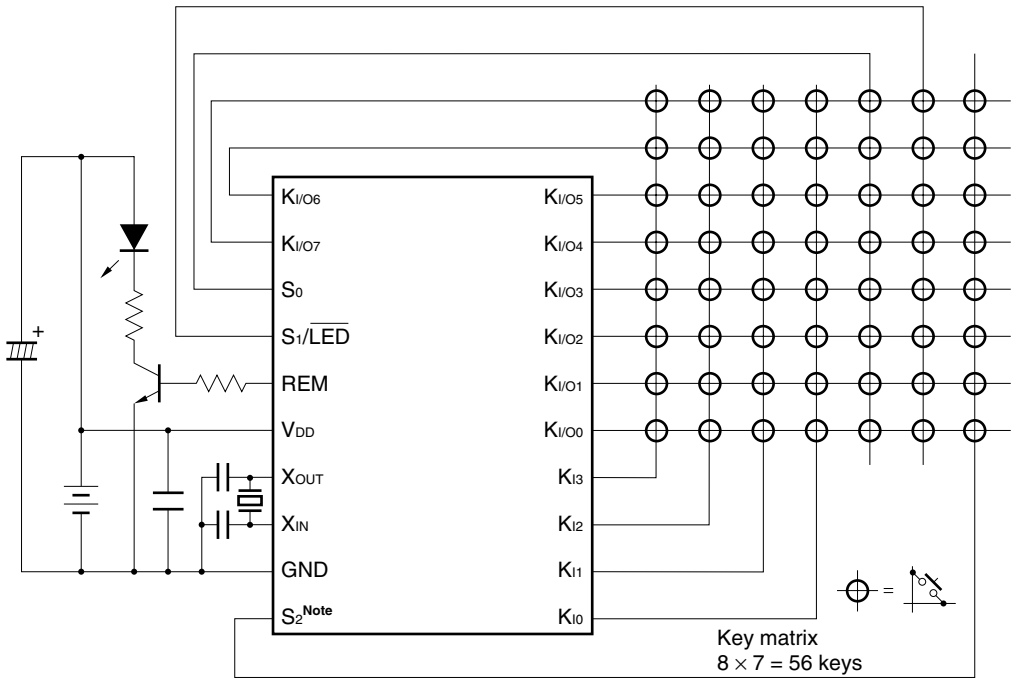
Example of Application to System

- **Remote-control transmitter (48 keys accommodated, mode selection switch accommodated)**



Note S_2: Set to STOP mode release disabled

- **Remote-control transmitter (56 keys accommodated)**

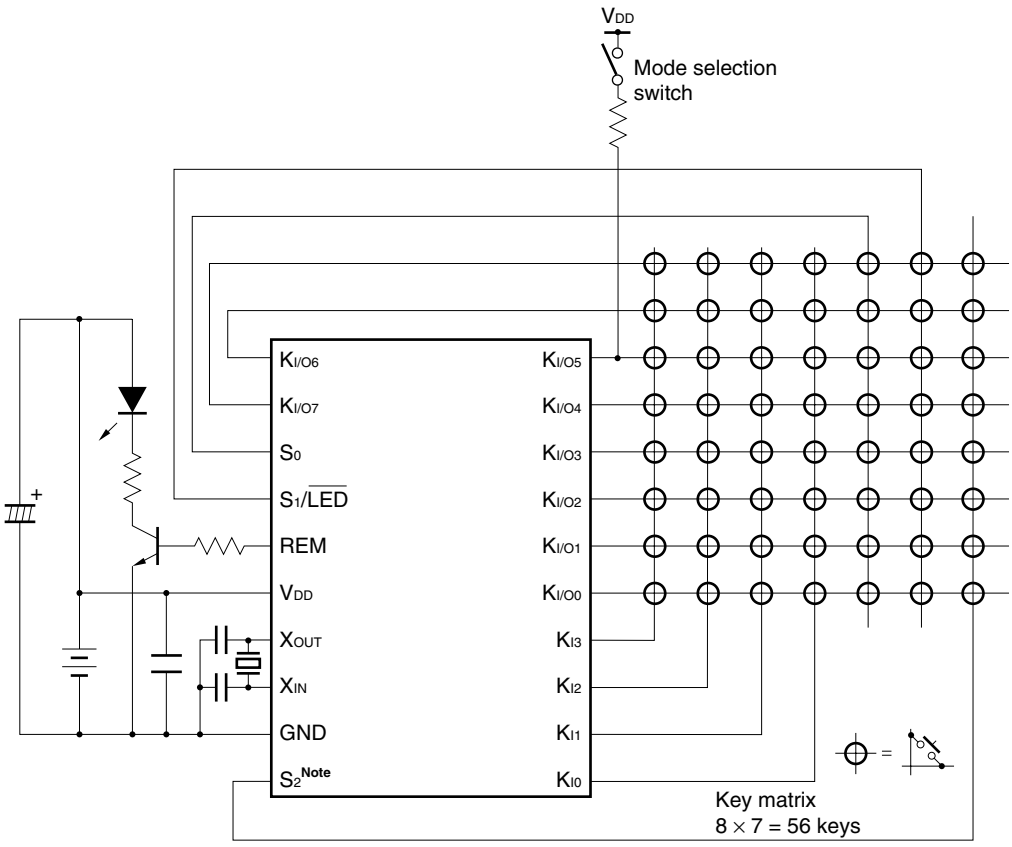


Note S_2: Set to STOP mode release enabled

- **Remote-control transmitter (56 keys accommodated, mode selection switch accommodated)**

  Data can be read from the $K_{I/O0}$ to $K_{I/O7}$ pins by connecting a pull-up resistor of approx. 50 kΩ and a switch to these pins (which then become high level when the switch is on and low level when off). Set the $K_{I/O0}$ to $K_{I/O7}$ pins to input mode at this time. Reading data from these pins enables multiple output data to be obtained for the same key input.

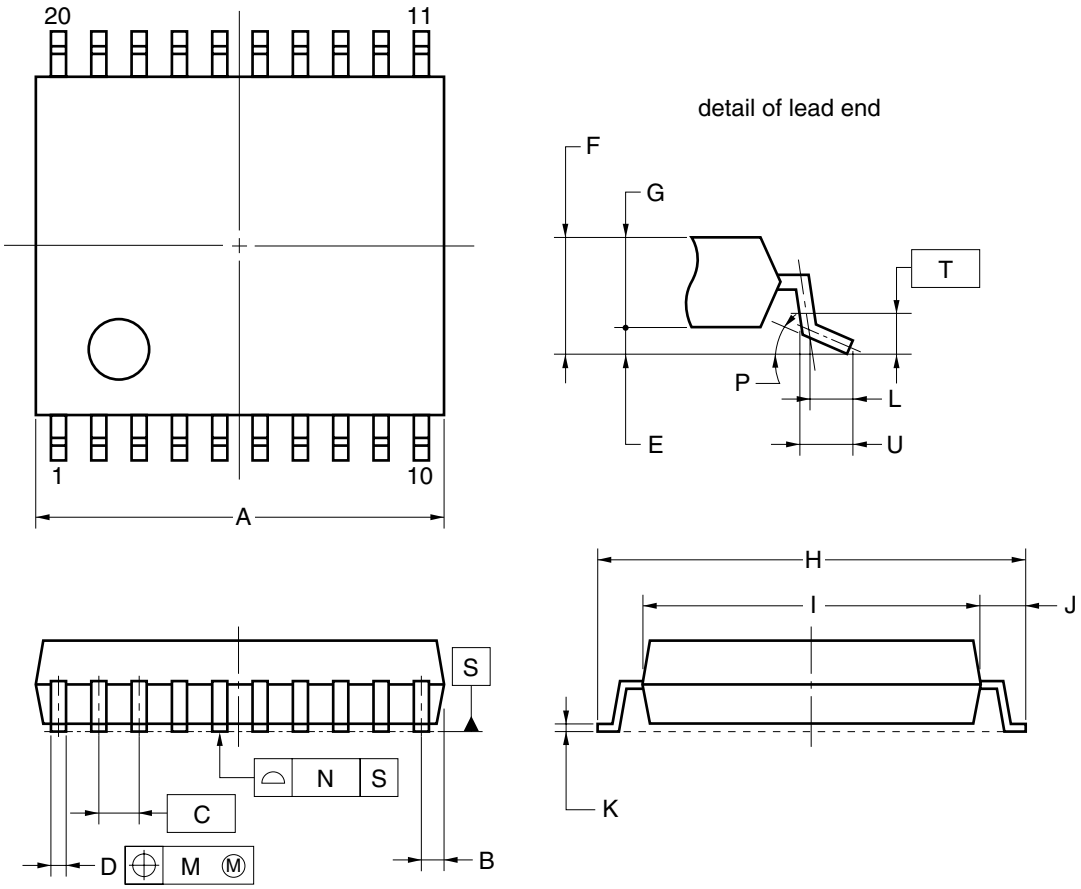
  A pull-up resistor can be connected to any of pins $K_{I/O0}$ to $K_{I/O7}$ (the figure below shows an example of when a pull-up resistor is connected to the $K_{I/O5}$ pin).



Note S_2: Set to STOP mode release enabled

9. PACKAGE DRAWING

20-PIN PLASTIC SSOP (7.62 mm (300))



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	6.65±0.15
B	0.475 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25
U	0.6±0.15

S20MC-65-5A4-2

★ 10. RECOMMENDED SOLDERING CONDITIONS

The μPD6P9 must be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

Table 10-1. Surface Mounting Soldering Conditions

μPD6P9M1MC-5A4: 20-pin plastic SSOP (7.62 mm (300))
μPD6P9M3MC-5A4: 20-pin plastic SSOP (7.62 mm (300))

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrated reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-103-2
Wave soldering	Solder bath temperature: 260°C max, Time: 10 seconds max., Count: once, preheating temperature: 120°C max. (package surface temperature) Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	WS60-103-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

A PROM programmer, program adapter, and an emulator are provided for the μPD6P9.

Hardware

- **PROM programmer (AF-9706[Note], AF-9708[Note], AF-9709[Note])**
  These PROM programmers support the μPD6P9.
  By connecting a program adapter to this PROM programmer, the μPD6P9 can be programmed.

  Note These are products of Ando Electric Co., Ltd. For details, consult Ando Electric Co., Ltd. (TEL: +81-3-3733-1163).

- **Program adapter (PA-61P34BMC)**
  This is used to program the μPD6P9 in combination with the AF-9706, AF-9708, or AF-9709.

★ • **Emulator (EB-69[Note 1], EB-69A[Note 1, 2])**
  This is used to emulate the μPD6P9.
  Use the EB-69 for the μPD6P9M1, and the EB-69A for the μPD6P9M3.

  Notes 1. These are products of Naito Densei Machida Mfg. Co., Ltd. For details, contact Naito Densei Machida Mfg. Co., Ltd. (+81-45-475-4191).
  2. Under development

Software

- **Assembler (AS6133 Ver. 2.22 or later)**
  This is a development tool for remote control transmitter software.

Part Number List of AS6133

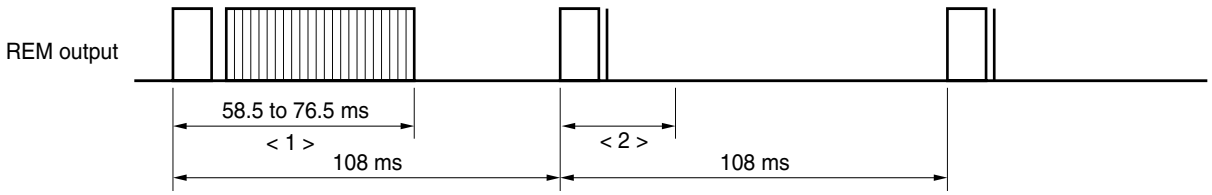
Host Machine	OS	Supply Medium	Part Number
PC-9800 series (CPU: 80386 or later)	MS-DOS™ (Ver. 5.0 to Ver. 6.2)	3.5-inch 2HD	μS5A13AS6133
IBM PC/AT™ compatible	MS-DOS (Ver. 6.0 to Ver. 6.22)	3.5-inch 2HC	μS7B13AS6133
	PC DOS™ (Ver. 6.1 to Ver. 6.3)		

Caution Although Ver.5.0 or later has a task swap function, this function cannot be used with this software.

APPENDIX B. EXAMPLE OF REMOTE CONTROL TRANSMISSION FORMAT
(In the case of NEC transmission format in command one-shot transmission mode)

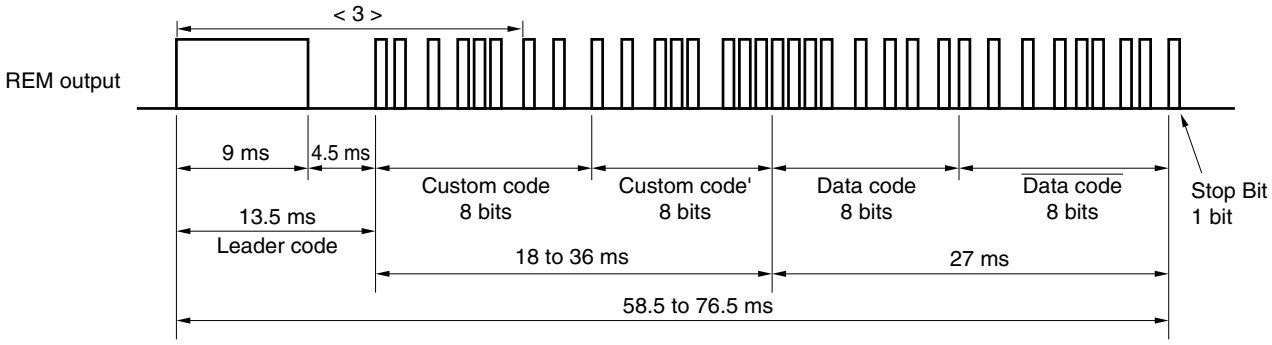
Caution When using the NEC transmission format, please apply for a custom code at NEC Electronics.

(1) REM output waveform (from <2> on, the output is made only when the key is kept pressed)

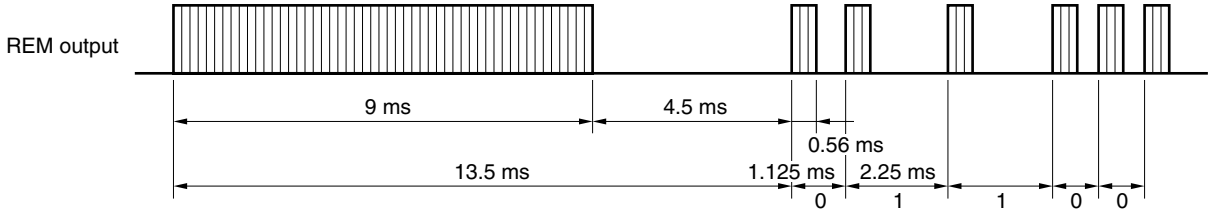


Remark If the key is repeatedly pressed, the power consumption of the infrared light-emitting diode (LED) can be reduced by sending the reader code and the stop bit from the second time.

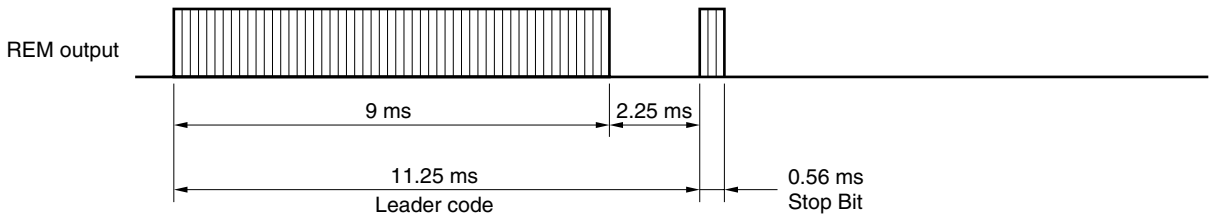
(2) Enlarged waveform of <1>



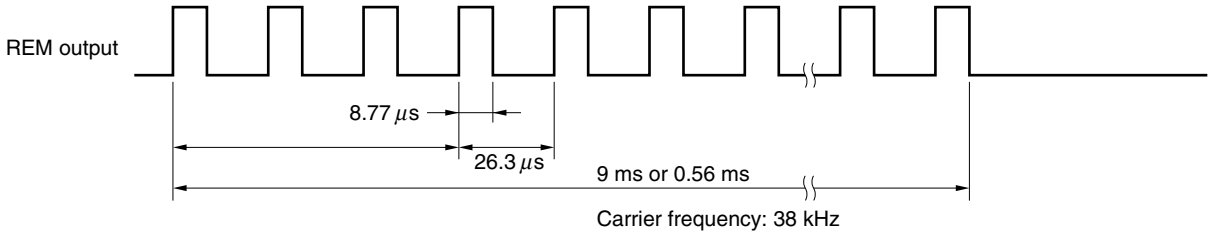
(3) Enlarged waveform of <3>



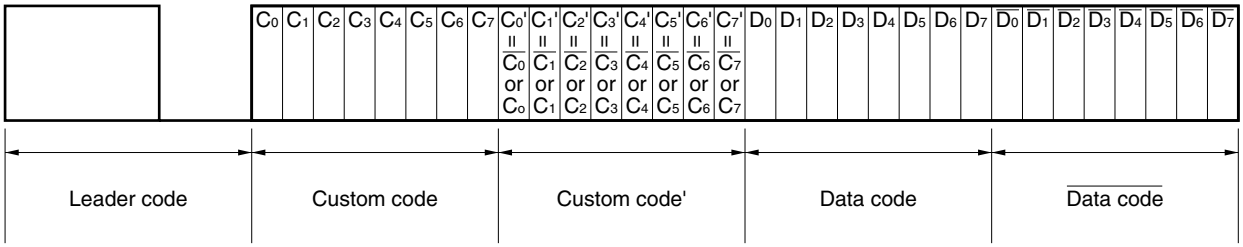
(4) Enlarged waveform of <2>



(5) Carrier waveform (enlarged waveform of each code's high period)



(6) Bit array of each code



Caution To prevent malfunction with other systems when receiving data in the NEC transmission format, not only fully decode (make sure to check $\overline{\text{Data Code}}$ as well) the total 32 bits of the 16-bit custom codes (Custom Code, Custom Code') and the 16-bit data codes (Data Code, $\overline{\text{Data Code}}$) but also check to make sure that no signals are present.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
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