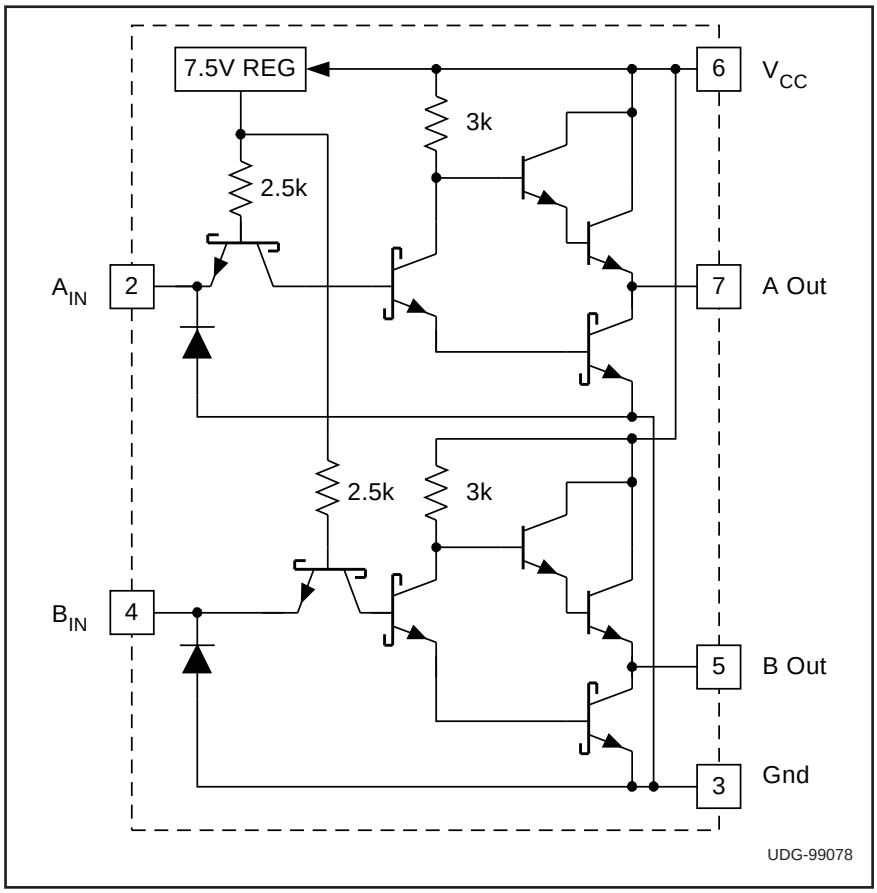
Dual Ultra High-Speed FET Driver

FEATURES

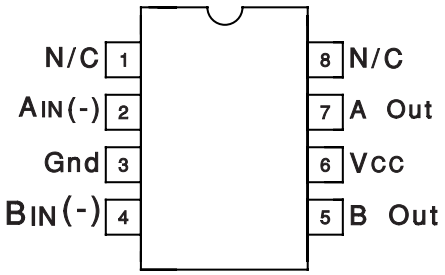
- 25ns Rise and Fall into 1000pF
- 15ns Propagation Delay
- 1.5A Source or Sink Output Drive
- Operation with 5V to 35V Supply
- High-Speed Schottky NPN Process
- 8-PIN MINIDIP Package

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-8 (Top View)
J or N Package



DESCRIPTION

The UC1711 family of FET drivers are made with an all-NPN Schottky process in order to optimize switching speed, temperature stability, and radiation resistance. The cost for these benefits is a quiescent supply current which varies with both output state and supply voltage. For lower power requirements, refer to the the UC1709 family which is both pin compatible with, and functionally equivalent to the UC1711.

These devices implement inverting logic with TTL compatible inputs, and output stages which will either source, or sink in excess of 1.5A of load current with minimal cross-conduction charge. Due to their monolithic construction, the channels are well matched and can be paralleled for doubled output current capability.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{CC} 40V
Output Current (Source or Sink)
  Steady State . . . . . ± 500mA
  Peak Transient . . . . . ± 1.5A
Maximum Forced Voltage . . . . . -0.3V to 7V
Maximum Forced Current . . . . . ± 10mA
Power Dissipation 1W
Operating Junction Temperature . . . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C

***Note 1**: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals. All reliability information for this device has been gathered at an ambient air temperature of 125°C, and a supply voltage of 25V.*

***Note 2:** Consult Unitrode databook for information regarding thermal specifications and limitations of packages.*

ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UC1711J	–55°C to +125°C	Ceramic DIP
UC3711J	0°C to +70°C	Ceramic DIP
UC3711N	0°C to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 15V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current (Note 3)	Both inputs = 0V; V_{CC} = 15V		11	15	mA
	Both inputs = 5V; $V_{CC= 15V}$		20	27	mA
	Both inputs = 0V; $V_{CC= 35V}$		15	20	mA
	Both inputs = 5V; $V_{CC= 35V}$		41	56	mA
Logic Inputs					
Logic 0 Input Voltage				0.8	V
Logic 1 Input Voltage		2.2			V
Input Current	V_{IN} = 0V	-5.0	-2.7		mA
	V_{IN} = 5V		0.5	2.0	mA
Output Stages					
Output High Level	I_{SOURCE} = 20mA, below V_{CC}		1.5	2.0	V
	I_{SOURCE} = 200mA, below V_{CC}		2.0	3.0	V
Output Low Level	I_{SINK} = 20mA		.25	0.4	V
	I_{SINK} = 200mA		0.4	1.0	V
Switching Characteristics (Note 4)					
Rise Time Delay, TPLH	C_{LOAD} = 0		10	40	ns
	C_{LOAD} = 1000pF, (Note 5)		15	50	ns
	C_{LOAD}= 2200pF		20	55	ns
Fall Time Delay, TPHL	C_{LOAD} = 0		3	20	ns
	C_{LOAD} = 1000pf, (Note 5)		5	20	ns
	C_{LOAD} = 2200pF		5	20	ns
Rise Time, TLH	C_{LOAD} = 0, (Note 5)		12	25	ns
	C_{LOAD} = 1000pF, (Note 5)		25	40	ns
	C_{LOAD} = 2200pF		40	55	ns
Fall Time, THL	C_{LOAD} = 0, (Note 5)		7	15	ns
	C_{LOAD} = 1000pF, (Note 5)		25	40	ns
	C_{LOAD}= 2200pF		40	55	ns
Total Supply Current	Freq = 200kHz, 50% Duty-cycle Both Channels Switching				
	C_{LOAD} = 0		17	23	mA
	C_{LOAD} = 2200pF		29	35	mA

Note 3: *Supply currents at other input supply votages can be calculated by extrapolating the 15V and 35V supply currents. The impedance of the chip at the V_{CC} pin is linear for supply voltages from 8V to 35V, the approximate value of this impedance is 4.3k for both inputs low, 0.94k for both inputs high, and 1.54k for one input high and one low.*

Note 4: *Switching test conditions are, V_{CC} = 15V, Input voltage waveform levels are 0V and 5V, with transition times of <3ns. The timing terms are defined as : TPHL Propagation delay 50% V_{IN} to 90% V_{OUT}; TPLH Propogation delay 50% V_{IN} to 10% V_{OUT}; THL 90% V_{OUT} to 10% V_{OUT}; TLH 10% V_{OUT} to 90% V_{OUT}.*

Note 5: *This specification not tested in production.Unless otherwise stated specifications hold for T_A = 0 to 70°C for the UC3711, and T_A = -55 to 125°C for the UC1711, V_{CC} = 15V. $T_A = T_J$.*

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UC1711J	OBSOLETE	CDIP	J	8		TBD	Call TI	Call TI	Add to cart
UC1711J883B	OBSOLETE	CDIP	J	8		TBD	Call TI	Call TI	Add to cart
UC1711JE	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Add to cart
UC1711JE883B	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Add to cart
UC1711L883B	OBSOLETE	TO/SOT	L	20		TBD	Call TI	Call TI	Add to cart
UC3711N	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	Add to cart
UC3711Q	OBSOLETE	PLCC	FN	20		TBD	Call TI	Call TI	Add to cart
UC3711QTR	OBSOLETE	PLCC	FN	20		TBD	Call TI	Call TI	Add to cart

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF UC1711, UC3711 :

- Catalog: UC3711
- Military: UC1711

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

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