UC1709, UC2709, UC3709
DUAL HIGH-SPEED FET DRIVER

SLUS196C – NOVEMBER 1996 – REVISED FEBRUARY 2008

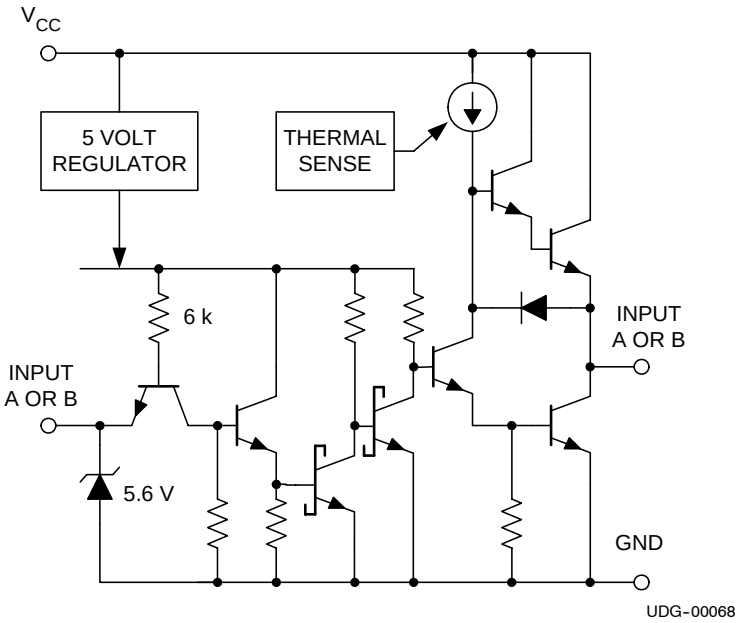
- **1.5 Amp Source/Sink Drive**
- **Pin Compatible with 0026 Products**
- **40 ns Rise and Fall into 1000pF**
- **Low Quiescent Current**
- **5 V to 40 V Operation**
- **Thermal Protection**

description

The UC3709 family of power drivers is an effective low-cost solution to the problem of providing fast turn-on and off for the capacitive gates of power MOSFETs. Made with a high-speed Schottky process, these devices will provide up to 1.5 A of either source or sink current from a totem–pole output stage configured for minimal cross-conduction current spike.

The UC3709 is pin compatible with the MMH0026 or DS0026, and while the delay times are longer, the supply current is much less than these older devices.

simplified schematic (only one driver shown)



With inverting logic, these units feature complete TTL compatibility at the inputs with an output stage that can swing over 30 V. This design also includes thermal shutdown protection.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡

Parameter	DW PACKAGE	J PACKAGE	L PACKAGE	N PACKAGE	UNIT
Supply Voltage, V_{CC}	40	40	40	40	V
Output Current (Source or Sink)					
. . . . . Steady–State	±500	±500	±500	±500	mA
. . . . . Peak Transient	±1.5	±1.0	±1.0	±1.5	A
. . . . . Capacitive Discharge Energy	20	15	15	20	mJ
Digital Inputs‡	5.5	5.5	5.5	5.5	V
Power Dissipation at T_A = 25°C	1	1	1	1	W
Power Dissipation at T_C = 25°C	3	2	2	3	W
Operating Junction Temperature Range (T_J)	–55 to 125	–55 to 125	–55 to 125	–55 to 125	°C
Storage Temperature Range	–65 to 150	–65 to 150	–65 to 150	–65 to 150	°C
Lead Temperature (Soldering, 10 Seconds)	300	300	300	300	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All currents are positive into and negative out of the specified terminals. Digital drive can exceed 5.5V if input is limited to 10mA. Consult the Packaging Section of the Databook for thermal limitations and considerations of the package.

THERMAL RESISTANCE TABLE

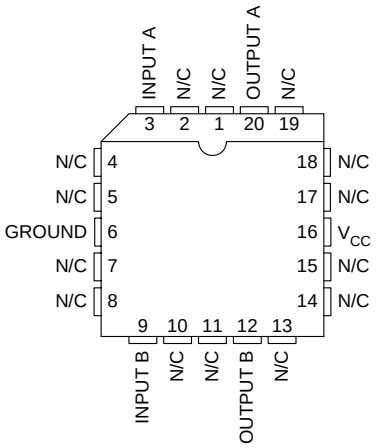
PACKAGE	θjc(°C/W)	θja(°C/W)
SOIC-16 (DW)	20 (1)	35 to 58 (3)
DIL-16 (J)	28 (2)	125 to 160
LCC-16 (L)	20 (2)	70 to 80
DIL-16 (N)	45	90 (3)

NOTES: (1) Specified thermal resistance is θjl (junction to lead)where noted.

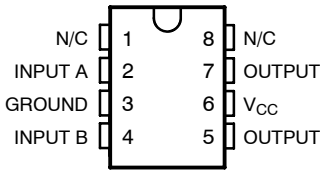
(2) θjc data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states, "The baseline values shown are worst case (mean +2s) for a 60x60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die sizes greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack, .10°C/W; pin grid array, 10°C/W".

(3) Specified θja (junction to ambient) is for devices mounted to 5-inch^2 FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 inch^2 aluminum PC board. Test PWB was 0.062 inch thick and typically used 0.635-mm trace widths for power packages and 1.3-mm trace widths for non-power packages with a 100-mil x 100-mil probe land area at the end of each trace.

LCC-20 (TOP VIEW)
L PACKAGES

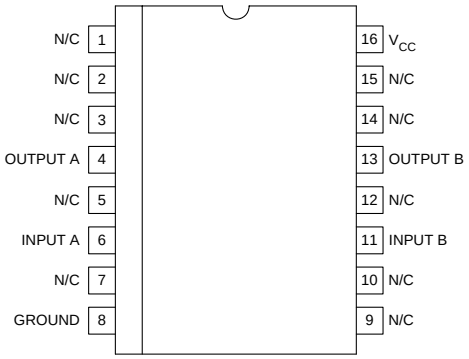


8 PIN DIL N OR J PACKAGE
(TOP VIEW)



N/C – No internal connection

SOIC-16 (TOP VIEW)
DW PACKAGE



electrical characteristics over recommended operating free-air temperature range, T_A = 55°C to 125°C for the UC1709, –40°C to 85°C for the UC2709, and 0°C to 70°C for the UC3709; V_{CC} = 20 V, T_A = T_J.

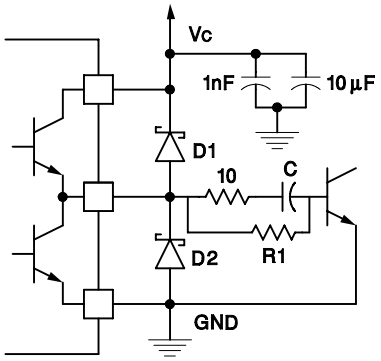
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current	Both outputs low		10	12	mA
	Both outputs high		7	10	mA
Logic 0 input voltage				0.8	V
Logic 1 input voltage		2.2			V
Input current	V_I = 0		–0.6	–1.0	mA
Input leakage	V_I = 5 V		0.05	0.1	mA
Output high saturation V_{CC}-V_O	I_O = –50 mA		1.5	2.0	V
	I_O = –500 mA		2.0	2.5	V
Output low saturation V_O	I_O = 50 mA		0.1	0.4	V
	I_O = 500 mA		2.0	2.5	V
Thermal shutdown			155		mA

typical switching characteristics, V_{CC} = 20 V, T_A = 25°C, delays measured to 10% output change

PARAMETER	TEST CONDITIONS	OUTPUT C_L =		UNITS
		0 nF	2.2 nF	
Rise time delay		80	80	ns
10% to 90% rise		20	40	ns
Fall time delay		60	80	ns
10% to 90% fall		20	40	ns
VCC cross-conduction curent spike duration	Output rise	25		ns
	Output fall	0		ns

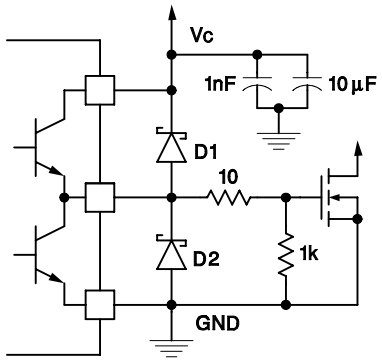
NOTE: Refer to UC1705 specifications for further information.

APPLICATION INFORMATION



D1, D2: UC3611 Schottky Diodes

Figure 1. Power bipolar drive circuit.



D1, D2: UC3611 Schottky Diodes

Figure 2. Power MOSFET drive circuit.

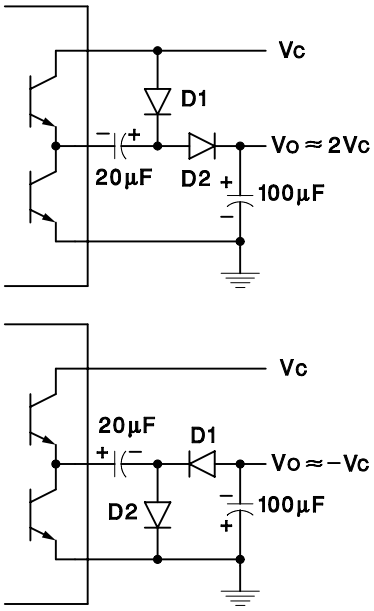
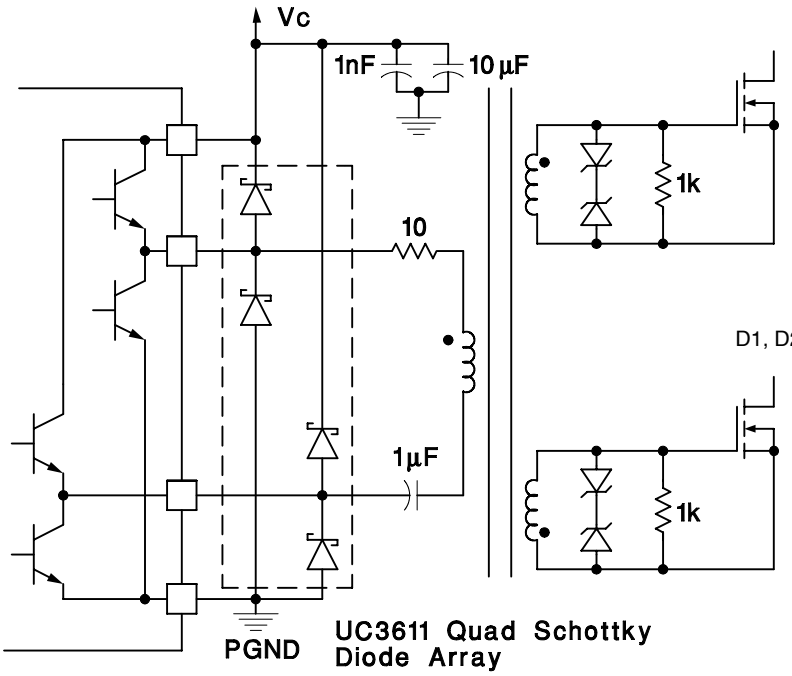
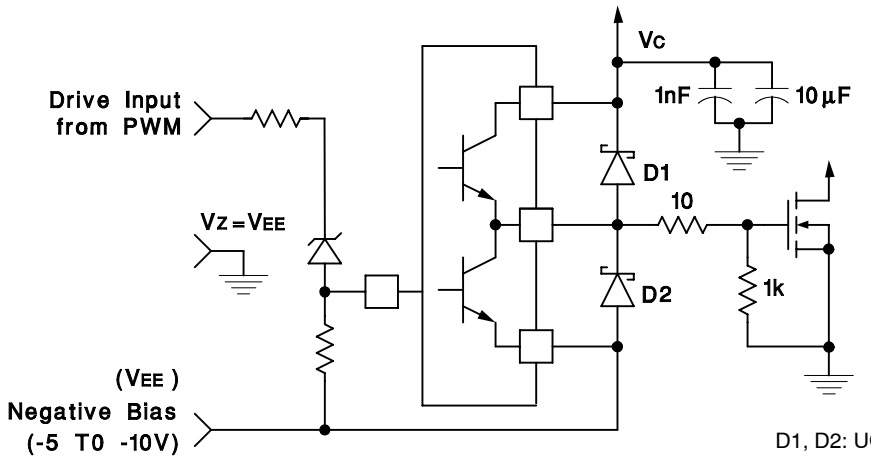


Figure 3. Charge pump circuits.



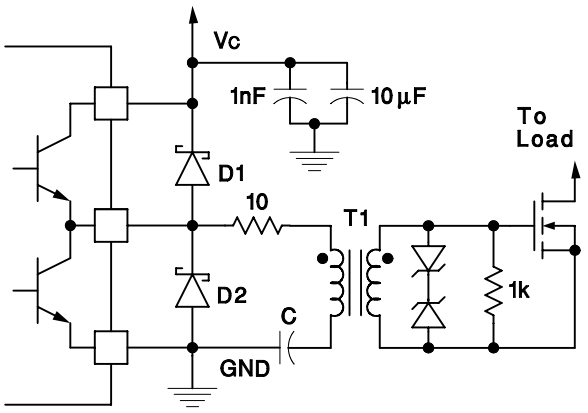
D1, D2: UC3611 Schottky Diodes

Figure 4. Transformer coupled push-pull MOSFET drive circuit.



D1, D2: UC3611 Schottky Diodes

Figure 5. Power MOSFET drive circuit using negative bias voltage and level shifting to ground referenced PWM



D1, D2: UC3611 Schottky Diodes

Figure 6. Transformer coupled MOSFET drive circuit.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-0151201VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1709J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1709J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1709L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC1709L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC2709DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2709DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2709N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2709NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3709DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3709DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3709N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3709NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

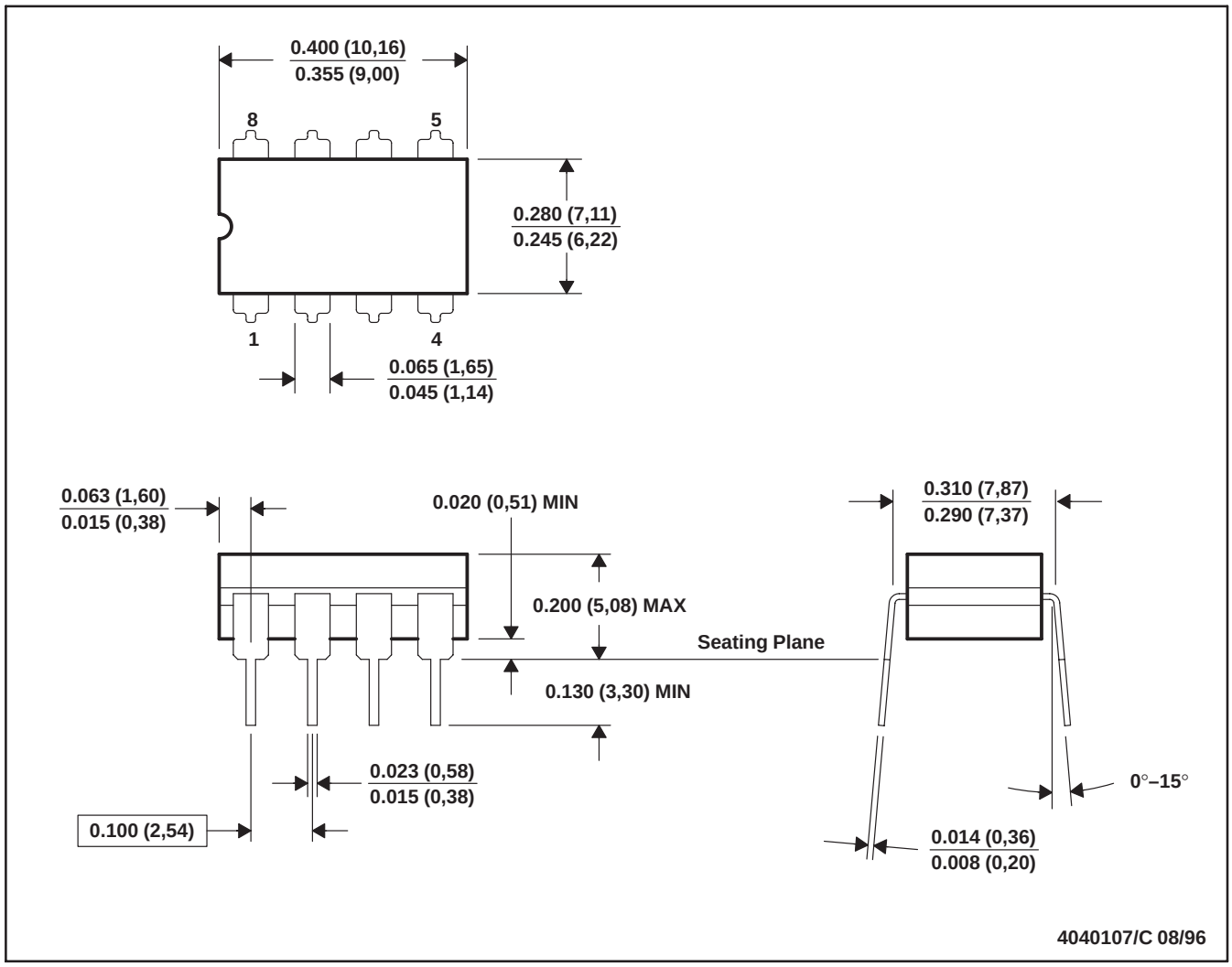
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

to Customer on an annual basis.

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

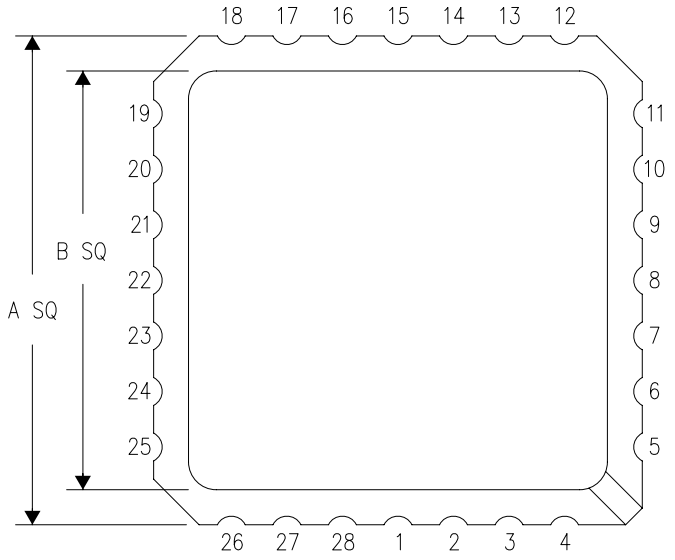
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



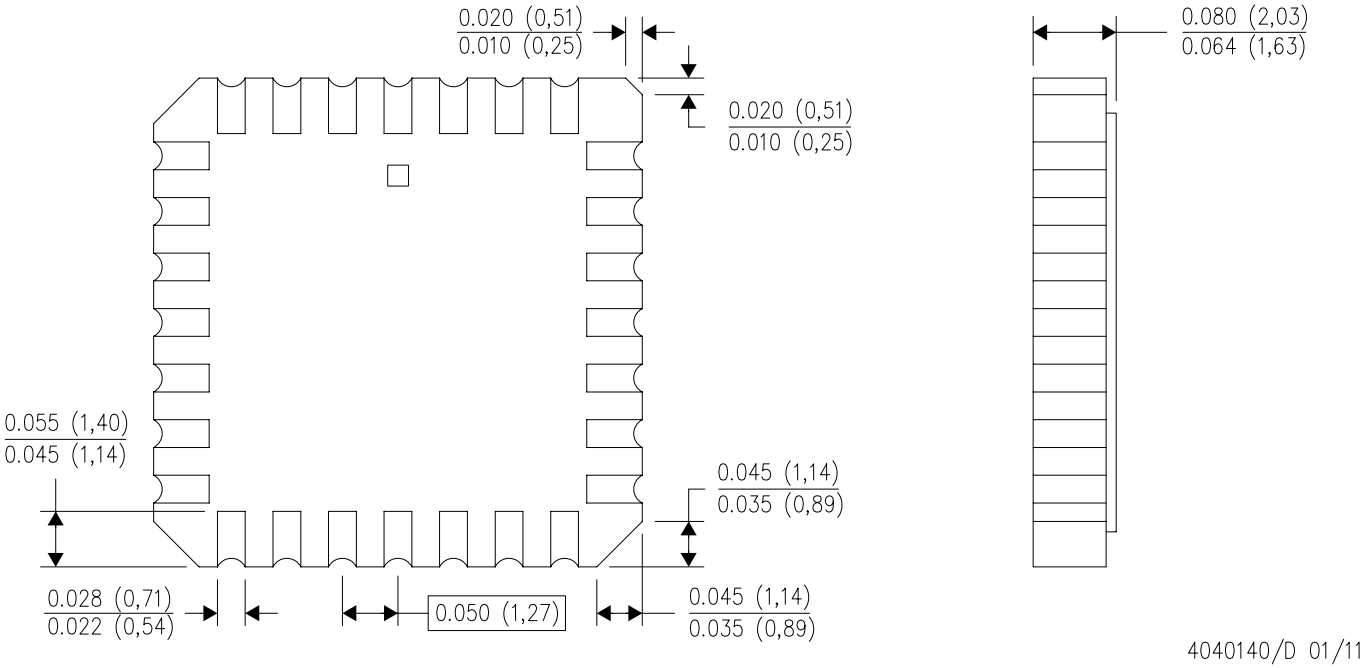
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



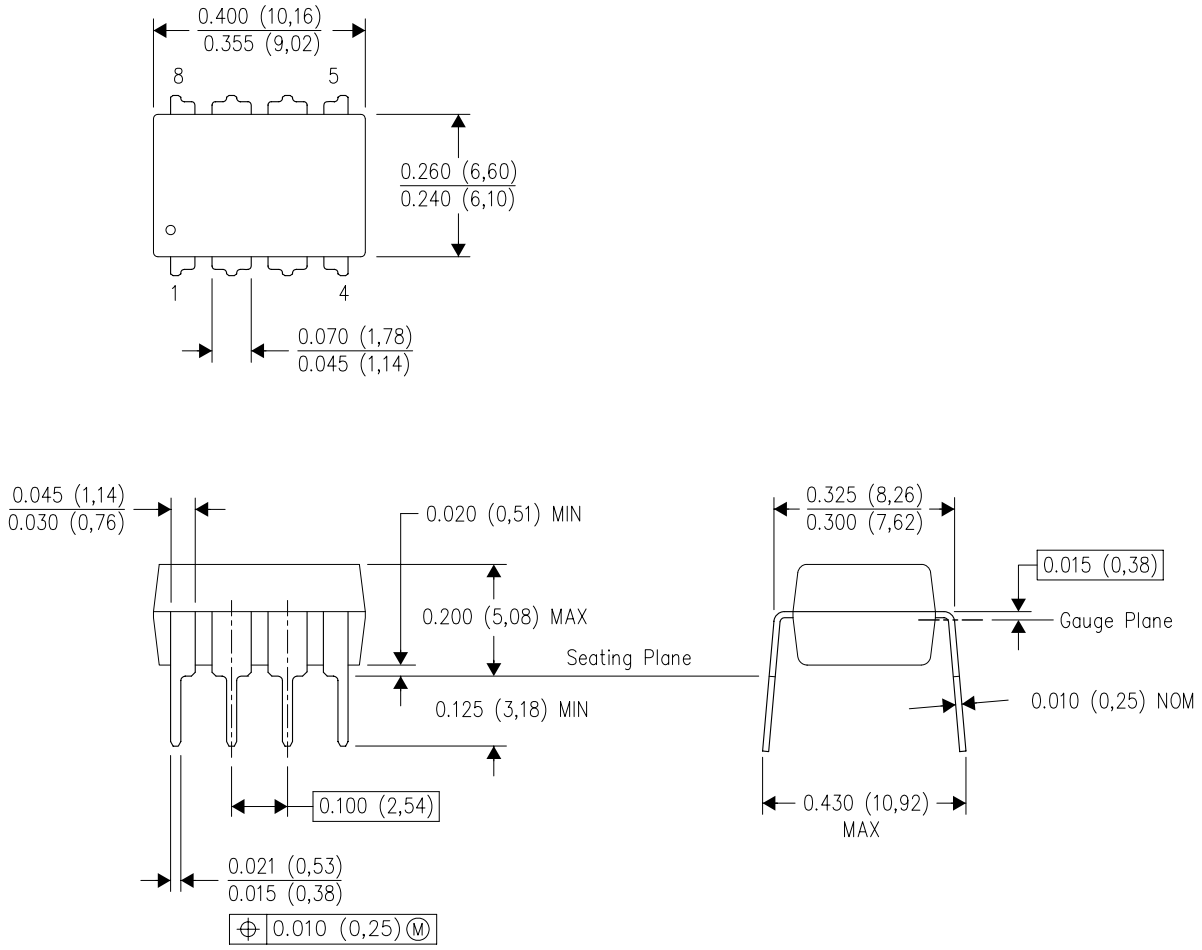
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

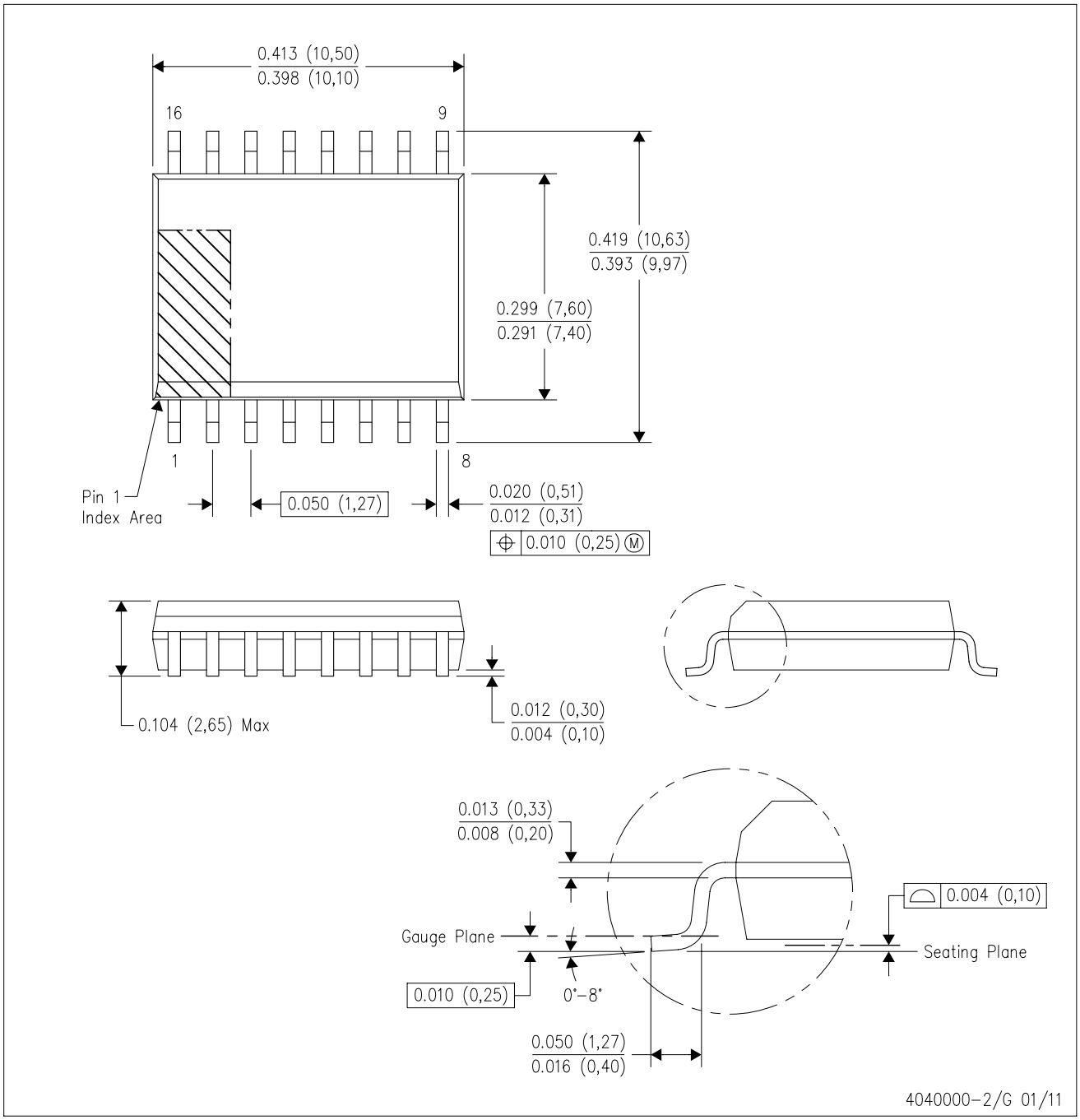
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



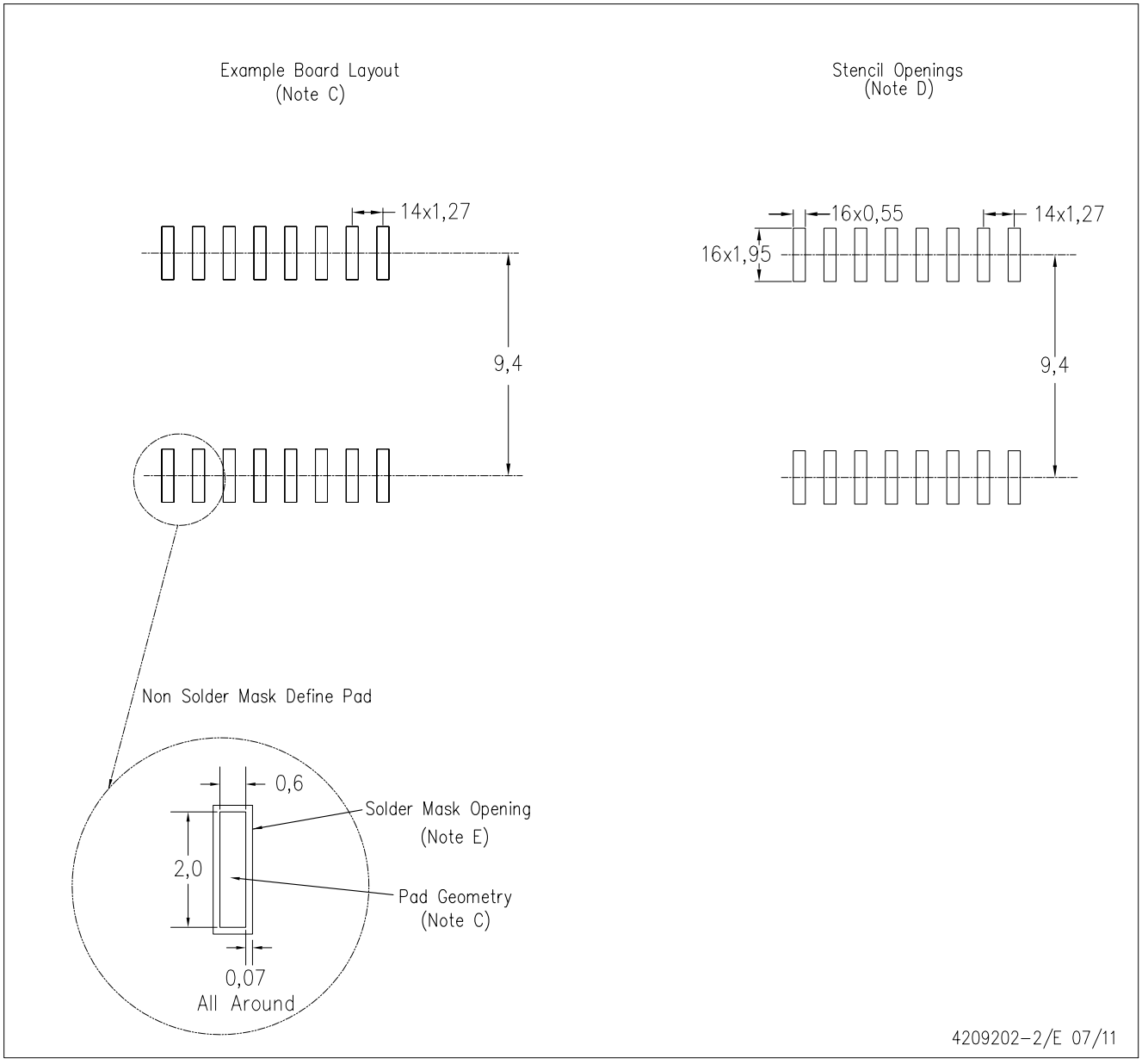
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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