National Semiconductor

μAV22 1200/600 bps Full Duplex Modem

General Description

The μAV22 1200/600 bps single-chip modem IC performs all signal processing required for a CCITT V.22 Alternative B-compatible modem, while typically dissipating only 40 mW. Handshaking protocols, and dialing and mode control functions can be serviced by a general purpose single chip microcontroller. These two chips, along with several components to handle the control and telephone line interfaces, provide a cost effective approach compared to either discrete or integrated chip set designs.

The modem chip performs the required V.22 modulation, demodulation, buffering, filtering, scrambling, descrambling and control and self-test functions, as well as additional functional enhancements. A novel switched capacitor modulator and a digital coherent demodulator provide 1200 bps and 600 bps QPSK operation. Switched-capacitor filters provide channel isolation, spectral shaping, fixed compromise equalization, and guard tone rejection. Additionally, the receive filter and energy detector may be configured for call-progress tone detection (dialtone, busy, ringback, voice) in the 350 Hz to 850 Hz band, providing the front end for a smart V.25-compatible dialer. On-chip tone generators provide DTMF dialing, 1300 Hz calling tone, 2100 Hz answer tone, and selectable 550 Hz and 1800 Hz guard tones. μAV22 also supports the Extended Signaling Rate Option (up to 2.3% overspeed in asychronous mode) and provides on-chip handshaking for Remote Digital Loop (V.54/Loop2).

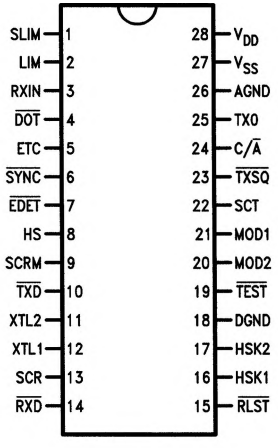
The μAV22 is fabricated in Double-Poly Silicon Gate CMOS process.

Features

- Performs all V.22 alternative B signal processing
- Very low power dissipation (40 mW typ.)
- Excellent bit error rate (BER) performance
- Interfaces to a microcontroller or bus for mode and handshake control
- Selectable extended signaling rate range
- On-chip tone generators provide:
  - — DTMF dialing
  - — 1300 Hz calling tone
  - — 2100 Hz answer tone
  - — Selectable 500 Hz and 1800 Hz guard tones
- Call progress tone detection
- Supports V.54 diagnostics on-chip
  - — Loop 1 (local digital loop)
  - — Loop 2 (remote digital loop)
  - — Loop 3 (analog loop)
- On-chip oscillator uses 3.6864 MHz crystal
- Requires ±5V
- Requires few external components
- Available in three 28-lead packages:
  - — Ceramic DIP
  - — Plastic DIP
  - — Plastic Leaded Chip Carrier (PLCC)

Connection Diagram

28-Lead DIP/28-Lead PLCC



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Top View

Note: 28-Lead PLCC (Lead numbers same as 28-Lead DIP)

***Ceramic Dual-In-Line Package**
Order Number μAV22DC
See NS Package Number F28B

***Molded Dual-In-Line Package**
Order Number μAV22PC
See NS Package Number N28B

***Plastic Leaded Chip Carrier**
Order Number μAV22QC
See NS Package Number V28A

*For most current package information, contact product marketing. For most current order information, contact your local sales office.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and PLCC	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 seconds)	300°C
Molded DIP and PLCC (soldering 10 seconds)	265°C
Internal Power Dissipation (Notes 1 and 2)	
28L-Ceramic DIP	2.50W
28L-Molded DIP	1.20W
28L-PLCC	1.39W

V_{DD} to DGND or AGND	+7.0V
V_{SS} to DGND or AGND	−7.0V
Voltage at Any Input	V_{DD} + 0.3V to V_{SS} − 0.3V
Voltage at Any Digital Output	V_{DD} − 0.3V to DGND − 0.3V
Voltage at Any Analog Output	V_{DD} + 0.3V to V_{SS} − 0.3V

Note 1: T_{JMax} = 175°C for the Ceramic DIP, 150°C for the Molded DIP and PLCC.

Note 2: Ratings apply to ambient temperauture at 25°C. Above this temperature, derate the 28L-Ceramic DIP at 16.7 mW/°C, the 28L-Molded DIP at 1.92 mW/°C, and the 28L-PLCC at 11.2 mW/°C.

Electrical Characteristics

Unless otherwise noted: V_{DD} = 5.0V, V_{SS} = −5.0V, DGND = AGND = 0V, T_A = 25°C. All digital signals are referenced to DGND; all analog signals are referenced to AGND.

Symbol	Parameter	Condition	Min	Typ	Max	Units
ANALOG INTERFACE						
	OUTPUT LEVELS AT TXO:	1200Ω from TXO to AGND				
V_{TXO}	DATA MODE (Notes 1 and 2)		0.66	0.71	0.76	V_{rms}
V_{tonehi}	DTMF HIGH Group		0.98	1.1	1.22	
V_{tonelo}	DTMF LOW Group		0.80	0.9	1.01	
P_{ext}	Out-of-band energy relative to DTMF output				−20	dB
V_{call}	Calling Tone		0.65	0.69	0.78	V_{rms}
V_{ans}	Answer Tone		0.65	0.69	0.78	
V_{TXSQ}	Transmitters Squelched			0.3		mV_{rms}
V_{OO}	Output Offset			5.0		mV_{dc}
V_{RXIN}	Talker Echo + Receiver Signal	at RXIN			1.56	V_{peak}
Z_{RXIN}	Input Impedance			100		kΩ
CLOCK INTERFACE						
F_{clock}	Clock Frequency			3.6864		MHz
T_{clktol}	Clock Frequency Tolerance		−0.01		+0.01	%
V_{extin}	External Clock Input HIGH	XTL2 driven and		4.5		V
V_{exl}	External Clock Input LOW	XTL1 grounded			0.5	V
DIGITAL INTERFACE						
V_{IL}	Input Voltage LOW				0.6	V
V_{IH}	Input Voltage HIGH		2.2			V
V_{OL}	Output Voltage LOW	I_L = 1.6 mA			0.6	V
V_{OH}	Output Voltage HIGH	I_L = −2.0 mA	3.0			V
	ALL DIGITAL INPUTS					
I_{IL}	Input Current LOW	DGND ≤ V_{IN} ≤ V_{IL},			−100	μA
I_{IH}	Input Current HIGH	V_{IH} ≤ V_{IN} ≤ V_{DD}			±50	μA
POWER INTERFACE						
I_{DD}	Supply Current at V_{DD}	No Analog Signals		5	8.0	mA
I_{SS}	Supply Current at V_{SS}			−3	−5.0	mA

Electrical Characteristics (Continued)

Unless otherwise noted: V_{DD} = 5.0V, V_{SS} = −5.0V, DGND = AGND = 0V, T_A = 25°C. All digital signals are referenced to DGND; all analog signals are referenced to AGND.

Symbol	Parameter	Condition	Min	Typ	Max	Units
ENERGY DETECTOR						
V_{thon} V_{thoff}	DATA MODE OFF/ON Threshold ON/OFF Threshold	At $\overline{RXIN}$		6.5 5.2		mV_{rms}
t_{on} t_{off}	DATA MODE Energy Detect OFF/ON timing Energy Detect ON/OFF timing	At $\overline{EDET}$	105 10	155 17	205 24	ms
V_{thon} V_{thon}	DIALER MODE OFF/ON Threshold (Dial Tone) OFF/ON Threshold (Busy, Ringback)	At $\overline{RXIN}$		10 4.6		mV_{rms}
t_{on} t_{off}	DIALER MODE Detecting Call Progress Tones Detecting Call Progress Tones	At $\overline{EDET}$	19 19	30 36	81 81	ms
TRANSMIT (ASYNC/SYNC) AND RECEIVE (SYNC/ASYNC) BUFFERS						
M	Input Character Length	Start bit + Data bits + Stop bit	8		11	bits
R_{txchar}	Input Intracharacter Signaling Rate Basic Signaling Rate Range Extended Signaling Rate Range	At $\overline{TXD}$ pin	 1170 1170	 1200 1200	 1212 1227.6	bps
L_{break} L_{brkgen}	Input Break Sequence Length Transmitted Break Length	At $\overline{TXD}$ pin At TXO pin	M 2M + 3			bits
R_{rxchar}	Output Intracharacter Signaling Rate	At $\overline{RXD}$ pin		1219.05		bps
CARRIER FREQUENCIES AND SIGNALING RATES						
F_{cxr}(CALL) F_{cxr}(ANS) Baud	Carrier Frequency (Calling Mode) Carrier Frequency (Answer Mode) Dibit (Symbol) Rate	C/$\overline{A}$ = 1 C/$\overline{A}$ = 0		1200 2400 600		Hz Hz Baud
$F_{calltone}$ $F_{anstone}$ $F_{guardlow}$ $F_{guardhigh}$	Calling Tone Frequency Answer Tone Frequency Low Guard Tone Frequency High Guard Tone Frequency	$\overline{TEST}$ = 1, HSK1 = HSK2 = 0		1301.7 2104.1 548.7 1800.0		Hz
F_{tonl}	DTMF Low Group Frequencies	Dialer Mode $\overline{TEST}$ = HSK1 = HSK2 = 0		698.2 771.9 853.3 942.3		Hz
F_{tonh}	DTMF High Group Frequencies	Dialer Mode $\overline{TEST}$ = HSK1 = HSK2 = 0		1209.4 1335.7 1476.9 1634.0		Hz
bps	Synchronous Data Rate	HS = 1 HS = 0		1200 600		bps
Tol	Tolerance of above frequencies/rates		−0.01		+0.01	%

Note 1: Output levels vary directly with V_{DD}.

Note 2: Guard tone levels, when enabled, are −6 dB (1800 Hz) and −3 dB (550 Hz) with respect to Answer mode data carrier level. When either guard tone is enabled, data carrier level is internally reduced to provide composite output power equal to that of the data carrier with guard tones disabled. See *CCITT Recommendation V.22*, para. 2.2.

Electrical Characteristics Unless otherwise noted: V_{DD} = 5.0V, V_{SS} = −5.0V, DGND = AGND = 0V, T_A = 25°C. All digital signals are referenced to DGND; all analog signals are referenced to AGND. (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
SYSTEM PERFORMANCE						
BER	**Bit Error Rate** Signal to Noise Ratio (SNR) required for indicated Bit Error Rate (BER). P_{line} = −30 dBm at RXIN, with added 5 kHz white noise (referred to 3 kHz), and −11 dBm talker echo (reflected transmitter output power). All tests were ≥5 × 10^6 bits at 1200 bps, and were performed on an AEA S3 test set. See *Figure 2*.	**C2 LINE** ANSWER MODE BER = 10^{-3} BER = 10^{-4} BER = 10^{-5} BER = 10^{-6} CALLING MODE BER = 10^{-3} BER = 10^{-4} BER = 10^{-5} BER = 10^{-6}		 4.7 6.2 7.5 8.5 6.3 7.2 8.6 9.2		 dB
		C0 LINE ANSWER MODE BER = 10^{-3} BER = 10^{-4} BER = 10^{-5} BER = 10^{-6} CALLING MODE BER = 10^{-3} BER = 10^{-4} BER = 10^{-5} BER = 10^{-6}		 5.2 6.9 8.4 10.2 7.0 8.6 10.3 11.8		 dB
F_{OS}	**Frequency offset:** incoming carrier frequency offset acquirable by receiver	Zero errors in 10^5 bits, call/answer modes, flat, C0, C2 lines. Pline = −40 dBm		±6		Hz

Note: Bit error Rate (BER) results will vary with test equipment setup, noise source, modem design, telephone interface, printed wiring board design and length of BER test.

Noise source must have a crest factor of at least 4.7 and random distribution of 5 sigma or greater to obtain accurate results.

Pin Descriptions

Pin No.	Label	Description
1 2	SLIM LIM	Connect external capacitor between pins 1 and 2. (Note 1)
3	RXIN	Line signal to modem; usually from 2-wire/4-wire hybrid. AC coupling is recommended. (Note 1)
4	$\overline{DOT}$	Test pattern. In Data ($\overline{TEST}$ = 1) or Analog Loop modes, substitutes a dotting pattern for $\overline{TXD}$, and overrides $\overline{SYNC}$, MOD1 and MOD2. If HS = 1, provides a 1200 bps dotting pattern (600 Hz square wave), and places RCVR and XMTR in SYNC mode with internal clock source. If HS = 0, provides a 600 bps dotting pattern. 1 = normal transmit data path, 0 = dotting.
5	ETC	External Transmit Clock. 600 Hz or 1200 Hz external clock providing XMTR timing in SYNC mode, selected by MOD1, MOD2. $\overline{TXD}$ changes on negative edge, sampled on positive edge. Provided at SCT if selected.

Pin No.	Label	Description
6	$\overline{SYNC}$	Selects CHAR ASYNC or BIT SYNC mode. 1 = ASYNC mode: enables XMIT & RCV buffers, sets character length according to MOD1, MOD2. 0 = SYNC mode: disables buffers, selects TX clock source with MOD1, MOD2.
7	$\overline{EDET}$	Energy Detect. In Data mode, $\overline{EDET}$ = 0 if valid signal above threshold is present for 155 ms ±50 ms, $\overline{EDET}$ = 1 if signal below threshold for >17 ms ±7 ms. In Dialer mode, follows on/off variations of call-progress tones: $\overline{EDET}$ = 0 if tones present for 30 ms ±5 ms, $\overline{EDET}$ = 1 if tones absent for 36 ms ±6 ms.
8	HS (Note 2)	Selects data rate, and transmit/receive clock rates. 1 selects 1200 bps, 0 selects 600 bps.

Pin Descriptions (Continued)

Pin No.	Label	Description
9	SCRM	Scrambler. Used alone to disable scrambler *and* descrambler for testing. Used with $\overline{\text{TEST}}$, HSK1, HSK2 to selectively disable scrambler *only*, to transmit unscrambled binary 1 (mark) during Answer mode handshake sequence (Force Unscrambled Mark). Inactive = 1 (scrambler/descrambler *enabled*). See Table II.
10	$\overline{\text{TXD}}$	XMIT Data. Serial data from host or UART. Disconnected when digitally looped, or in Dialer, Dotting, Calling Tone, Answer Tone or Force Continuous Mark or Space or Unscrambled Mark modes.
11 12	XTL2 XTL1	Frequency control. 3.6864 MHz Pierce crystal oscillator. XTL2 can be driven by external 5V logic, with XTL1 grounded. XTL2 can drive external logic through an AC-coupled buffer.
13	SCR	Serial Clock Receive. In SYNC mode, 600 Hz or 1200 Hz bit clock recovered from RCVD signal. May be pin-selected (MOD1, MOD2) as local transmit clock (SLAVE mode); provided on SCT pin if selected; undefined in ASYNC mode. $\overline{\text{RXD}}$ changes on negative edge, sampled on positive edge.
14	$\overline{\text{RXD}}$	RCVD Data. Serial data to host. Internally clamped to mark (= 1) when modem is in local digital loop or $\overline{\text{EDET}}$ is inactive (= 1).
15	$\overline{\text{RLST}}$	Remote Loop Status. Responding modem: $\overline{\text{RLST}}$ = 0 upon receipt of unscrambled binary 1 (mark) for 154 ms–231 ms. Initiating modem: if in remote digital loopback mode, asserts $\overline{\text{RLST}}$ = 0 upon receipt of scrambled mark for 231 ms–308 ms. (See Table IV.)
16 17 19	HSK1 HSK2 $\overline{\text{TEST}}$	Test and handshake selection. When $\overline{\text{TEST}}$ = 1, HSK1, HSK2, and C/$\overline{\text{A}}$ select data mode or one of five other transmit conditions, for use when programming μAV22 connect and disconnect handshaking sequences. When $\overline{\text{TEST}}$ = 0, HSK1 and HSK2 select either one of four μAV22 test conditions, or Dialer mode. (See Table II.)
18	DGND	Digital Ground.
20 21	MOD2 MOD1 (Note 2)	Character length (ASYNC) or TX clock source (SYNC) select. In ASYNC mode, selects 8, 9, 10 or 11 bit character length; in SYNC mode, selects internal, external or recovered RCV clock as XMTR data clock source. (See Table II.)
22	SCT	Serial Clock Transmit. 600 Hz or 1200 Hz clock providing XMTR timing in SYNC mode. SCT source (INT., EXT., SLAVE) selected by MOD1, MOD2 pins. $\overline{\text{TXD}}$ changes on negative edge, sampled on positive edge. Internal clock provided in ASYNC mode.
23	$\overline{\text{TXSQ}}$	Squelch XMTRS. 0 = XMTR off; 1 = on.
24	C/$\overline{\text{A}}$ (Note 2)	Calling/Answer Mode Select. Assigns channels to XMTRS/RCVRS. 1 = Calling mode, 0 = Answer mode.
25	TXO	Transmit line signal from modem; usually to 2-wire/4-wire line hybrid input. AC coupling is recommended. (Note 1)
26	AGND	Analog Ground.
27	V_{SS}	Negative power supply. V_{SS} = −5V (Note 3)
28	V_{DD}	Positive power supply. V_{DD} = +5V (Note 3)

Note 1: Capacitors in signal paths should be ≥0.033 μF and have ~ zero voltage coefficient.

Note 2: In Dialer mode with $\overline{\text{TXSQ}}$ = 1, C/$\overline{\text{A}}$, HS, MOD1 and MOD2 select the desired DTMF tone pair.

Note 3: RC decoupling is recommended: (10Ω–22Ω and 0.1 μF).

Functional Description

Figure 1 is a block diagram of the μAV22.

TRANSMITTER

The transmitter consists of a QPSK modulator, a transmit buffer and scrambler, and a transmit filter and line driver. In the asynchronous mode, serial transmit data from the host enters the transmit buffer, which synchronizes the data to the internal 600 bps or 1200 bps clock. Data which is underspeed relative to 600 bps or 1200 bps periodically has the last stop bit sampled twice, resulting in an added stop bit. Similarly, overspeed input data periodically has unsampled—and therefore deleted—stop bits. The MOD1 and MOD2 pins choose 8, 9, 10 or 11 bit character lengths. In synchronous mode the transmit buffer is disabled. The transmitter clock may be internal, external or derived from the recovered received data. A scrambler preceeds the encoder to ensure that the line spectrum is sufficiently distributed to avoid interference with the in-band supervisory single-frequency signaling system employed in most telephone system toll trunks. The randomized spectrum also facilitates timing recovery in the receiver. The scrambler is characterized by the following recursive equation:

$$Y_i = X_i \oplus Y_{i-14} \oplus Y_{i-17}$$

where X_i is the scrambler input bit at time i, Y_i is the scrambler output bit at time i. and $\oplus$ denotes the XOR operation.

V.22-type modems achieve full-duplex 1200 bps operation by encoding transmitted data by bit-pairs (dibits). The digits (symbols) are transmitted at 600 Baud (symbols/sec), thus halving both the apparent line data rate and the required signal bandwidth. This allows both transmit and receive channels to coexist in the limited bandwidth telephone channel. The four unique dibits thus obtained are gray-coded and differentially phase modulate either a 1200 Hz (Calling mode) or 2400 Hz (Answer mode) carrier. Each dibit is encoded as a phase change relative to the phase of the preceding signal dibit element:

Dibit	Phase Shift
00	+90°
01	0°
11	−90°
10	180°

At the receiver, the dibits are decoded and the bits are reassembled in the correct sequence. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator after the scrambler. In the 600 bps lowspeed mode, only the 00 and 11 dibits are utilized, representing 0 and 1, respectively. Two programmable tone generators provide V.25 calling tone (1300 Hz), CCITT answer tone (2100 Hz), guard tones (550 Hz, 1800 Hz) and 16 DTMF tone pairs. The DTMF selection matrix is shown in Table III.

The summed QPSK modulator and tone generator outputs drive a lowpass filter which both serves as a fixed compromise amplitude and delay equalizer for the telephone line and reduces output harmonic energy. The filter output drives an output buffer amplifier with low output impedance. The buffer provides a nominal 0.7 Vrms output in data mode. In the dialer mode, nominal DTMF output levels are 0.90 Vrms (low group) and 1.11 Vrms (high group). These levels are +2 dB and +4 dB with respect to data mode output level.

RECEIVER

The received signal from the line-connection circuitry drives a lowpass filter which performs anti-aliasing, and compromise amplitude and delay equalization of the incoming signal. Depending upon mode selection the following mixer either passes (Answer mode) or down converts (Calling mode) the signal to the 1200 Hz bandpass filter. In Analog Loopback mode, the receiver calling and answer mode assignments are inverted, which forces the receiver to operate in the transmitter frequency band. In this self-test configuration, a fraction of the transmit signal reflects to the RXIN pin due to the mismatch caused by the modem being on-hook (disconnected from the telephone line).

In Data mode, the 1200 Hz bandpass filter passes the desired received signal while attenuating the adjacent transmitted signal component reflected from the line (talker echo). The chosen passband converts the spectrum of the received highspeed signal to a raised cosine shape to minimize intersymbol interference in the recovered data. Following the filter is a soft limiter and a signal energy detector. An external capacitor is required to eliminate the DC offset between the soft limiter output and the following limiter/comparator.

The energy detector provides a digital indication that energy is present within the filter passband at a level above a preset threshold. At least 2 dB of hysteresis is provided between on and off levels to stabilize the detector output. In Dialer mode, integration times are modified so that the detector output follows the on/off envelope signature of call progress tones.

The limiter output drives the QPSK demodulator and the carrier and clock recovery phase-locked loops; these form a digital coherent receiver. The demodulator outputs are in-phase (I) and quadrature (Q) binary signals which together represent the recovered dibit stream. The dibit decoder circuit utilizes the recovered clock signal to convert this dibit stream to serial data at 600 bps or 1200 bps.

The recovered bit stream is then descrambled, using the inverse of the transmit scrambler algorithm. In synchronous mode the descrambler output is identically the received data, while in asynchronous mode the descrambler output stream is selectively processed by the receive buffer. Underspeed data presented to the transmitting modem passes essentially unchanged through the receive buffer. Overspeed data, which had stop bits deleted at the transmitter, has those stop bits reinserted by the receive buffer. (Generally, stop bit lengths will be elastic.) The receive buffer output is then presented to the receive data pin ($\overline{RXD}$) at a nominal intracharacter rate of 1219.05 bps in both basic and extended signaling rate modes.

MASTER CLOCK/OSCILLATOR/DIVIDER CHAIN

The μAV22 clock source may be either a quartz crystal operating in parallel mode or an external signal source at 3.6864 MHz. The crystal is connected between XTL1 and XTL2, with 30 pF net capacitance from each pin to ground (see *Figure 1*). The external capacitors should be mica or high-Q ceramic. An external circuit may be driven from XTL2: AC coupling to a high impedance load should be used; total capacitance to ground from XTL2, including the

Functional Description (Continued)

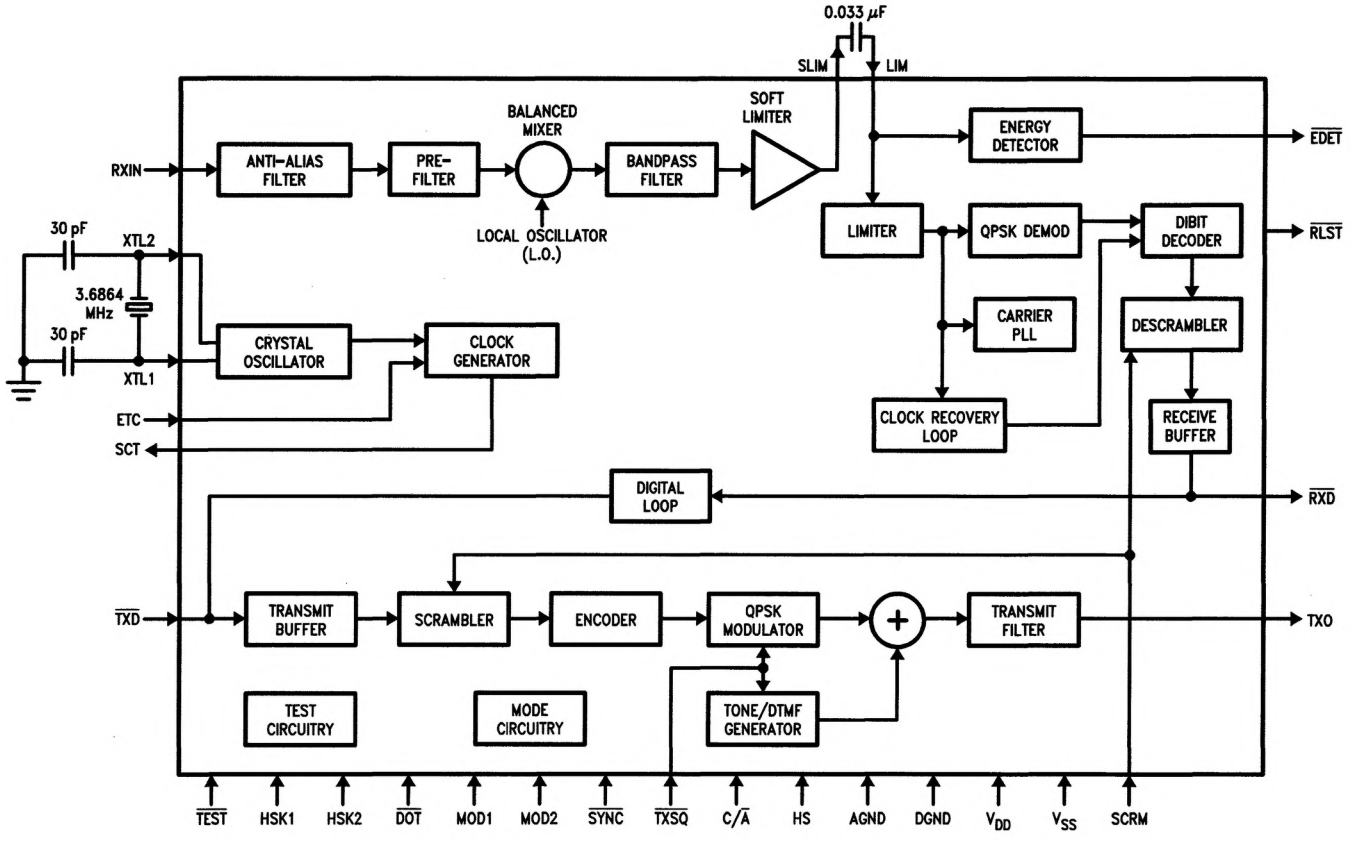

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FIGURE 1. Block Diagram

Functional Description (Continued)

external circuit, should be 30 pF. Crystal requirements: $R_S < 150\Omega$, $C_L = 18$ pF, parallel mode, tolerance (accuracy, temperature, aging) less than ±75 ppm. An external 5V drive may be applied to the XTL2 pin, with XTL1 grounded. Internal circuits provide the timing signals required for the signal processing functions. Timing for line connect and disconnect sequences (handshaking) derives from the host controller, ensuring maximum applications flexibility.

CONTROL CONSIDERATIONS

The host controller, whether a dedicated micro-controller or a digital interface, controls the μAV22 as well as the line connect circuit and other IC's. μAV22 on-chip timing and logic circuitry has been specifically designed to simplify the development of control firmware.

OPERATING AND TEST MODES

Table II indicates the handshake, data and test mode groups directly accessed by the μAV22 control pins, in conjunction with the host controller.

The handshake mode group includes Dialer Mode, Calling Tone, Answer Tone, Force Unscrambled Mark, Force Continuous Mark, and Force Continuous Space. Calling Tone (1300 Hz) is utilized in conjunction with Dialer Mode for V.25 Autodialing applications. Answer Tone (2100 Hz) and Force Unscrambled Mark are required for the Answer mode handshake sequence. Force Continuous Mark is used in both Calling and Answer mode sequences. Force Continuous Space simplifies transmission of Break and Space Disconnect sequences. See *CCITT Recommendation V.22.*

The μAV22 supports local and remote digital loopback (V.54 Loop 1 and Loop 2) and analog loopback (V.54 Loop 3). Analog loopback forces the receiver to the transmitter channel. The controller forces the line control circuit on-hook but continues to monitor the ring indicator. This mode is available for 600 bps and 1200 bps synchronous and asynchronous operation. In local digital loop, the μAV22 isolates the interface, slaves the transmit clock to SCR (high-speed mode), and loops received data back to the transmitter. In remote digital loop, local digital loop is initiated in the far-end modem by request of the near-end modem, if the far-end modem is so enabled. The μAV22 includes the handshake sequences required for this mode; the controller merely monitors $\overline{RLST}$ and controls remote loopback according to Table IV. Remote loop is available in both 600 bps and 1200 bps modes.

Calling Tone If selected, and $\overline{TXSQ} = 1$, μAV22 transmits 1300 Hz calling tone, for use in V.25 automatic dialing, during the Calling mode connect sequence.

Answer Tone If selected, and $\overline{TXSQ} = 1$, μAV22 transmits 2100 Hz answer tone, during the Answer mode connect sequence. Receiver data rate is independently selected with the HS pin.

Force Unscrambled Mark Disconnects $\overline{TXD}$ pin from the transmitter and—if $\overline{TXSQ} = 1$—forces transmission of an unscrambled mark (binary 1). Utilized during the Answer mode connect sequence. The descrambler remains enabled to allow reception of scrambled mark from the Calling modem.

Force Continuous Mark Disconnects $\overline{TXD}$ pin from the transmitter and—if $\overline{TXSQ} = 1$—forces transmission of a scrambled mark (binary 1). Utilized during the Calling mode connect sequence.

Force Continuous Space Disconnects $\overline{TXD}$ pin from the transmitter and—if $\overline{TXSQ} = 1$—forces transmission of a space (binary 0). Utilized for transmitting Break and Space Disconnect sequences. Break transmission—whether forced by this mode or application of binary 0 to $\overline{TXD}$ in Data mode—automatically obeys *CCITT Recommendation V.22,* para. 4.2.1.3.

Analog Loop Local test mode. The modem receiver is forced to the transmitter channel (selected by the C/$\overline{A}$ pin). With modem on-hook (disconnected from line), signal from TXO is reflected through the line hybrid to RXIN.

Local Digital Loop Forces synchronous mode, and internally loops received data to transmitter and SCR to SCT. Transmit data ($\overline{TXD}$) and external clock (ETC) are ignored. SCR and SCT are provided. $\overline{RXD}$ is forced to 1.

Remote Digital Loop **Initiating modem.** If RDL is initiated ($\overline{TEST} = 0$, HSK1 = 1, HSK2 = 0), $\overline{TXD}$ is isolated, $\overline{RXD} = 1$, and unscrambled mark (binary 1) is transmitted. Upon detection of scrambled dotting pattern (alternating 1's and 0's) from the remote modem, scrambled mark is transmitted. Upon subsequent receipt of scrambled mark, $\overline{RLST}$ is set to 0. RDL is terminated by setting $\overline{TXSQ} = 0$ for 77 ms.

Responding modem. Upon receipt of unscrambled mark while in data mode ($\overline{TEST}$ = HSK1 = HSK2 = 1), μAV22 sets $\overline{RLST} = 0$. The controller responds by setting $\overline{TEST}$ = HSK2 = 0; μAV22 sets synchronous mode, isolates $\overline{TXD}$, clamps $\overline{RXD}$ to 1 and transmits a scrambled dotting pattern. Then, upon receipt of scrambled mark (binary 1), μAV22 internally loops received data and clock to the XMTR, and resets $\overline{RLST}$ to 1 (see Table IV).

Dialer (ACU) Mode Dialer Mode ($\overline{TEST}$ = HSK1 = HSK2 = 0) selects both DTMF transmission and Call Progress Tone Detection.

DTMF generation. $\overline{TXSQ} = 1$ enables the DTMF generator. 16 DTMF tone pairs can be selected by C/$\overline{A}$, HS, MOD1, and MOD2. (See Table III.)

Call Progress Tone Detection. Energy detector response times are altered and receive filter frequency response is downscaled, to enable tracking the on/off envelope of call progress tone pairs in the 350 Hz to 850 Hz band. When $\overline{TXSQ} = 0$, $\overline{EDET}$ provides this information to the controller to enable identification of dial tone, busy, ringback, and voice signals.

Functional Description (Continued)

GUARD TONE AND SIGNALING RATE SELECTION

In addition to the above handshake, data and test modes, μAV22 provides for transmission of 550 Hz or 1800 Hz guard tones in the Answer mode only (*CCITT Recommendation V.22*, para. 2.2), and selection of either the Basic or Extended signaling rate range in Character Asynchronous Mode (paras. 4.2.1.1, 4.2.1.2). If the Basic signaling rate range is selected, μAV22 accepts 600 bps or 1200 bps +1%, −2.5%. If the Extended signaling rate range is chosen, μAV22 accepts 600 bps or 1200 bps +2.3%, −2.5%. **μAV22 powers up with 1800 Hz guard tone selected and enabled, and Basic signaling rate range selected.** Other options are chosen following power-up, according to the following sequence:

1. Set $\overline{SYNC}$ = MOD1 = MOD2 = $\overline{TXSQ}$ = 0.
2. Set HS, HSK1 and HSK2 according to Table I.
   - HS selects Basic or Extended Signaling Range.
   - HSK1 selects 550 Hz or 1800 Hz Guard Tone.
   - HSK2 enables or disables Guard Tone.
3. Toggle $\overline{TEST}$ from 1 to 0 to 1 to latch the selections. Ensure that $\overline{TEST}$ = 0 for ≥ 200 ns.

TABLE I. Guard Tone and Signaling Rate Selection

	1	0
HS	Extended Range	Basic Range
HSK1	550 Hz	1800 Hz
HSK2	Tone Off	Tone On

TABLE II. Operating and Test Modes

$\overline{DOT}$	HS	$\overline{SYNC}$	MOD1	MOD2	$\overline{TEST}$	HSK1	HSK2	C/$\overline{A}$	SCRM	Description	SCT
1	X	X	X	X	0	0	0	X	X	Dialer Mode (See Table III)	*
1	—	—	—	—	1	0	0	1	1	Calling Tone (1300 Hz)	*
1	—	—	—	—	1	0	0	0	1	Answer Tone (2100 Hz)	*
1	—	—	—	—	1	0	1	—	0	Force Unscrambled Mark	*
1	—	—	—	—	1	0	1	—	1	Force Continuous Mark	*
1	—	—	—	—	1	1	0	—	1	Force Continuous Space	*
1	—	1	0	0	1	1	1	—	1	ASYNC, 8 Bit	INT
1	—	1	0	1	1	1	1	—	1	ASYNC, 9 Bit	INT
1	—	1	1	1	1	1	1	—	1	ASYNC, 10 Bit	INT
1	—	1	1	0	1	1	1	—	1	ASYNC, 11 Bit	INT
1	—	0	1	1	1	1	1	—	1	SYNC, Internal	INT
1	—	0	1	0	1	1	1	—	1	SYNC, Slave	SCR
1	—	0	0	1	1	1	1	—	1	SYNC, External	ETC
—	—	—	—	—	0	0	1	—	1	Analog Loop	*
1	—	X	X	X	0	1	1	—	1	Local Digital Loop	SCR
1	—	—	—	—	0	1	0	—	1	Remote Digital Loop Initiate	*
1	—	X	X	X	0	1	0	—	1	Response to far end RDL request	SCR
0	—	X	X	X	1	X	X	—	1	Dotting Pattern (600 bps to 1200 bps)	INT

Key:

X—Don't Care (except avoid $\overline{SYNC}$ = MOD1 = MOD2 = 0)

— —Set as appropriate for desired operation condition.

SCT column denoters source of transmitter timing at SCT pin:

*****—determined by $\overline{SYNC}$, MOD1, MOD2

INT—internal 600 Hz or 1200 Hz clock

ETC—external 600 Hz or 1200 Hz clock

SCR—slaved to recovered receive clock

Functional Description (Continued)

TABLE III. DTMF Encoding

$\overline{TXSQ}$	C/$\overline{A}$	HS	MOD1	MOD2	DTMF Digit/Tones	
0	X	X	X	X	DTMF Off	
1	0	0	0	0	0	941/1336
1	0	0	0	1	1	697/1209
1	0	0	1	0	2	697/1336
1	0	0	1	1	3	697/1477
1	0	1	0	0	4	770/1209
1	0	1	0	1	5	770/1336
1	0	1	1	0	6	770/1477
1	0	1	1	1	7	852/1209
1	1	0	0	0	8	852/1336
1	1	0	0	1	9	852/1477
1	1	0	1	0	*	941/1209
1	1	0	1	1	#	941/1477
1	1	1	0	0	A	697/1633
1	1	1	0	1	B	770/1633
1	1	1	1	0	C	852/1633
1	1	1	1	1	D	941/1633

TABLE IV. Remote Digital Loopback (RDL) Command Sequences

μAV22 Internal Sequences	Sequence Labels	Control Inputs			Response
		$\overline{TEST}$	HSK1	HSK2	$\overline{RLST}$
Data Mode (Initial Conditions)		1	1	1	1
Initial RDL:	"INITIATE RDL"	0	1	0	1
Disable scrambler					
Disconnect $\overline{TXD}$					
Force 1 on $\overline{RXD}$					
Transmit unscrambled mark (U.M.)					
Recognize Dotting for 231 ms–308 ms					
Enable scrambler					
Transmit scrambled mark (S.M.)					
Recognize S.M. for 231 ms–308 ms					
Connect $\overline{TXD}$					
Unclamp $\overline{RXD}$					
"RDL ESTABLISHED"					
Response to far-end request		1	1	1	0
U.M. recognized for 154 ms–231 ms					
"RDL REQUESTED"	"RDL RESPONSE OK"	0	1	0	0
Disconnect $\overline{TXD}$					
Force 1 on $\overline{RXD}$					
Force Sync Slave Mode					
Transmit Dotting					
S.M. recognized					
Internally loop Receiver to Transmitter					
"RDL ESTABLISHED"		0	1	0	1
Terminate RDL:	$\overline{TXSQ}$ = 0 for 80 ms	1	1	1*	0
Reset to Data Mode		1	1	1	1

*$\overline{TEST}$ = HSK1 = HSK2 = 1 may be asserted at any time after "RDL ESTABLISHED" and before terminating.

Functional Description (Continued)

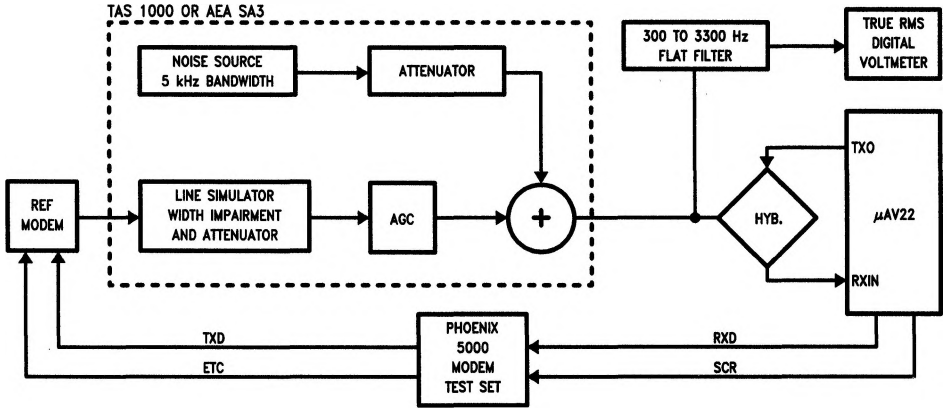

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FIGURE 2. Two-Wire Bit Error Rate (BER) Test Setup