Phase Control Circuit for Industrial Applications

Description

The UAA145 is a bipolar integrated circuit, designed to provide phase control for industrial applications. It permits the number of components in thyristor drive circuits to be drastically reduced. The versatility of the device is further enhanced by the provision of a large number of pins giving access to internal circuit points.

Features

- Separate pulse output synchronized by mains half wave
- Output pulse-width is freely adjustable
- Phase angle variable from >0° to <180°
- High-impedance phase shift input
- Less than 3° pulse symmetry between two half-cycles or phase of different integrated circuits
- Output pulse blocking

Applications

- Industrial power control
- Silicon controlled rectifier

Package: DIP16 (special case)

Block Diagram

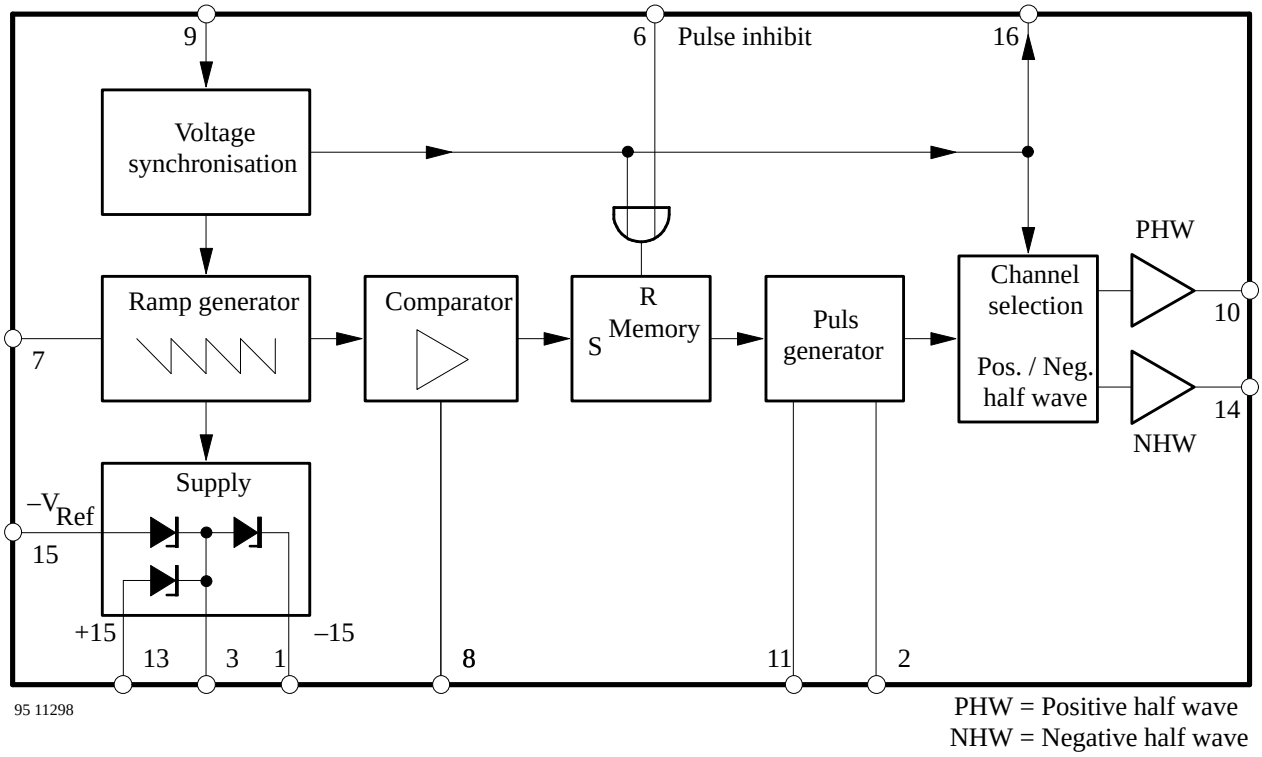


Figure 1. Block diagram

General Description

The operation of the circuit is best explained with the help of the block diagram shown in figure 1. It comprises a synchronizing stage, ramp generator, voltage com-parator, pulse generator, channel selecting stage and two output amplifiers. The circuit diagram in figure 2 also shows the external components and terminal connections necessary for operation of the circuit.

As can be seen from figure 2, the circuit requires two supply rails i.e. a +15 V and a –15 V. The positive voltage is applied directly to Pin 1, while an external series resistor in each line is used to connect the negative voltage Pin 13 and Pin 15. In the following circuit description each section of the block diagrams is discussed separately.

Synchronization Stage

Pin 9 is connected, via a voltage divider (22 kΩ and R_p), to the ac line (sync. signal source). A pulse is generated during each zero crossover of the sync. input. The pulse duration depends on the resistance R_p and has a value of 50 to 100 µs. (figure 2).

In addition to providing zero voltage switching pulses this section of the circuit generates blocking signals for use in the channel selecting stage.

Ramp Generator

Transistor T_7 amplifies the zero-crossover switching pulses. During the sync process capacitor C_S at Pin 7 is charged to the operating voltage of reference diode Z_4, i.e., to approximately 8.5 V, the charging time being always less than the duration of the sync pulse. The capacitor discharges via resistor R_S during each half-cycle. The discharge voltage is of the same magnitude as the charge voltage, and is determined by Z_3. To ensure an approximately linear ramp waveform, the voltage is allowed to decay up to ca. 0.7 C_sR_s. Because Z-diodes Z_3 and Z_4 have the same temperature characteristics, the timing of the ramp zero crossover point in relation to that of the sync. pulse is constant, and consequently the pulse phasing rear limit is also very stable.

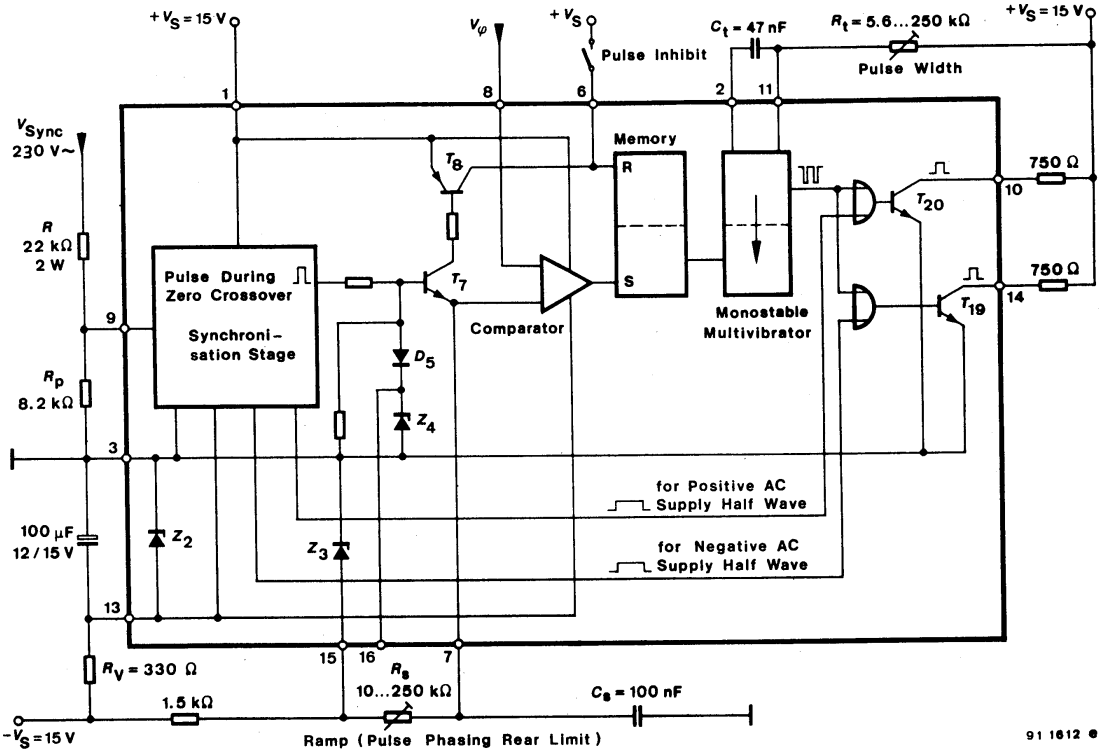


Figure 2. Block diagram and basic circuit

Comparator (Differential Amplifier) and Memory

In the (voltage) comparator stage, the ramp voltage is compared with the shift voltage V_φ applied to Pin 8. The comparator switches whenever the instantaneous ramp voltage is the same as the shift voltage (corresponding to the desired phase angle), thereby causing the memory to be set, i.e. the integrated thyristor in memory is to be turned on. The time delay between the signal input and the comparator output signal is proportional to the required phase angle. Design of the circuit is such that the memory content is reset only during the instant of zero crossover, the reset signal always overriding the set signal. This effectively prevents the generation of additional output pulses and causes any pulse already started to be immediately inhibited on application of an inhibit signal to Pin 6. The memory content can also be reset via Pin 6. Thus the memory ensures that any noise (negative voltage transients) superimposed on the shift signal at Pin 8 cannot give rise to the generation of multiple pulses during the half-cycle.

Pulse Generator (Monostable Multivibrator)

The memory setting pulse also triggers a monostable stage. The duration of the pulse produced by the monostable is determined by C_t and R_t, connected to Pin 2 and Pin 11.

Channel Selection and Output Amplifier

A pulse is produced at either output Pin 10 or Pin 14 if transistor T_{20} or T_{19} respectively is cut-off. The pulses derived from the pulse generator are applied to the output transistors via OR gates controlled by the half-cycle signals derived from the sync stage. During the positive half-cycle no signal is applied from the sync stage to T_{19} so that an output pulse is produced at Pin 14. The same is valid for Pin 10 during the negative half-cycle.

Pulse Diagram

Figure 3 shows the pulse voltage waveforms measured at various points of the circuit, all signals being time referenced to the sync signal shown at the top. The input circuit limits any signal applied to ± 0.8 V at Pin 9. The sync pulse can be measured at Pin 16, whereas the ramp waveform and the pulse phasing rear limit (φ_h) are at Pin 7. The time relationship between the shift voltage applied to Pin 8 and the ramp waveform is indicated by dotted lines. A pulse trigger signal is produced whenever the ramp crosses the shift level. The memory control pulse can be monitored by means of an oscilloscope applied to Pin 6. The Pin 11 pulse waveform is that at C_t, and the waveforms at Pin 10 and Pin 11 are those of the output pulses.

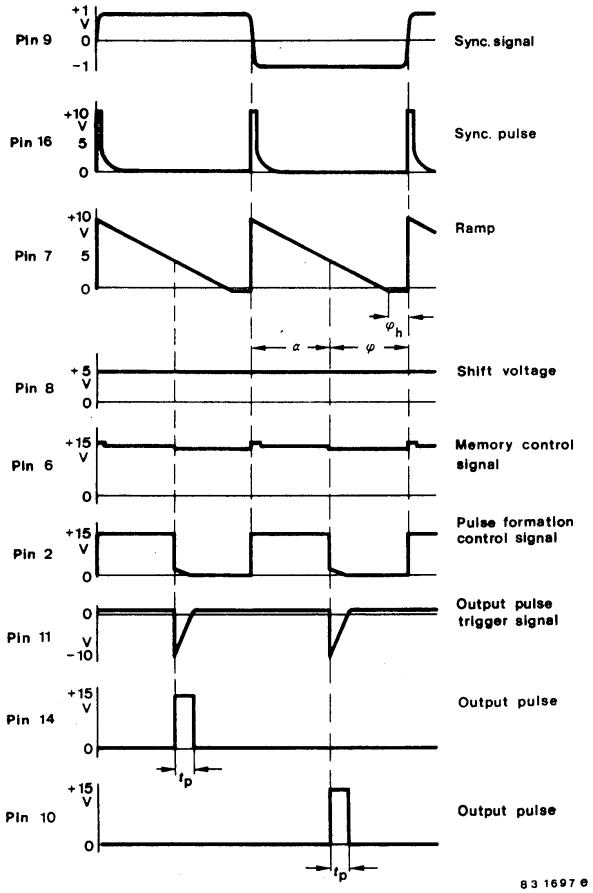


Figure 3. Pulse diagram

Influence of External Components, Syncronization Time

An ideal 0 to 180° shift range and perfect half-cycle pulse timing symmetry are attained, if the sync pulse duration is kept short. However, there is a lower pulse duration limit, which is governed by the time required to charge capacitor C_s (figure 5).

As can be seen, it takes about 35 µs to charge C_s. The sync time can be altered by adjustment of R_p, the relationship between R_p and the sync time being shown in figure 6. The ratio of R and R_p determines the width of internal sync pulse, t_{sync}, at Pin 16. The pulse shape is valid only for sync pulse of 230 V~. The lower the sync voltage, longer is the sync pulse.

A minimum of 50 µs (max. 200 µs) input sync pulse is required for a pulse symmetry of $\Delta\varphi \leqq \pm 3°$.

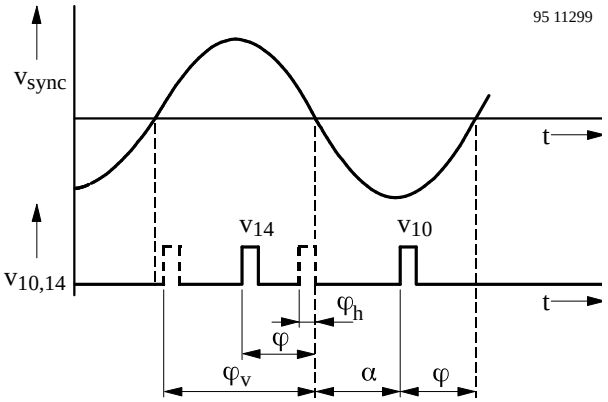


Figure 4. Pulse phasing

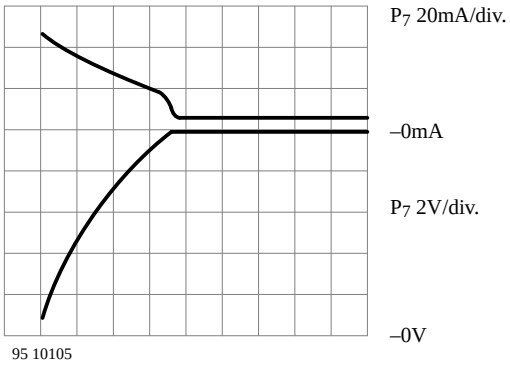


Figure 5. Charging time 10 µs/div.

Pulse Phasing Limits

The pulse phasing front limit is determined by limiting the maximum shift voltage applied to Pin 8 which is thus adjustable by external circuitry. This can be done by connecting a Z-diode between Pin 8 and Pin 3. The pulse phasing rear limit, φ_h, is the residual phase angle of the output pulses when the shift voltage V_φ is zero. Since φ_h coincides with the zero crossover point of the ramp, it can be adjusted by variation of the time constant C_sR_s (figure 14). Figure 10 shows the pulse phasing rear limit plotted as a function of R_s.

Pulse Blocking

The output pulses can be blocked via Pin 6, the memory content being erased whenever Pin 6 is connected to $+V_S$ (Pin 1). This effectively de-activates the pulse generator; any output pulse in the process of generation is interrupted.

Pulse blocking can be accomplished either via relay contacts or a PNP switching transistor (figure 14).

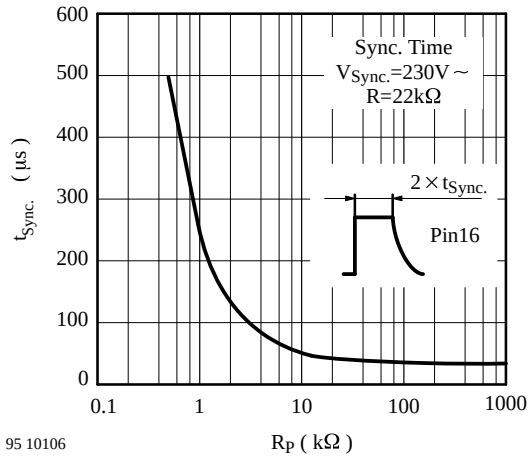


Figure 6.

Output Pulse Width

The output pulse width can be varied by adjustment of R_t and C_t. In figure 11 pulse width is shown plotted as a function of R_t for C_t = 50 nF.

The output pulse always finishes at zero crossover. This means that if there is a minimum pulse width requirement (for example, when the load is inductive) provision must be made for a corresponding pulse phasing rear limit. The output stages are arranged so that the transistors are cut off when a pulse is produced. Consequently, the thyristor trigger pulse current flows via the external load resistors, this current being passed by the transistors during the period when no output pulse is produced. During this period the output voltage drops to the transistor saturation level and is therefore load dependent. Figure 12 shows the relationship between saturation voltage and load current.

Shift Characteristic

In figure 13 the angle of phase shift is shown plotted as a function of the voltage applied to Pin 8 for a pulse phasing rear limit of approximately 0°. Because the ramp waveform is a part of the exponential function, the shift curve is also exponential.

The limitation of the shift voltage to approximately 8.5 V is due to the internal Z-diode Z_4, which has a voltage spread of 7 to 9 V.

The waveforms in figures 7 to 9 show the output pulse phase shift as a function of V_φ. It can be seen from the oscillograms, the instants at which pulses are released coincide with the intersections of the ramp and the shift voltage.

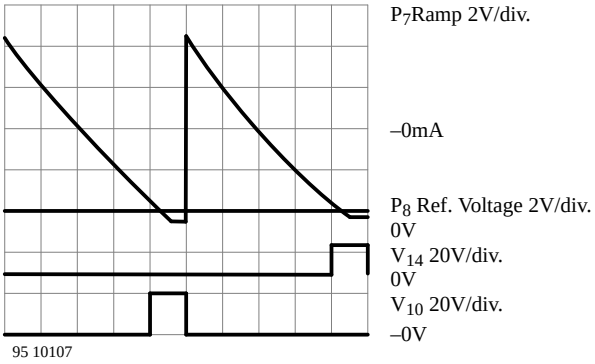


Figure 7. Output pulses phase shift 2 ms/div

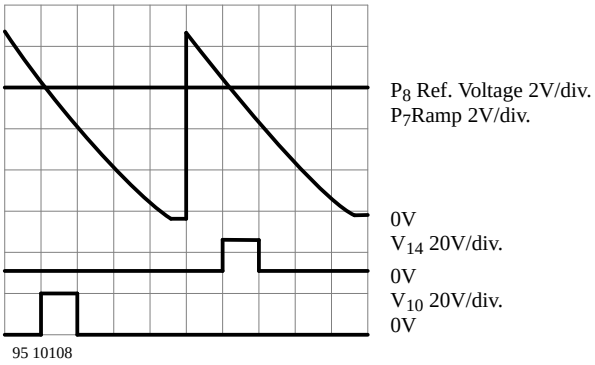


Figure 8. Output pulses phase shift 2 ms/div

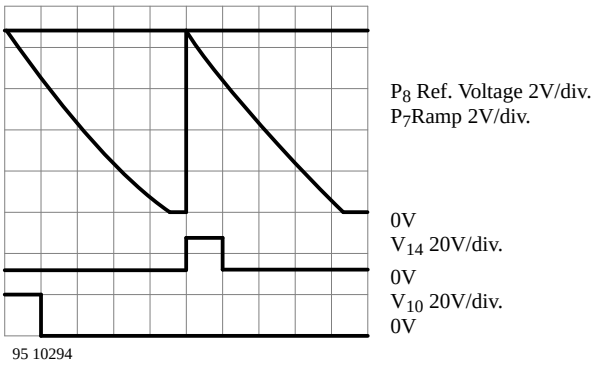


Figure 9. Output pulses phase shift 2 ms/div

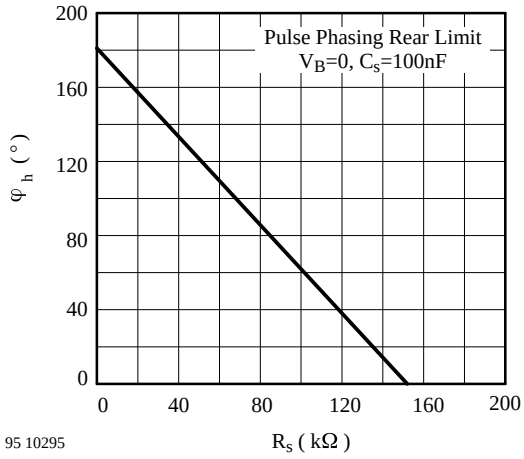


Figure 10.

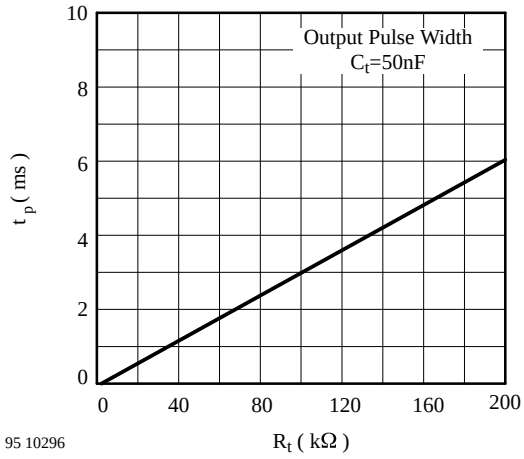


Figure 11.

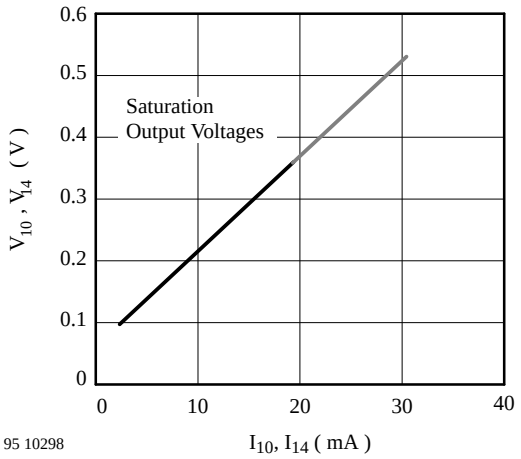


Figure 12.

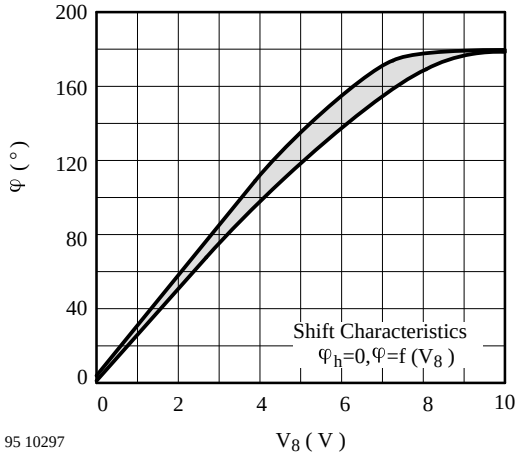


Figure 13.

Absolute Maximum Ratings

Reference point Pin 3, T_{amb} = 25°C, unless otherwise specified

Parameters		Symbol	Value	Unit
Positive supply voltage	Pin 1	V_S	18	V
Shift voltage	Pin 8	V_φ $-V_\varphi$	V_{S1} 5	V V
Reverse voltage, control input	Pin 11	$-V_{IR}$	15	V
Negative supply current	Pin 13 Pin 15	$-I_S$	25 5	mA
Synchronization current	Pin 9	$\pm I_{sync}$	20	mA
Control input pulse current	Pin 11	I_I	3	mA
Output currents	Pin 10 Pin14	I_O	20 20	mA
Total power dissipation Tamb ≦ 70°C		P_{tot}	550	mW
Junction temperature		T_j	125	°C
Ambient temperature range		T_{amb}	–25 to +70	°C
Storage temperature range		T_{stg}	–25 to +125	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient Junction case	R_{thJA} R_{thJC}	100 35	K/W

DC Characteristics

V_{S1} = 13 to 16 V, $-I_{S13}$ = 15 mA, reference point Pin 3, figure 2, T_{amb} = 25°C, unless otherwise specified

Parameters	Test Conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Positive supply current	V_S = 16 V Pin 1	I_S	12		30	mA
Voltage limitation	$-I_{S13}$ = 15 mA Pin 13 $-I_{S15}$ = 3.5 mA Pin 15 V_S = 13 V, V_9 = 0V Pin 16	$-V_{Z2}$ $-V_{Z3}$ V_{Z4}	7.0 7.0 7.0		9.0 9.0 9.0	V
Input current	V_S = 16 V, Pin 8 $V_{\varphi 8}$ = 13 V, V_7 = 0V, I_9 = 0.3 mA	I_φ			10	µA
C_t-potential shift current	$V_S = V_{I2}$ =13 V, Pin 2 V_{I7} = 3 V, $I_{\varphi 8}$ = 5 µA, I_9 = 0.3 mA	I_I	4.5			mA
C_t-charging current	V_S = 13 V, Pin 2 $V_{I2} = V_{I7}$ = 0 V $V_{\varphi 8} = V_9$ = 0V t_p/T = 0.01, $t_p \leqq$ 1 ms	$-I_I$	10		30	mA
C_S-charging current	Pin 7 $V_S = V_{I2} = V_{\varphi 8}$ = 13 V $V_{I7} = V_9$ = 0V t_p/T = 0.01, $t_p \leqq$ 1 ms	$-I_I$	20		62	mA
Output saturation voltage	$V_S = V_{I2}$ =16 V, $V_{I7} = V_{\varphi 8}$ = 0 V, I_{I11} = 50 µA I_{10} = 20 mA, $-I_9$ = 0.3 mA, Pin 10 I_{14} = 20 mA, I_9 = 0.3 mA Pin 14	V_{Osat} V_{Osat}		0.3 0.3	1.0 1.0	V

AC Characteristics

T_{amb}= 25°C, figures 2, 4 and 14

Parameters	Test Conditions / Pin	Symbol	Min.	Type.	Max.	Unit
Rise time	Pin 10 Pin 14	t_r			0.5 0.5	µs
Pulse width	figure 11 Pin 10 Pin 14	t_p t_p	0.1 0.1		4 4	ms
Pulse phasing difference for two half-waves	f = 50 Hz	$\Delta\varphi$			± 3	°
Inter lC phasing difference	f = 50 Hz	$\Delta\varphi$			± 3	°
Pulse phasing front limit	f = 50 Hz, figure 4	φ_v	177			°
Pulse phasing rear limit	f = 50 Hz, figures 4 and 10	φ_h			0	°

Angle of current flow φ = 0 to 177° at $V_{\varphi 8}$ = 0.2 to 7.5 V, φ_h = 0°, figures 4 and 13

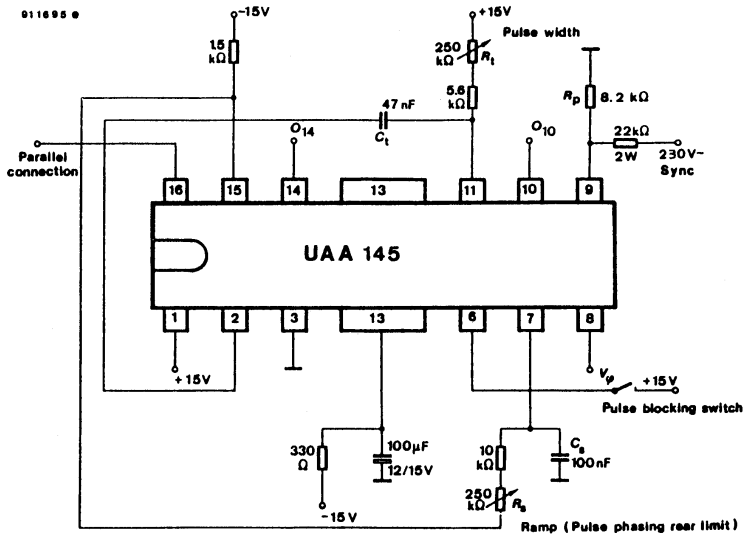


Figure 14. Test circuit for ac characteristics

Applications

Parallel connection for three-phase current applications

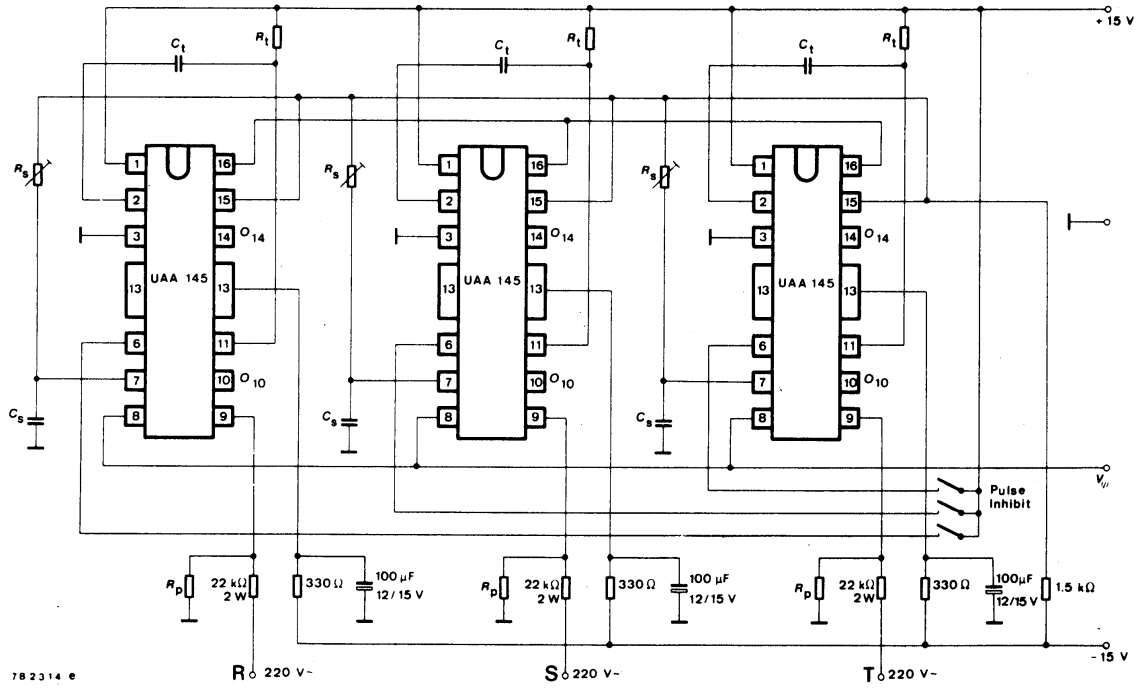


Figure 15. Parallel connection for three-phase current applications. For polyphase operation connect all Pins 15 and Pins 16.

To ensure good pulse phasing symmetry as well as identical shift characteristics in three-phase applications, when three devices are employed, two parallel connection pins (figure 15) are provided on each device. Besides the supply pins, the input pins 15 and 16 are to be paralleled. If this is done, then all the Z_4 and Z_3 diodes are connected in parallel so that the reference voltage effective for all three devices becomes that of the Z-diode with the lowest operating voltage. In this way all the C_S capacitors are charged and discharged to the same voltage levels. By symmetrical adjustment of the time constants with resistors R_S, good pulse phasing symmetry and identical shift characteristics are attained.

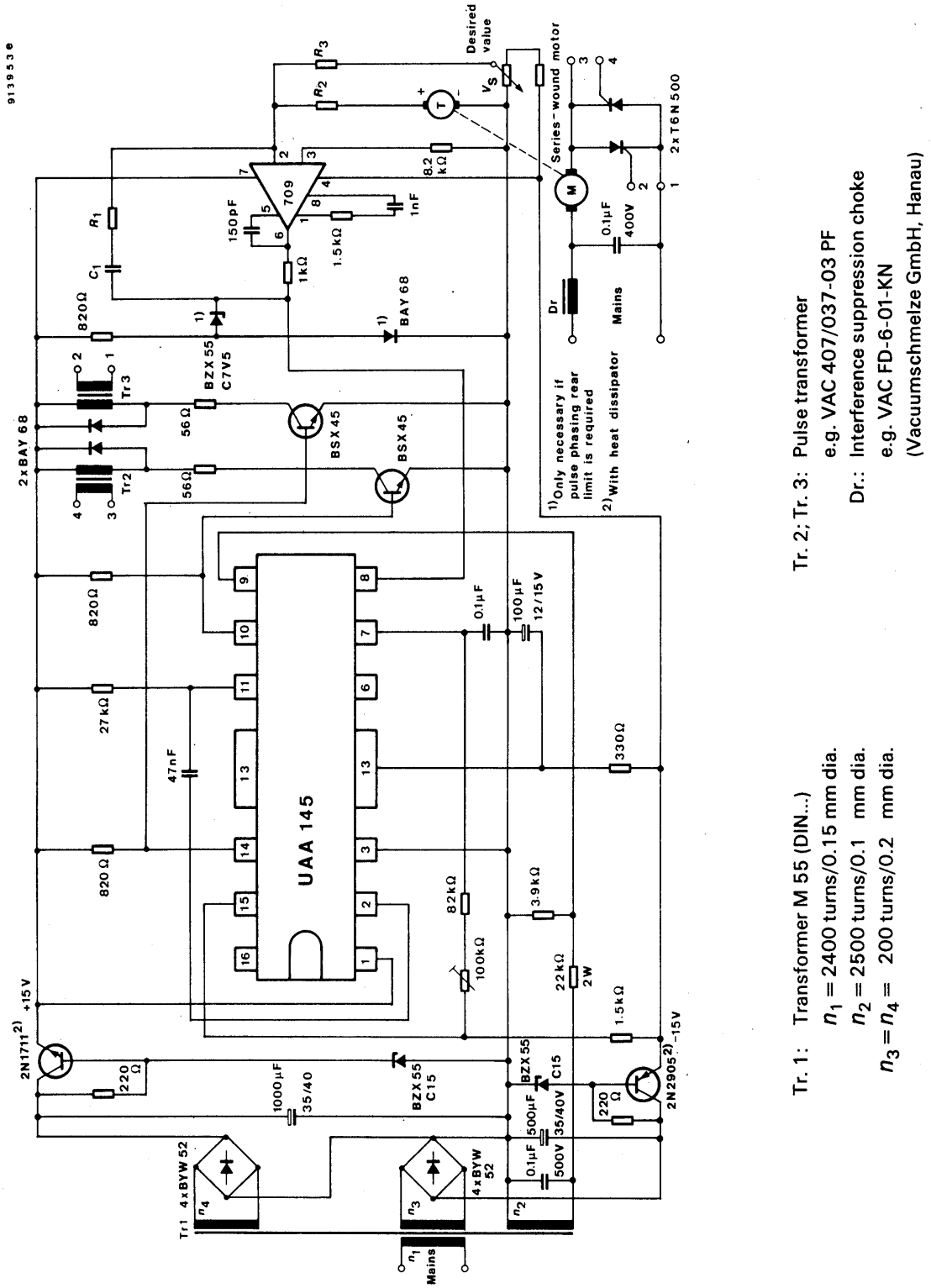
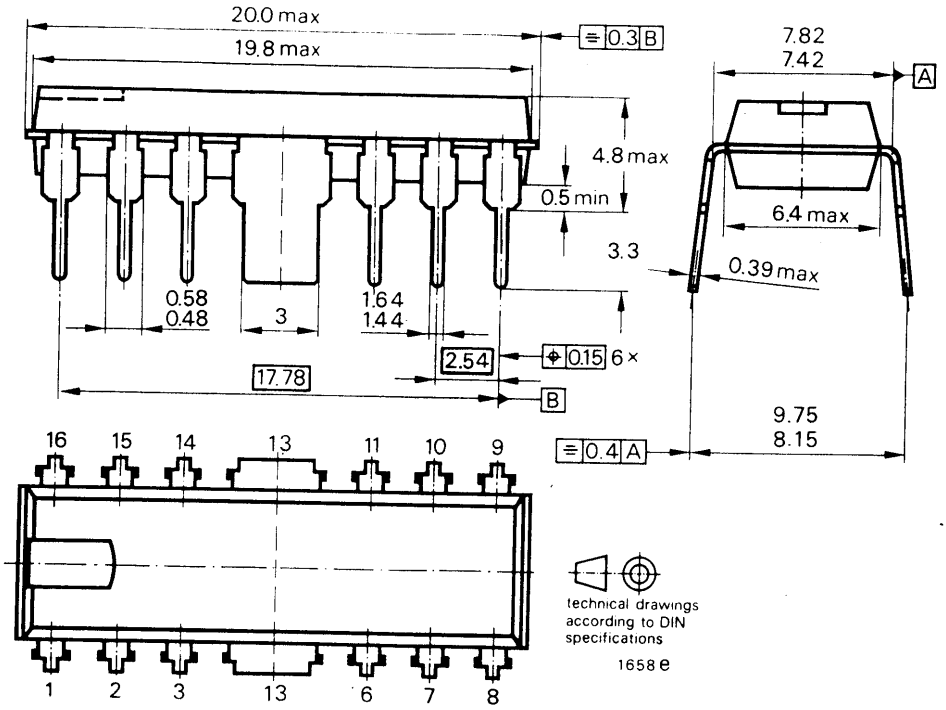


Figure 16. Speed control with tacho-generator

Dimensions in mm



Case:
DIP 16
(Special case)

Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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