DECT PLL / TX IC

Description

The U2785B is an RF IC for low-power DECT transmit applications. The SSO28-packaged IC is a complete PLL including a 1-GHz prescaler, on-chip frequency doubler, biasing for off-chip VCO, an integrated TX-filter and a modulation compensation circuit for advanced closed-loop modulation concept. No mechanical tuning is necessary in production.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- 1-GHz PLL, TX data filter (10.368-MHz / 20.736-MHz reference clock), frequency doubler
- Low current consumption
- Few external components
- Supply-voltage range 2.7 V to 4.7 V
- Switchable charge-pump current for enhanced switching time
- Two operational amplifiers for active loop filter
- Advanced closed-loop modulation (with 10.368-MHz / 20.736-MHz reference clock) and open-loop modulation supported

Block Diagram

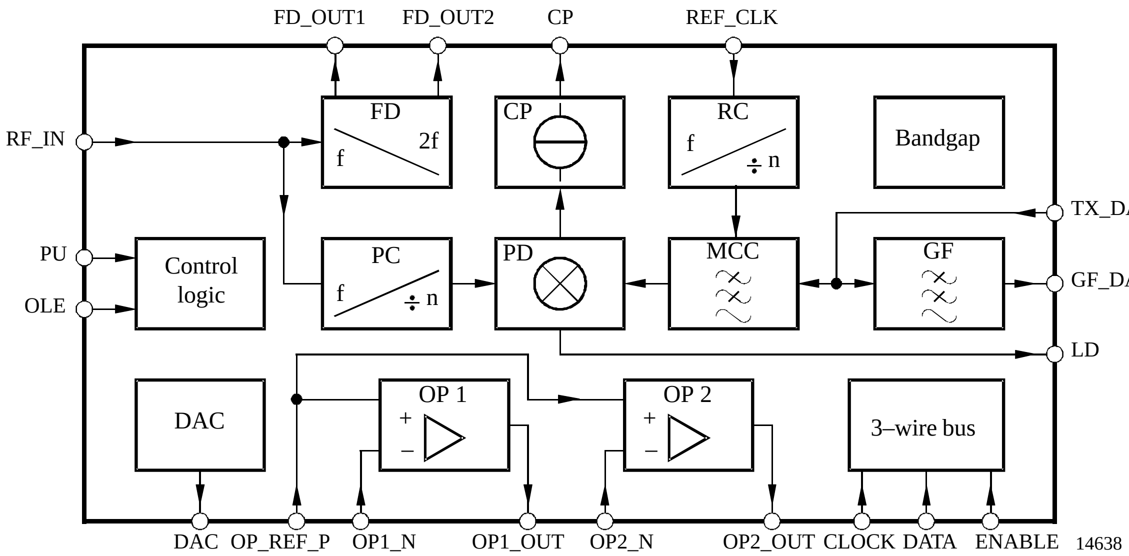


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U2785B-MFS	SSO28	Tube
U2785B-MFSG3	SSO28	Taped and reeled

Preliminary Information

Pin Description

Pin	Symbol	Function
1	CLOCK	3-wire bus: clock input
2	DATA	3-wire bus: data input
3	ENABLE	3-wire bus: enable input
4	REF_CLK	Reference frequency input
5	LD	Lock-detect output
6	I_CP_SW	Charge-pump current switch
7	GND_FD_ OUT	Frequency doubler buffer ground
8	FD_OUT1	Frequency doubler buffer output
9	FD_OUT2	
10	VS	Supply voltage
11	GF_DATA	Modulation output (Gaussian-filtered data signal)
12	GND_CP	Charge-pump ground
13	VS_CP	Charge-pump supply voltage
14	CP	Charge-pump output
15	OP1_N	Operational amplifier 1 inverting input
16	OP_REF_P	Operational amplifier reference voltage (internal)
17	OP1_OUT	Operational amplifier 1 output
18	GND_OP	Operational amplifier ground
19	OP2_N	Operational amplifier 2 inverting input
20	OP2_OUT	Operational amplifier 2 output
21	VCO_BIAS	VCO bias voltage output
22	GND_RF_IN	RF input ground
23	RF_IN	RF input from VCO to doubler and PLL
24	DAC	DAC for VCO pretune
25	GND_D	Digital ground
26	OLE	Open-loop enable input
27	PU	Power-up input (active high)
28	TX_DATA	Digital TX data input to Gaussian filter and modulation-compensation circuit

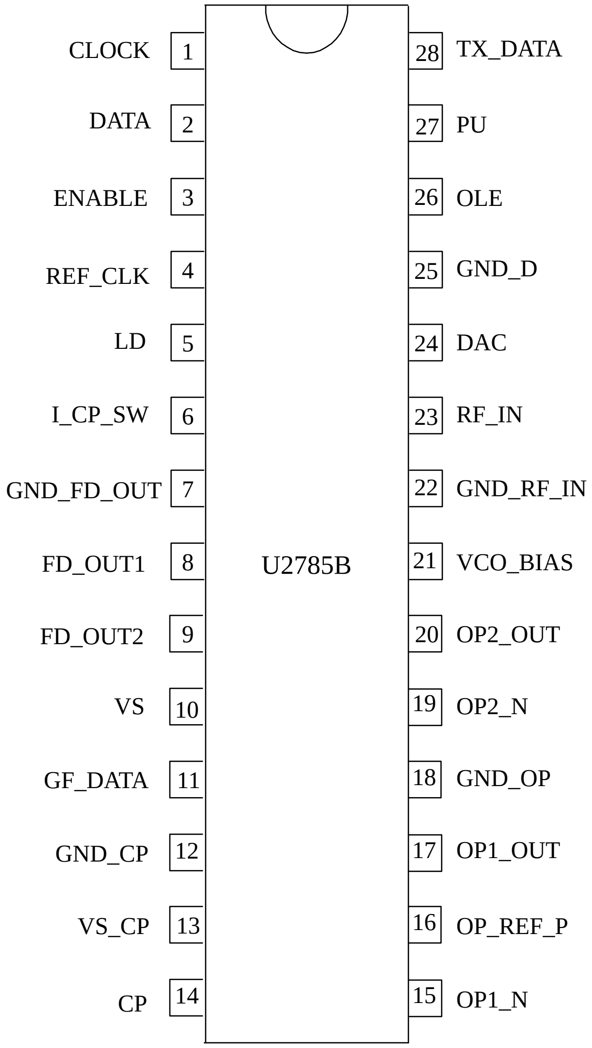


Figure 2. Pinning

Functional Blocks

CP	Charge pump
DAC	D/A converter for pretuning the VCO
FD	Frequency doubler
GF	Gaussian filter for transmit data
OP1	1st amplifier for loop filter
OP2	2nd amplifier for loop filter
MCC	Modulation-compensation circuit
PC	Programmable counter = main counter (MC) + swallow counter (SC)
PD	Phase detector
RC	Reference counter
VCO	Voltage-controlled oscillator

Absolute Maximum Ratings

All voltages refer to GND (Pins 7, 12, 18, 22 and 25)

Parameter		Symbol	Value	Unit
Supply voltage	Pins 10, 13	V_S	5.0	V
Logic input voltage	Pins 1, 2, 3, 6, 26, 27 and 28	V_{IN}	–0.3 to V_S	V
Junction temperature		T_j	150	°C
Storage temperature		T_{stg}	–40 to +150	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction ambient	R_{thJA}	130	K/W

Operating Range

All voltages refer to GND (Pins 7, 12, 18, 22 and 25)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_S	2.7	3.0	4.7	V
Ambient temperature	T_{amb}	–25	+25	+85	°C

Electrical Characteristics

Test conditions (unless otherwise specified) : V_S = 3 V, T_{amb} = 25°C

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power supply	**Pin 10**					
Supply current	V_{PU} = low level = '0'	$I_{S,OFF}$		1	10	µA
	RX (OLE = '1')	I_S		5.6		mA
	TX (OLE = '0')	I_S		13		mA
	TX, MCC ON	I_S		15		mA
	TX, MCC, GF ON	I_S		17		mA
	TX, MCC, GF, OP ON	I_S		19		mA
	TX, MCC, GF, OP, FD ON	I_S		30		mA
Supply current CP	V_{VS_CP} = 3 V, PLL in lock condition, Pin 14	I_{CP}		1		µA
Frequency doubler	**f_{RF_IN} = 900 MHz**					
Output power	P_{RF_IN} = –10 dBm, Z_{load} = 50 Ω (differential), Pins 8 and 9 (differential)	P_{FD_OUT}	– 10	– 5	– 3	dBm
Harmonic suppression	P_{RF_IN} = –10 dBm, 2nd and 3rd, Pin 8 and 9 (differential)	HS	– 20			dBc
Subharmonic suppression	P_{RF_IN} = –10 dBm, Pin 8 and 9 (differential)	SHS	– 20			dBc
PLL						
Input frequency	Pin 23	f_{RF_IN}	800		1000	MHz
Input voltage	f_{RF_IN} = 800 to 1000 MHz AC-coupled sine wave Pin 23	V_{RF_IN}	20		200	mV_{rms}
Scaling factor prescaler		S_{PSC}	–	32/33	–	
Scaling factor main counter		S_{MC}	–	31/32/ 33/34	–	
Scaling factor swallow counter		S_{SC}	0		31	
Scaling factor reference counter	Pin 4	S_{RC}	–	12/16/ 24	–	
External reference input frequency	AC-coupled sine wave Pin 4	f_{REF_CLK}	5	10.368 20.736	22	MHz
External reference input voltage	AC-coupled sine wave Pin 4	V_{REF_CLK}	50		250	mV_{rms}

Electrical Characteristics (continued)

Test conditions (unless otherwise specified) : V_S = 3 V, T_{amb} = 25°C

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Charge pump, active when RX, TX Pin 14						
Output current	CPCS = 100%, $V_{I\_CP\_SW}$ = ’0‘, $V_{CP} = V_{VS\_CP}$ / 2	I_{CP_NOM1}		± 1		mA
	CPCS = 100%, $V_{I\_CP\_SW}$ = ’1‘, $V_{CP} = V_{VS\_CP}$ / 2	I_{CP_NOM5}		± 5		mA
Current scaling factor	See bus protocol D0...D2 $I_{CP} = CPCS \times I_{CP\_NOM}$	CPCS	60		130	%
Leakage current		I_{CP_O}		±100		pA
Operational amplifiers 1 and 2						
Power gain bandwidth	Pins 17 and 20	PGBW		10		MHz
Excess phase	R_{load} = 1 kΩ, C_{load} = 15 pF Pins 17 and 20	δ		80		degree
Input offset voltage	Pins 15, 16 and 19	V_{offs}		± 1		mV
Open-loop gain	Pins 17 and 20	g		70		dB
Output-voltage range	Pins 17 and 20	V_{out}	0.3		V_S – 0.3	V
Common-mode input voltage	Pins 15, 16 and 19	V_{in}	0.3		V_S – 0.3	V
Modulation-compensation circuit @ max. DSV 64						
Oversampling	f_{REF_CLK} = 10.368 MHz or f_{REF_CLK} = 20.736 MHz	OVS	–	9	–	
Integration counter		MAC	– 576		576	
Current scaling factor	See bus protocol E3 ... E5	MCCS	60		130	%
Gaussian transmit filter (Gaussian shape B × T = 0.5) f_{REF_CLK} has to be chosen						
TX data filter clock	f_{REF_CLK} = 10.368 MHz, TX, 18 taps in filter, S_{RC} = 12	f_{TXFCLK}	–	10.368	–	MHz
	f_{REF_CLK} = 20.736 MHz, TX, 18 taps in filter, S_{RC} = 24	f_{TXFCLK}	–	10.368	–	MHz
Maximum output current	Polarity see bus protocol D13, GFCS = 100%, Pin 11	$\|I_{GF\_NOM}\|$		80		µA
Current scaling factor	See bus protocol D6 ... D8 $I_{GF\_DATA} = GFCS \times I_{GF\_NOM}$ Pin 11	GFCS	60		130	%
VCO biasing Pin 21						
Bias voltage		V_{VCO}		1.5		V
	Standby, PU = ’0‘	V_{VCO_O}			10	mV
Temperature coefficient		TC_{VCO}		– 3.3		mV/K

Preliminary Information

Electrical Characteristics (continued)

Test conditions (unless otherwise specified) : V_S = 3 V, T_{amb} = 25°C

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
DAC for VCO pretune, 3-bit programming, see bus protocol D3 ... D5 Pin 24						
DAC low level	I_{load} = 1 µA	V_{DAC_min}		0.3		V
DAC step level	I_{load} = 1 µA	V_{DAC_step}		0.3		V
DAC high level	I_{load} = 1 µA	V_{DAC_max}		2.3		V
Output impedance		R_{DAC_out}		10		kΩ
Lock-detect and test-mode output Pin 5						
Lock-detect output	Locked = ’1‘, unlocked = ’0‘	LD	–	–	–	
Test-mode output	Test modes see bus protocol E0 ... E2	LD	–	–	–	
Leakage current	V_{OH} = 4.5 V	I_{LD_O}			5	µA
Saturation voltage	I_{OL} = 0.5 mA	V_{LD_min}			0.4	V
3-wire bus Pin 1						
Clock		f_{clock}		1.152		MHz
Logic input levels (CLOCK, DATA, ENABLE, I_CP_SW, OLE, GF_DATA) Pins 1, 2, 3, 6, 26 and 28						
High input level	= ’1‘	V_{iH}	1.5			V
Low input level	= ’0‘	V_{iL}			0.5	V
High input current	= ’1‘	I_{iH}	–5		5	µA
Low input current	= ’0‘	I_{iL}	–5		5	µA
Standby control Pin 27						
Power-up high input level	PU = ’1‘	V_{PU}	2.0			V
Power-up low input level	PU = ’0‘ (standby)	V_{PU_O}			0.7	V
Power-up high input current	V_{PU} = 3 V, PU = ’1‘ V_{PU} = 4.5 V	I_{PU}	100 220	125 300	150 420	µA
Power-up low input current	V_{PU} = 0 V, PU = ’0‘ V_{PU} = 0.5 V	I_{PU_O}			0.1 1	µA
Settling time V_S = 0 –> active operation	Switched from V_S = 0 to V_S = 3 V	t_{soa}			10	µs
Settling time standby–> active operation	Switched from standby to PU = ’1‘	t_{ssa}			10	µs
Settling time active operation–> standby	Switched from PU = ’1‘ to standby	t_{sas}			2	µs

PLL Principle

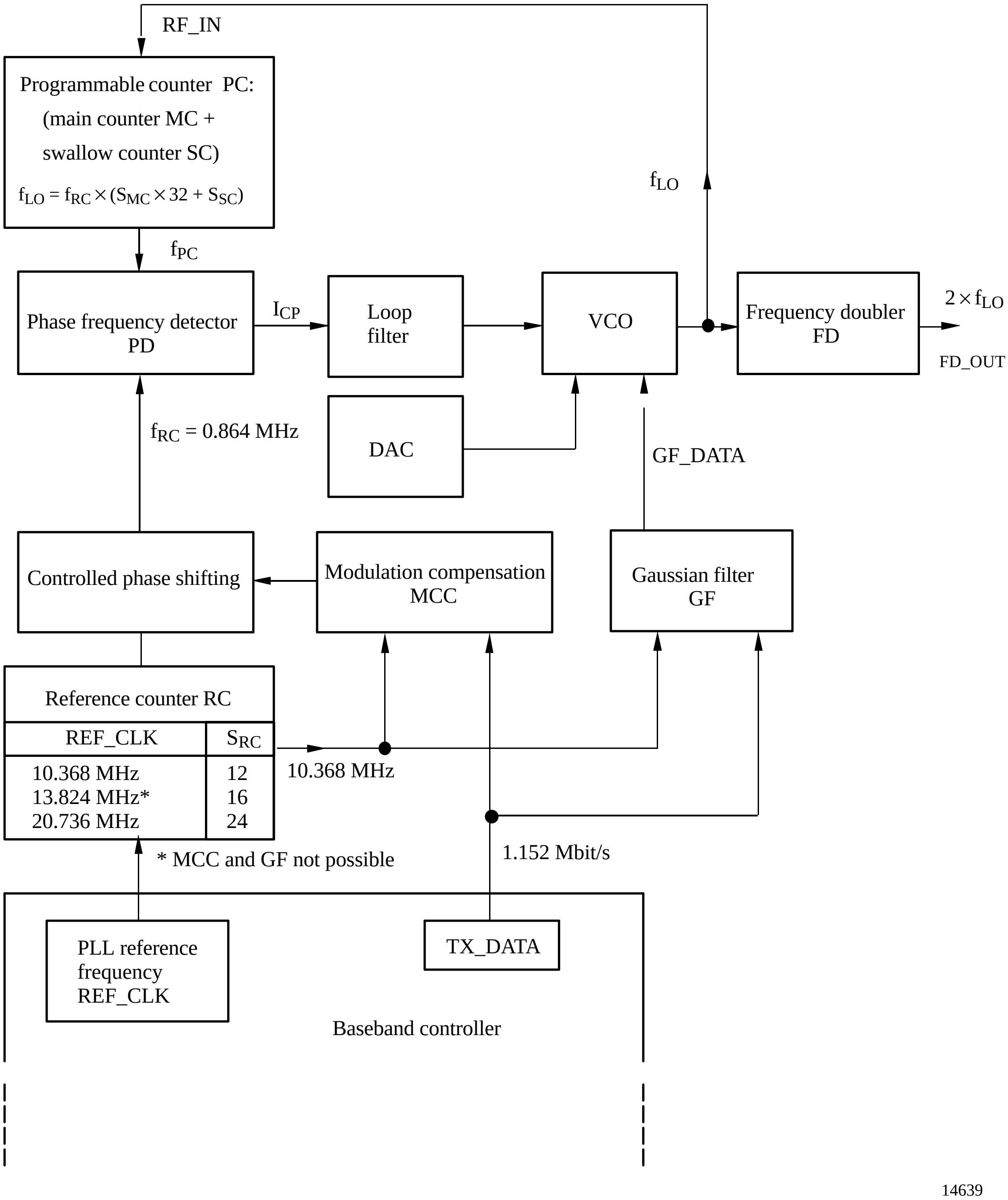


Figure 3. PLL principle

The following table shows the LO frequencies for RX and TX for the DECT band plus additional channels for an optional DECT band extension. Intermediate frequencies of 110.592 and 112.32 MHz are supported.

Mode	f_{IF} (MHz)	Channel	f_{ANT} (MHz)	f_{LO} (MHz)	$2f_{LO}$ (MHz)	S_{MC}	S_{SC}
TX		CO	1897.344	948.672	1897.344	34	10
		C1	1895.616	947.808	1895.616	34	9
		C2	1893.888	946.944	1893.888	34	8
		C3	1892.16	946.08	1892.16	34	7
		C4	1890.432	945.216	1890.432	34	6
		C5	1888.704	944.352	1888.704	34	5
		C6	1886.976	943.488	1886.976	34	4
		C7	1885.248	942.624	1885.248	34	3
		C8	1883.52	941.76	1883.52	34	2
		C9	1881.792	940.896	1881.792	34	1
RX	110.592	CO	1897.344	893.376	1786.752	32	10
		C1	1895.616	892.512	1785.024	32	9
		C2	1893.888	891.648	1783.296	32	8
		C3	1892.16	890.784	1781.568	32	7
		C4	1890.432	889.92	1779.84	32	6
		C5	1888.704	889.056	1778.112	32	5
		C6	1886.976	888.192	1776.384	32	4
		C7	1885.248	887.328	1774.656	32	3
		C8	1883.52	886.464	1772.928	32	2
		C9	1881.792	885.6	1771.2	32	1
	112.32	CO	1897.344	892.512	1785.024	32	9
		C1	1895.616	891.648	1783.296	32	8
		C2	1893.888	890.784	1781.568	32	7
		C3	1892.16	889.92	1779.84	32	6
		C4	1890.432	889.056	1778.112	32	5
		C5	1888.704	888.192	1776.384	32	4
		C6	1886.976	887.328	1774.656	32	3
		C7	1885.248	886.464	1772.928	32	2
		C8	1883.52	885.6	1771.2	32	1
		C9	1881.792	884.792	1769.472	32	0

Limits

Mode	f_{IF} (MHz)		f_{ANT} (MHz)	f_{LO} (MHz)	$2f_{LO}$ (MHz)	S_{MC}	S_{SC}
TX		f_{min}	1714.176	857.088	1714.176	31	0
RX	110.592		1824.768	857.088	1714.176	31	0
	112.32		1826.496	857.088	1714.176	31	0
TX		f_{max}	1933.632	966.816	1933.623	34	31
RX	110.952		2044.224	966.816	1933.623	34	31
	112.32		2045.952	966.816	1933.623	34	31

Formulas

$f_{ANT\,C1} - f_{ANT\,C2} = 1.728$ MHz

for TX: $f_{LO} = f_{ANT} / 2$
for RX: $f_{LO} = (f_{ANT} - f_{IF}) / 2$
S_{MC} = integer (f_{FD} / 0.864 MHz / 32)
S_{SC} = MOD ((f_{FD} / 0.864 MHz) / 32)

Control Signals

I_CP_SW	input for switching charge-pump current by factor 5
LD	output which is active after PLL is locked and test-mode output (according to programmed test mode)
OLE	enable input for open-loop modulation
DAC	DAC for VCO band switch
PU	hardware power-up / standby of complete PLL / TX IC

Serial Programming Bus

Reference and programmable counters can be programmed by the 3-wire bus (CLOCK, DATA and ENABLE). Besides this information, additional control bits as phase-detector polarity and scaling of charge-pump currents as well as internal currents for Gaussian lowpass filter and modulation-compensation circuit can be transferred.

After setting the enable signal to low condition, the data status is transferred bit-by-bit on the rising edge of the clock signal into the shift register, starting with the MSB bit. When the enable signal has returned to high condition, the programmed information is loaded into the addressed latches according to the address-bit condition (last bit). Additional leading bits are ignored and there is no check carried out how many pulses arrived during enable low condition. The bus then returns to low-current standby mode until the enable signal changes to low again.

During standby of the PLL, the information in the registers of the PLL is not maintained.

Bus Protocol Formats

MSB																							LSB
Data bits																							Address bit
D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A0
RC		SC					MC		PS			GF	MCC	GFCS			DAC			CPCS			1
0	1	0	1	0	1	0	1	1	0	0	0	1	1	1	0	0	1	1	1	1	0	0	1
															FD	OP	MCCS			TEST			0
															1	1	1	0	0	0	0	0	0

Standard bit setting: word 1 (upper rows)

word 2 (lower rows)

PLL Settings

RC (Reference Divider)		
D22	D21	S_{CR}
0	0	–
0	1	12
1	0	16
1	1	24

MC (Main Divider)		
D15	D14	S_{MC}
0	0	31
0	1	32
1	0	33
1	1	34

SC (Swallow Counter)					
D20	D19	D18	D17	D16	S_{SC} 1)
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
1	1	1	1	0	30
1	1	1	1	1	31

$S_{PGD} = 32 \times S_{MC} + S_{SC}$

1) $S_{SC} = [D16] \times 2^0 + [D17] \times 2^1 + ... + [D20] \times 2^4$

Phase Settings

Phase of GF_DATA	
D13	GF_DATA
0	Source
1	Sink

Phase of MCC Internal Connection	
D12	MCC_DATA
1	Normal
0	Inverted

Phase of CP (Charge Pump)			
D11	$f_R > f_P$	$f_R < f_P$	$f_R = f_P$
1	I_{Source}	I_{Sink}	High imp.
0	I_{Sink}	I_{Source}	High imp

Current-Saving Power-up/ down Settings

D10	GF (Gaussian Filter)
0	off
1	on

D9	MCC (Modulation-Compensation Circuit)
0	off
1	on

E7	FD (Frequency Doubler)
0	off
1	on

E6	OP1 + OP2 (Op Amps)
0	off
1	on

Current Gain Settings

GFCS (Gaussian-Filter Current Settings)			
D8	D7	D6	GFCS
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

CPCS (Charge-Pump Current Settings)			
D2	D1	D0	CPCS
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

MCCS (Modulation-Compensation Current Settings)			
E5	E4	E3	MCCS
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

Pretune DAC Voltage Settings

Pretune DAC Voltage			
D5	D4	D3	DAC
0	0	0	0.3 V
0	0	1	0.6 V
0	1	0	0.9 V
0	1	1	1.2 V
1	0	0	1.4 V
1	0	1	1.7 V
1	1	0	2.0 V
1	1	1	2.3 V

Test Mode Settings

Test Output Pin LD (Lock Detect)					
D11	E2	E1	E0	Signal at Lock Detect Output	CP Mode
x	0	0	0	Lock detect	Active
0	0	0	1	RC out	Active
1	0	1	0	PC out	Active
x	0	1	1	RC out div. by 2048 (MCCTEST)	Active
x	1	0	0	CP tristate only	High impedance
0	1	0	1	RC out	High impedance
1	1	1	0	PC out	High impedance
x	1	1	1	RC out div. by 2 (GFTEST)	High impedance

3-Wire Bus Protocol

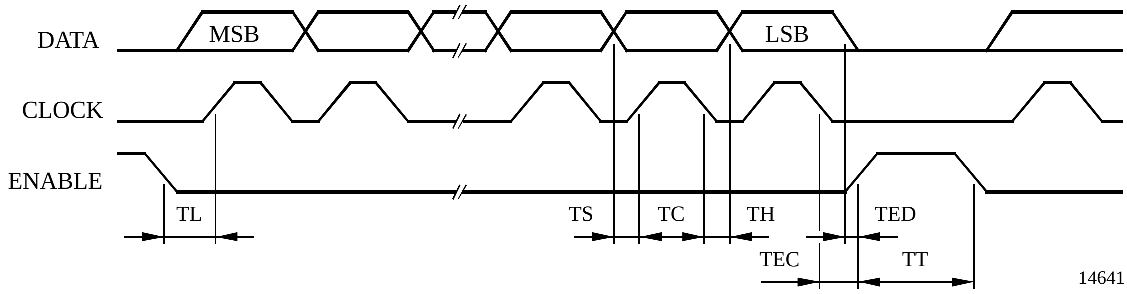


Figure 4. 3-wire bus protocol timing diagram

Parameters	Symbol	Min. Value	Unit
Set time data to clock	TS	434	ns
Hold time data to clock	TH	0	ns
Clock pulse width	TC	434	ns
Set time enable to clock	TL	217	ns
Hold time enable to clock	TEC	0	ns
Hold time enable to data	TED	0	ns
Time between two protocols	TT	868	ns

Typical Application Circuit

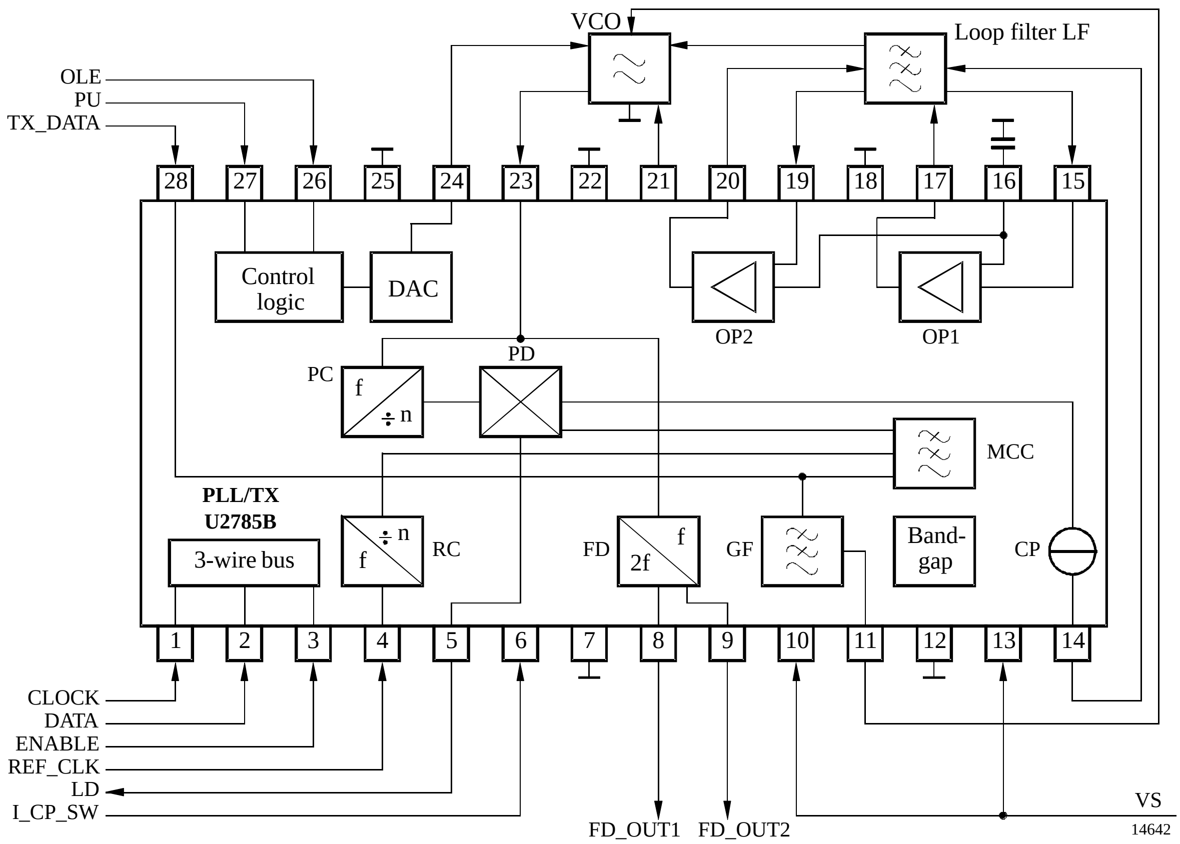


Figure 5. Typical application circuit

Input / Output Interface Circuits

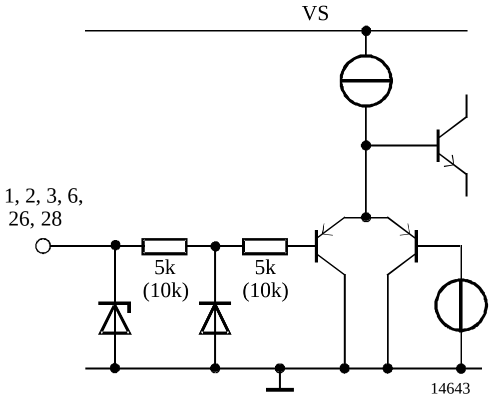


Figure 6.

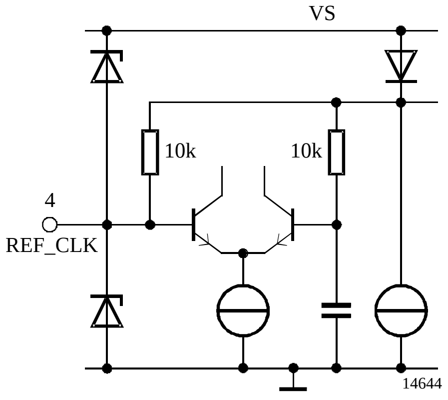


Figure 9.

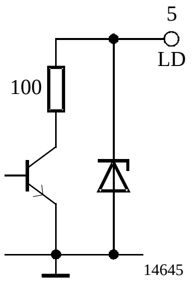


Figure 7.

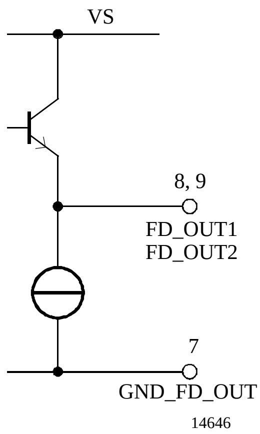


Figure 10.

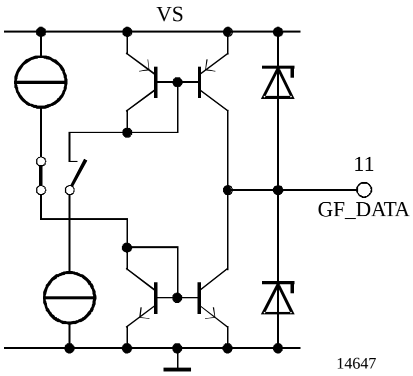


Figure 8.

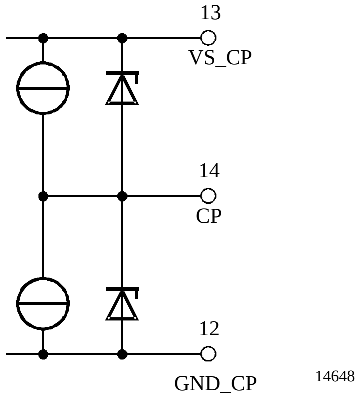


Figure 11.

Input / Output Interface Circuits (continued)

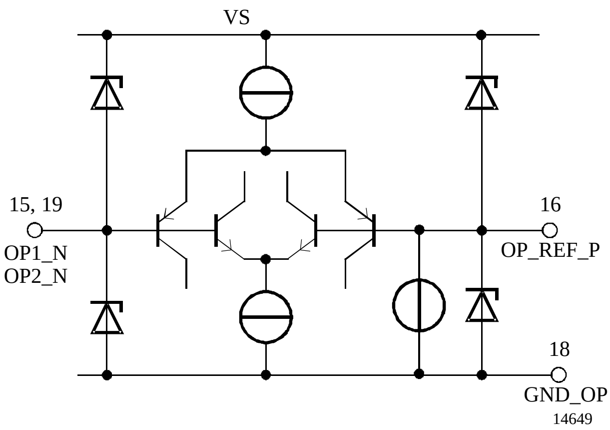


Figure 12.

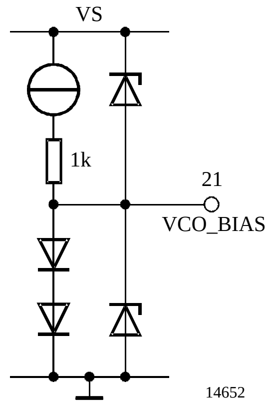


Figure 15.

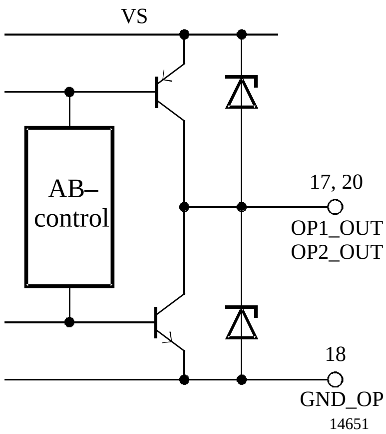


Figure 13.

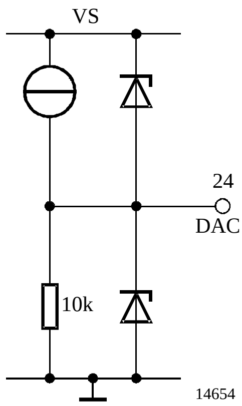


Figure 16.

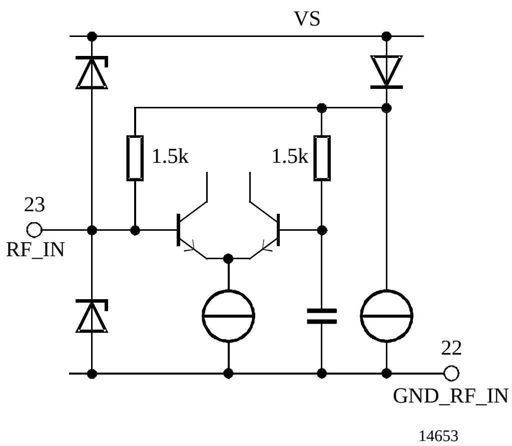


Figure 14.

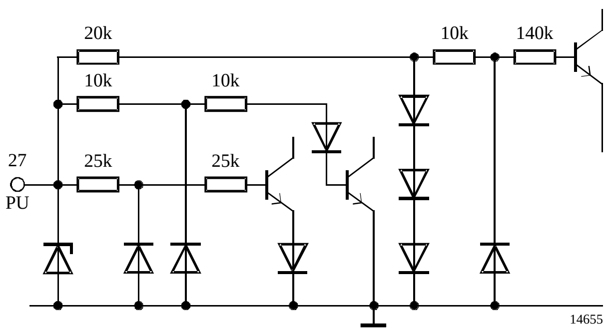


Figure 17.

Input / Output Interface Circuits (continued)

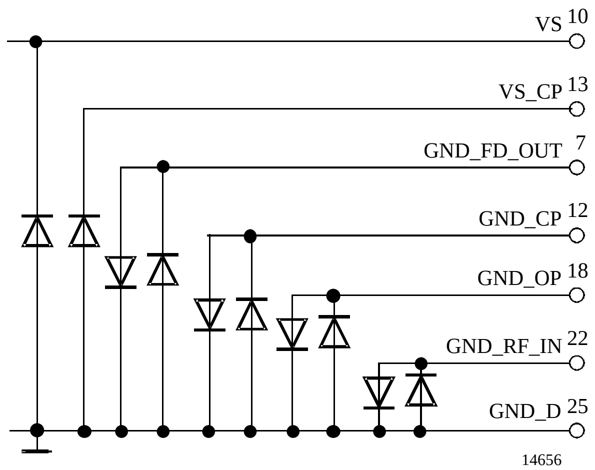
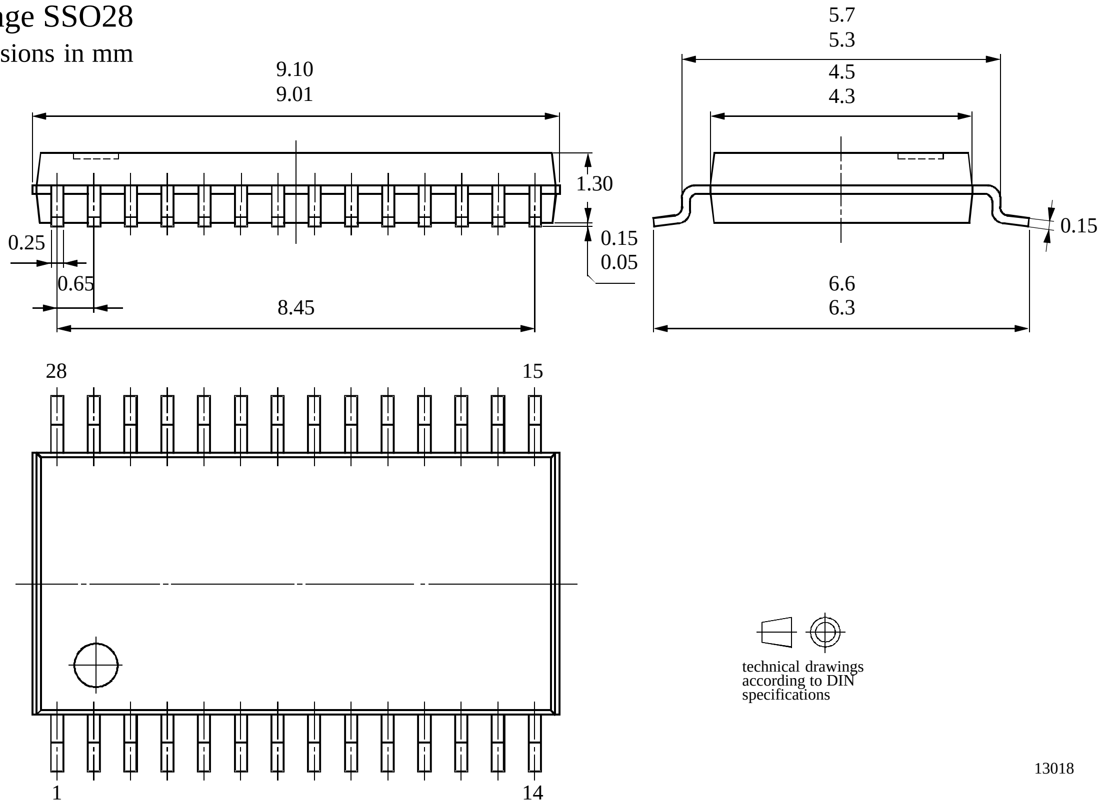


Figure 18.

Package Information

Package SSO28

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Data sheets can also be retrieved from the Internet: http://www.temic–semi.com

TEMIC Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2594, Fax number: 49 (0)7131 67 2423