Phase-Control IC – Tacho Applications

Description

The integrated circuit U209B is designed as a phase-control circuit in bipolar technology with an internal frequency-voltage converter. Furthermore, it has an internal open-loop amplifier which means it can be used for motor speed control with tacho feedback.

The U209B is a 14-pin shrink version of the U211B with reduced features. Using the U209B, the designer is able to realize sophisticated as well as economic motor control systems.

Features

- Internal frequency-to-voltage converter
- Externally controlled integrated amplifier
- Automatic soft start with minimized “dead time”
- Voltage and current synchronization
- Retriggering
- Triggering pulse typ. 155 mA
- Internal supply-voltage monitoring
- Temperature-compensated reference source
- Current requirement ≤ 3 mA

Block Diagram

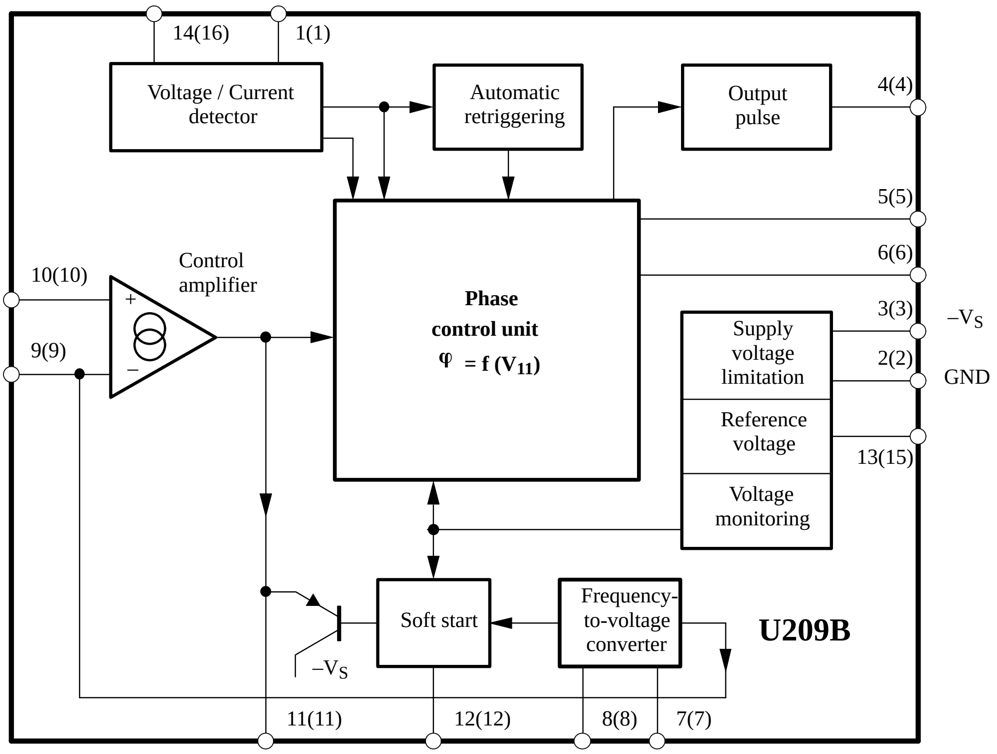


Figure 1. Block diagram (Pins in brackets refer to SO16)

Ordering Information

Extended Type Number	Package	Remarks
U209B-x	DIP14	Tube
U209B-xFP	SO16	Tube
U209B-xFPG3	SO16	Taped and reeled

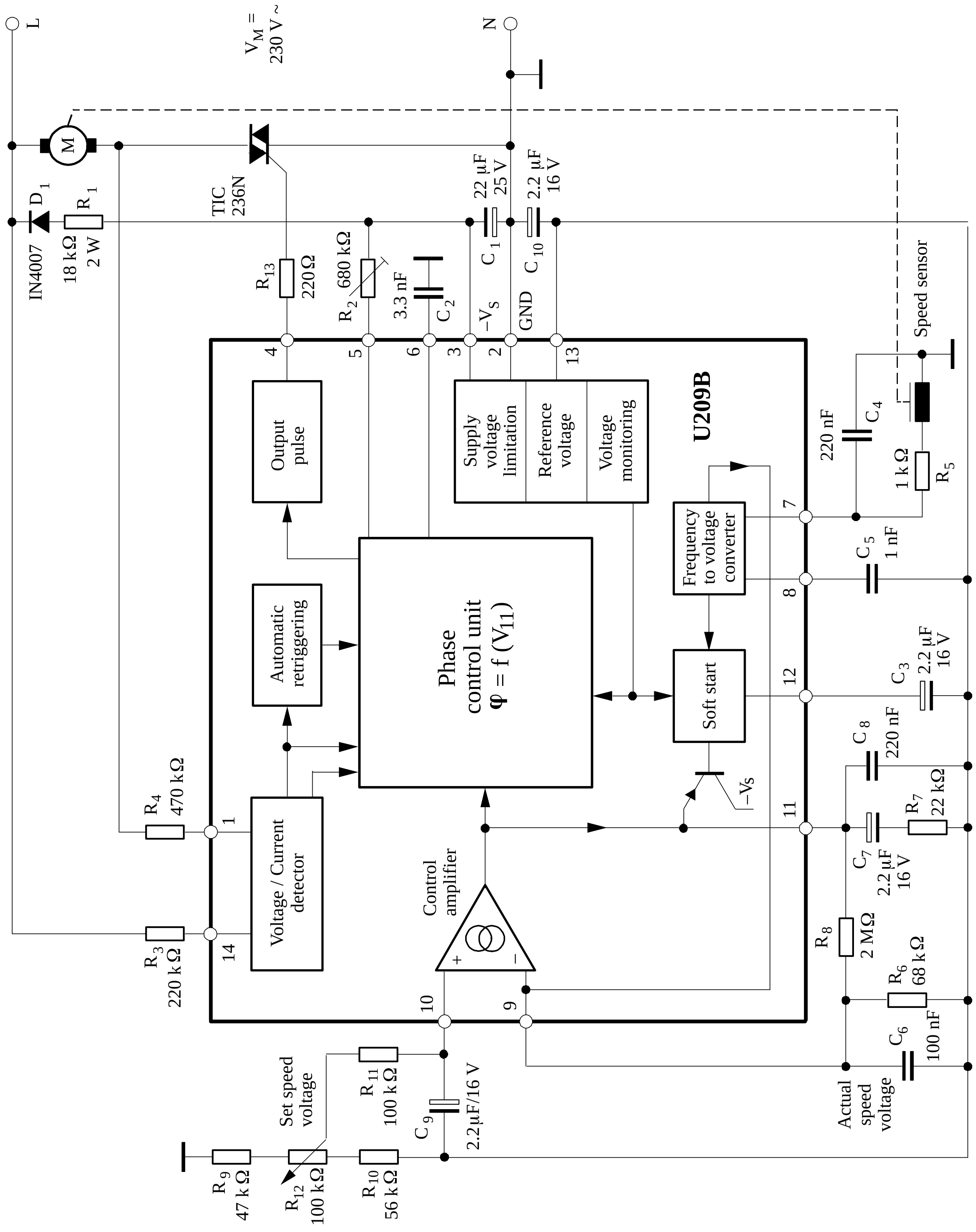


Figure 2. Block diagram with typical circuitry for speed regulation

Description

Mains Supply

The U209B is designed with voltage limiting and can therefore be supplied directly from the mains. The supply voltage between Pin 2 (+ pol/⊥) and Pin 3 builds up across D_1 and R_1 and is smoothed by C_1. The value of the series resistance can be approximated using:

$$R_1 = \frac{V_M - V_S}{2\ I_S}$$

Further information regarding the design of the mains supply can be found in the chapter "Design Calculations for Mains Supply". The reference voltage source on Pin 13 of typ. –8.9 V is derived from the supply voltage and represents the reference level of the control unit.

Operation using an externally stabilised DC voltage is not recommended.

If the supply cannot be taken directly from the mains because the power dissipation in R_1 would be too large, then the circuit shown in the following figure 3 should be employed.

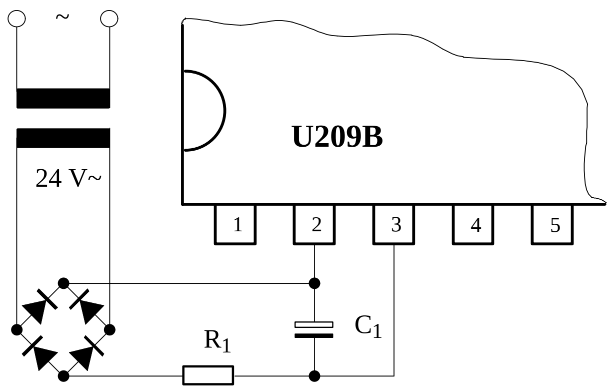


Figure 3. Supply voltage for high current requirements

Phase Control

The function of the phase control is largely identical to that of the well known integrated circuit U2008B. The phase angle of the trigger pulse is derived by comparing the ramp voltage. This is mains-synchronized by the voltage detector with the set value on the control input Pin 4. The slope of the ramp is determined by C_2 and its charging current. The charging current can be varied using R_2 on Pin 5. The maximum phase angle α_{max} can also be adjusted using R_2.

When the potential on Pin 6 reaches the nominal value predetermined at Pin 11, a trigger pulse is generated whose width t_p is determined by the value of C_2 (the value of C_2 and hence the pulse width can be evaluated by assuming 8 µs/nF).

The current sensor on Pin 1 ensures that no pulse is generated (for operation with inductive loads) in a new half cycle as long as the current from the previous half cycle is still flowing in the opposite direction to the supply voltage at that instant. This makes sure that "Gaps" in the load current are prevented.

The control signal on Pin 11 can be in the range 0 V to –7 V (reference point Pin 2).

If V_{11} = –7 V, the phase angle is at maximum = α_{max}, i.e., the current flow angle is a minimum. The minimum phase angle α_{min} is when $V_{11} = V_{pin2}$.

Voltage Monitoring

As the voltage is built up, uncontrolled output pulses are avoided by internal voltage surveillance. At the same time, all latches in the circuit (phase control, soft start) are reset and the soft-start capacitor is short circuited. Used with a switching hysteresis of 300 mV, this system guarantees defined start-up behaviour each time the supply voltage is switched on or after short interruptions of the mains supply.

Soft Start

As soon as the supply voltage builds up (t_1), the integrated soft start is initiated. Figure 4 shows the behaviour of the voltage across the soft-start capacitor which is identical with the voltage on the phase control input on Pin 11. This behaviour guarantees a gentle start-up for the motor and automatically ensures the optimum run-up time.

C_3 is first charged up to the starting voltage V_o with typically 30 µA current (t_2). By then reducing the charging current to approx. 4 µA, the slope of the charging function is substantially reduced so that the rotational speed of the motor only slowly increases. The charging current then increases as the voltage across C_3 increases giving a progressively rising charging function which accelerates the motor with increasing rotational speed. The charging function determines the acceleration up to the set-point. The charging current can have a maximum value of 50 µA.

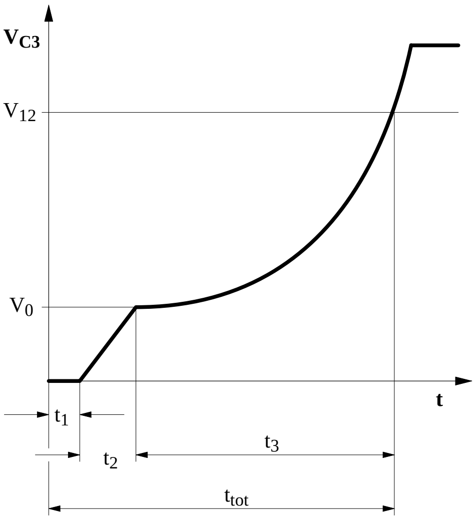


Figure 4. Soft start

t_1 = build-up of supply voltage
t_2 = charging of C_3 to starting voltage
$t_1 + t_2$ = dead time
t_3 = run-up time
t_{tot} = total start-up time to required speed

Frequency-to-Voltage Converter

The internal frequency-to-voltage converter (f/V-converter) generates a DC signal on Pin 9 which is proportional to the rotational speed using an AC signal from a tacho generator or a light beam whose frequency is in turn dependent on the rotational speed. The high impedance input with a switch-on threshold of typ. –100 mV gives very reliable operation even when relatively simple tacho generators are employed. The tacho frequency is given by:

$$f = \frac{n}{60} \; p[Hz]$$

n = revolutions per minute

p = number of pulses per revolution

The converter is based on the charge pumping principle. With each negative half wave of the input signal, a quantity of charge determined by C_5 is internally amplified and then integrated by C_6 at the converter output on Pin 9. The conversion constant is determined by C_5, its charging voltage of V_{ch}, R_6 (Pin 9) and the internally adjusted charge amplification G_i.

$k = G_i \times C_5 \times R_6 \times V_{ch}$

The analog output voltage is given by

$V_o = k \times f$

where: $V_{ch} = 6.7$ V

$G_i = 8.3$

The values of C_5 and C_6 must be such that for the highest possible input frequency, the maximum output voltage V_0 does not exceed 6 V. The R_i on Pin 8 is approx. 6 kΩ while C_5 is charging up. To obtain good linearity of the f/V converter the time constant resulting from R_i and C_5 should be considerably less (1/5) than the time span of the negative half cycle for the highest possible input frequency. The amount of remaining ripple on the output voltage on Pin 9 is dependent on C_5, C_6 and the internal charge amplification.

$$\Delta V_O = \frac{G_i \times V_{ch} \times C_5}{C_6}$$

The ripple ΔV_o can be reduced by using larger values of C_6, however, the maximum conversion speed will then also be reduced.

The value of this capacitor should be chosen to fit the particular control loop where it is going to be used.

Control Amplifier

The integrated control amplifier with differential input compares the set value (Pin 10) with the instantaneous value on Pin 9 and generates a regulating voltage on the output Pin 11 (together with external circuitry on Pin 12) which always tries to hold the real voltage at the value of the set voltages. The amplifier has a transmittance of typically 110 μA/V and a bipolar current source output on Pin 11 which operates with typically ±100 μA. The amplification and frequency response are determined by R_7, C_7, C_8 and R_8 (can be left out). For operation as a power divider, C_4, C_5, R_6, C_6, R_7, C_7, C_8 and R_8 can be left out. Pin 9 should be connected with Pin 11 and Pin 7 with Pin 2. The phase angle of the triggering pulse can be adjusted using the voltage on Pin 10. An internal limiting circuit prevents the voltage on Pin 11 from becoming more negative than V_{13} + 1 V.

Pulse-Output Stage

The pulse-output stage is short-circuit protected and can typically deliver currents of 125 mA. For the design of smaller triggering currents, the function $I_{GT} = f(R_{GT})$ can be taken from figure 14.

Automatic Retriggering

The automatic retriggering prevents half cycles without current flow, even if the triacs are turned off earlier e.g., due to not exactly centered collector (brush lifter) or in the event of unsuccessful triggering. If necessary, another triggering pulse is generated after a time lapse of $t_{PP} = 4.5\, t_P$ and this is repeated until either the triac fires or the half cycle finishes.

General Hints and Explanation of Terms

To ensure safe and trouble-free operation, the following points should be taken into consideration when circuits are being constructed or in the design of printed circuit boards.

- The connecting lines from C_2 to Pin 6 and Pin 2 should be as short as possible, and the connection to Pin 2 should not carry any additional high current such as the load current. When selecting C_2, a low temperature coefficient is desirable.
- The common (earth) connections of the set-point generator, the tacho-generator and the final interference suppression capacitor C_4 of the f/V converter should not carry load current.
- The tacho generator should be mounted without influence by strong stray fields from the motor.

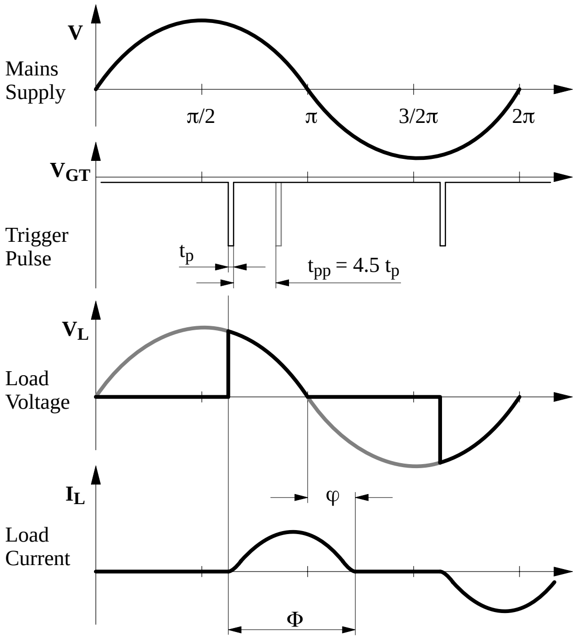


Figure 5. Explanation of terms in phase relationship

Design Calculations for Mains Supply

The following equations can be used for the evaluation of the series resistor R_1 for worst case conditions:

$$R_{1max} = 0.85 \frac{V_{Mmin} - V_{Smax}}{2\ I_{tot}} \qquad R_{1min} = 0.85 \frac{V_M - V_{Smin}}{2\ I_{Smax}}$$

$$P_{(R1max)} = \frac{(V_{Mmax} - V_{Smin})^2}{2\ R_1}$$

where:

V_M = Mains voltage 230 V
V_S = Supply voltage on Pin 3
I_{tot} = Total DC current requirement of the circuit
= $I_S + I_p + I_x$
I_{Smax} = Current requirement of the IC in mA
I_p = Average current requirement of the triggering pulse
I_x = Current requirement of other peripheral components

R_1 can be easily evaluated from figures 15 to 17

Absolute Maximum Ratings

Reference point Pin 2, unless otherwise specified

Parameters			Symbol	Value	Unit
Current requirement		Pin 3	$-I_S$	30	mA
	$t \leq 10$ µs		$-i_S$	100	mA
Synchronization current		Pin 1	I_{syncI}	5	mA
		Pin 14	I_{syncV}	5	mA
	$t < 10$ µs	Pin 1	$\pm i_i$	35	mA
	$t < 10$ µs	Pin 14	$\pm i_v$	35	mA
f/V converter:					
Input current		Pin 7	I_{eff}	3	mA
	$t < 10$ µs		$\pm i_i$	13	mA
Phase control:		Pin 11			
Input voltage			$-V_I$	0 to 7	V
Input current			$\pm I_I$	500	µA
Soft start:					
Input voltage		Pin 12	$-V_I$	$\lvert V_{13}\rvert$ to 0	V
Pulse output:					
Reverse voltage		Pin 4	V_R	V_S to 5	V
Amplifier					
Input voltage		Pin 10	$-V_I$	$\lvert V_S\rvert$	
Pin 8 open		Pin 9	$-V_I$	$\lvert V_{13}\rvert$ to 0	V
Reference voltage source					
Output current		Pin 13	I_o	7.5	mA
Power dissipation		$T_{amb} = 45°C$	P_{tot}	570	mW
		$T_{amb} = 80°C$		320	mW
Storage temperature range			T_{stg}	–40 to +125	°C
Junction temperature			T_j	125	°C
Ambient temperature range			T_{amb}	–10 to +100	°C

Thermal Resistance

Parameters		Symbol	Maximum	Unit
Junction ambient	DIP14	R_{thJA}	140	K/W
	SO16: on p.c. board	R_{thJA}	180	K/W
	SO16: on ceramic substrate	R_{thJA}	100	K/W

Electrical Characteristics

$-V_S$ = 13.0 V, T_{amb} = 25°C, reference point Pin 2, unless otherwise specified

Parameters	Test Conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Supply voltage for mains operations	Pin 3	$-V_S$	13.0		V_{Limit}	V
Supply voltage limitation	$-I_S$ = 3 mA Pin 3	$-V_S$	14.6		16.6	V
	$-I_S$ = 30 mA		14.7		16.8	V
DC supply current	$-V_S$ = 13.0 V Pin 3	$-I_S$	1.1	2.5	3.0	mA
Reference voltage source	$-I_L$ = 10 µA Pin 13	V_{Ref}	8.6	8.9	9.2	V
	$-I_L$ = 5 mA		8.3		9.1	V
Temperature coefficient	Pin 13	TC_{VRef}			0.5	mV/K

Parameters	Test Conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Voltage monitoring Pin 3						
Turn-on threshold		$-V_{TON}$		11.2	13	V
Turn-off threshold		$-V_{TOFF}$	9.9	10.9		V
Phase-control currents						
Current synchronization	Pin 1	$\pm I_{syncI}$	0.35		2.0	mA
Voltage synchronization	Pin 14	$\pm I_{syncV}$	0.35		2.0	mA
Voltage limitation	$\pm I_L$ = 5 mA Pin 1, 14	$\pm V_I$	1.4	1.6	1.8	V
Reference ramp, figure 6						
Charge current	$I_6 = f (R_5)$, R_5 = 1 K ... 820 kΩ Pin 6	I_6	1		20	µA
R_φ – reference voltage	α ≥ = 180 ° Pin 5, 3	$V_{\varphi\ Ref}$	1.06	1.13	1.18	V
Temperature coefficient	Pin 5	$TC_{\varphi\ Ref}$		0.5		mV/K
Output pulse						
Output pulse current	$R_V = 0$, V_{GT} = 1.2 V Pin 4	I_O	100	155	190	mA
Reverse current	Pin 4	I_{OR}		0.01	3.0	µA
Output pulse width	Pin 5, 2	t_p		8		µs/nF
Automatic retriggering						
Repetition rate	Pin 4	t_{pp}	3	4.5	6	t_p
Amplifier						
Common-mode voltage range	Pin 9, 10	V_{ICR}	(V_{13}–1V)		(V_2–1V)	V
Input bias current	Pin 10	I_{IB}		0.01	1	mA
Input offset voltage	Pin 9, 10	V_{IO}		10		mV
Output current	Pin 11	$-I_O$ $+I_O$	75 88	110 120	145 165	µA µA
Short circuit forward transmittance	$I_{11} = f (V_{9/10})$ Pin 11	Y_f		1000		µA/V
Frequency-to-voltage converter						
Input bias current	Pin 7	I_{IB}		0.6	2	µA
Input voltage limitation	$\pm I_{I\ =}$ 1 mA Pin 7	$+V_I$ $-V_I$	660 7.25		750 8.05	mV V
Turn-on threshold	Pin 7	$-V_{TON}$		100	150	mV
Turn-off threshold	Pin 7	$-V_{TOFF}$	20	50		mV
Discharge current	Figure 2 Pin 8	I_{dis}		0.5		mA
Charge transfer voltage	Pin 8	V_{ch}	6.50	6.70	6.90	V
Charge transfer gain I_9 / I_8	Pin 8/9	G_i	7.5	8.3	9.0	
Conversion factor	C_8 = 1 nF, R_9 = 100 kΩ	k		5.5		mV/Hz
Operating range f/V output	Ref. point Pin 13 Pin 9	V_O		0 – 6		V
Linearity				± 1		%
Soft start Pin 12						
f/v–converter non-active figures 8 and 9						
Starting current	$V_{12} = V_{13}$, $V_7 = V_2$	I_O	20	30	50	µA
Final current	V_{12} = –0.5 V	I_O	50	85	130	µA
f/v–converter active figures 7 and 10						
Starting current	$V_{12} = V_{13}$	I_O	2	4	6	µA
Final current	V_{12} = –0.5 V	I_O	30	55	80	µA
Discharge current	Restart pulse	$-I_O$	0.5	3	10	mA

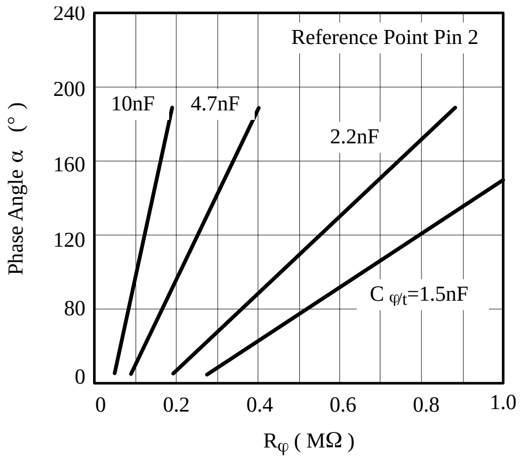


Figure 6. Ramp control

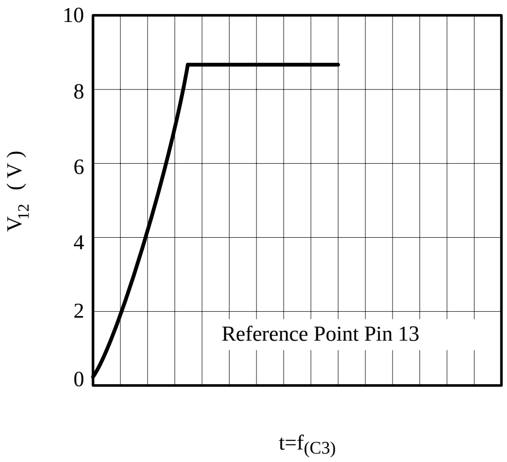


Figure 9. Soft-start voltage (f/V-converter non-active)

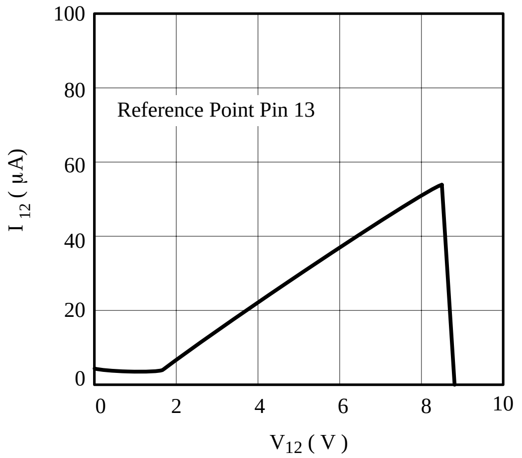


Figure 7. Soft-start charge current (f/V-converter active)

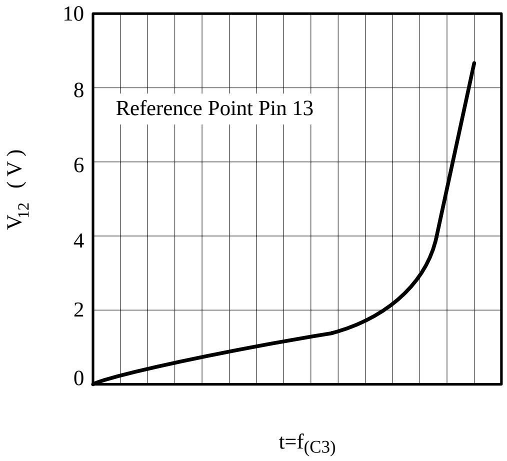


Figure 10. Soft-start voltage (f/V-converter active)

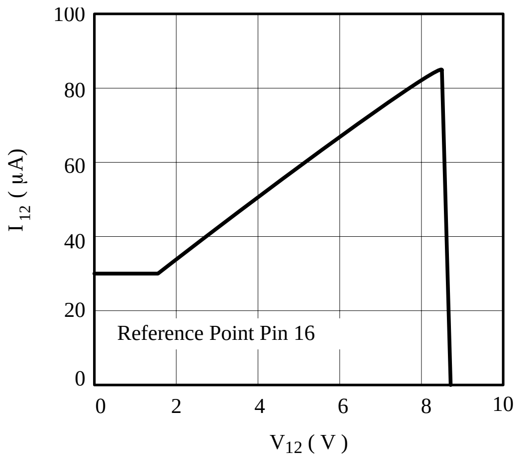


Figure 8. Soft-start charge current (f/V-converter non-active)

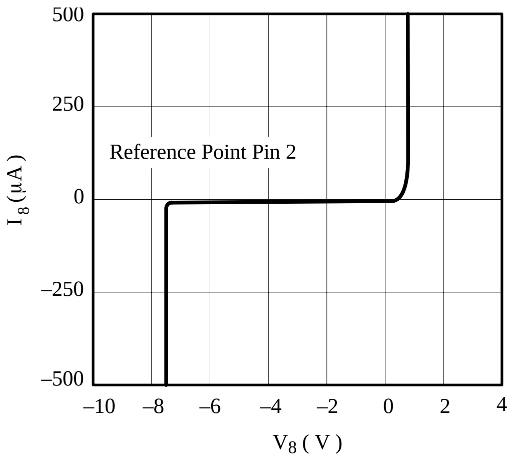


Figure 11. f/V-converter voltage limitation

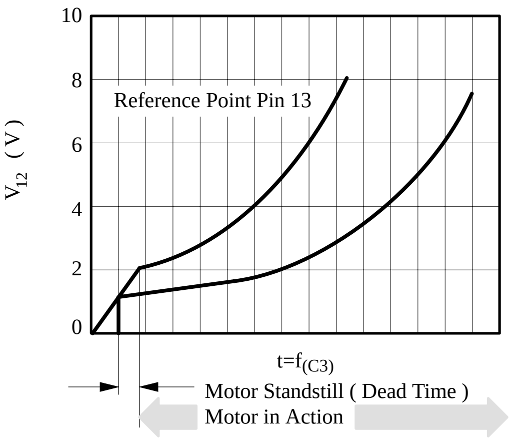


Figure 12. Soft start function

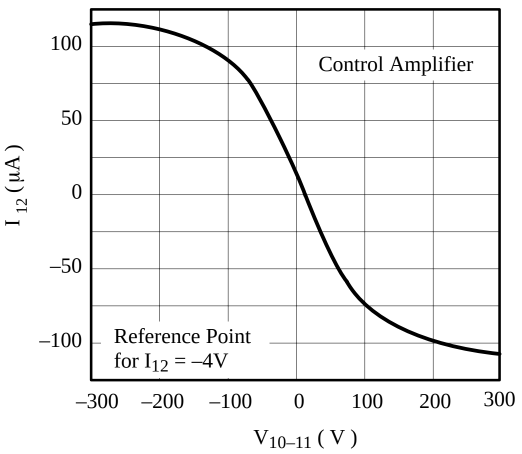


Figure 13. Amplifier output characteristic

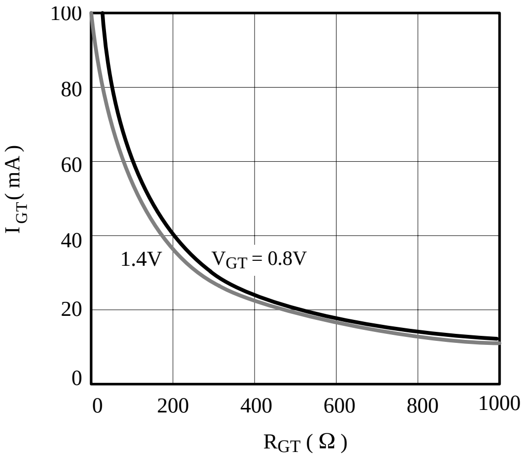


Figure 14. Pulse output

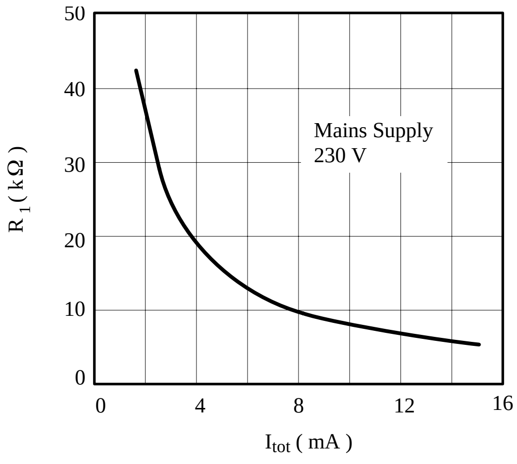


Figure 15. Determination of R_1

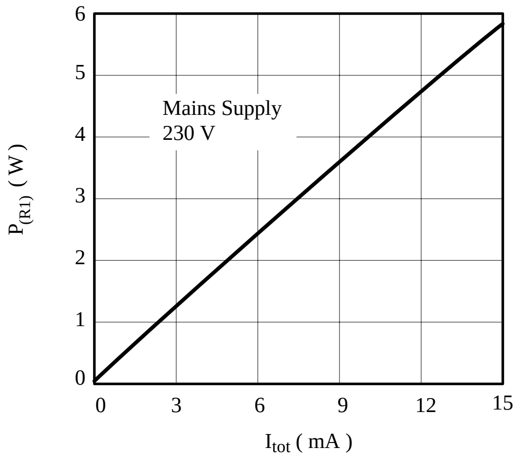


Figure 16. Power dissipation of R_1 according to current consumption

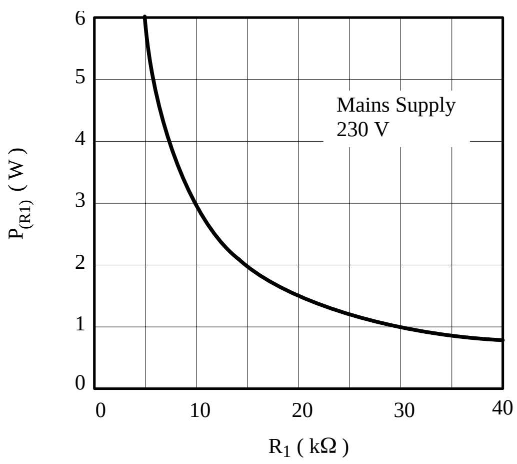
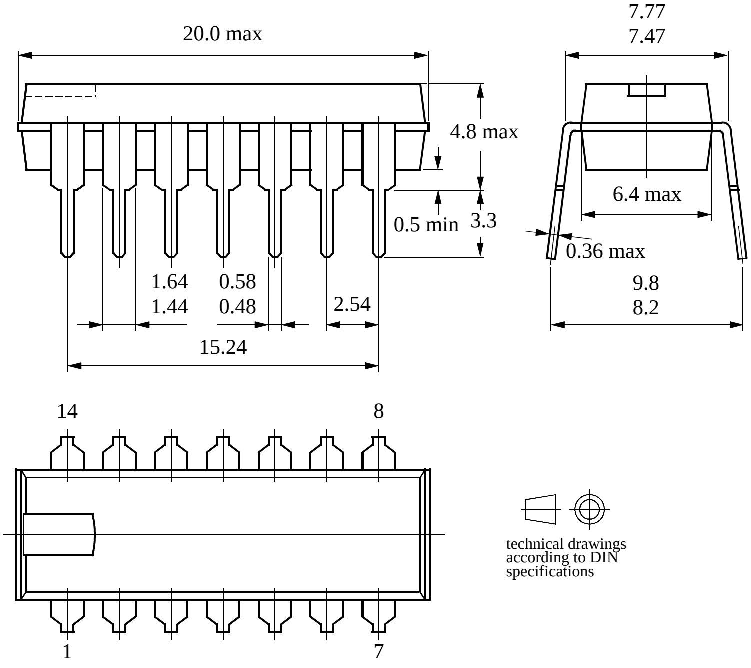


Figure 17. Power dissipation of R_1

Package Information

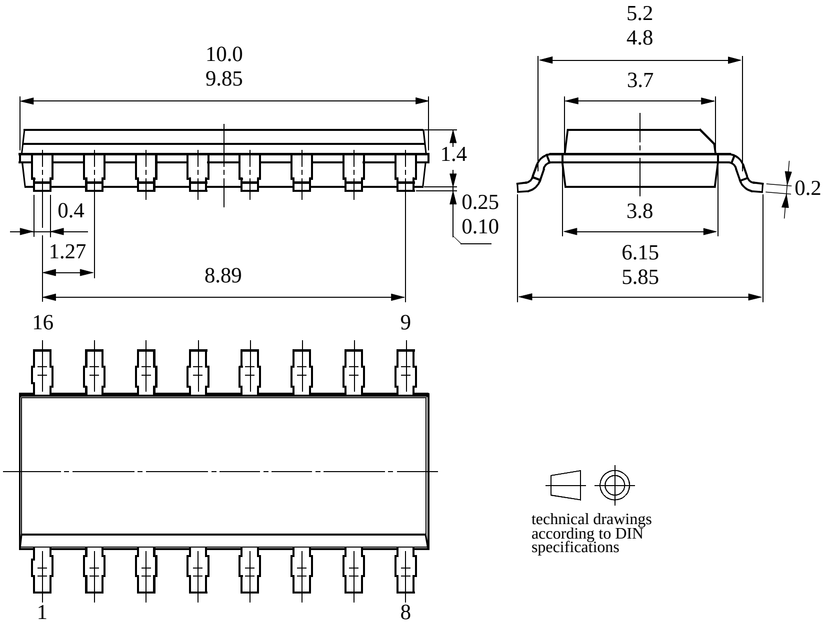
Package DIP14

Dimensions in mm



Package SO16

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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