MIXED ANALOG - DIGITAL BIPOLAR ARRAYS

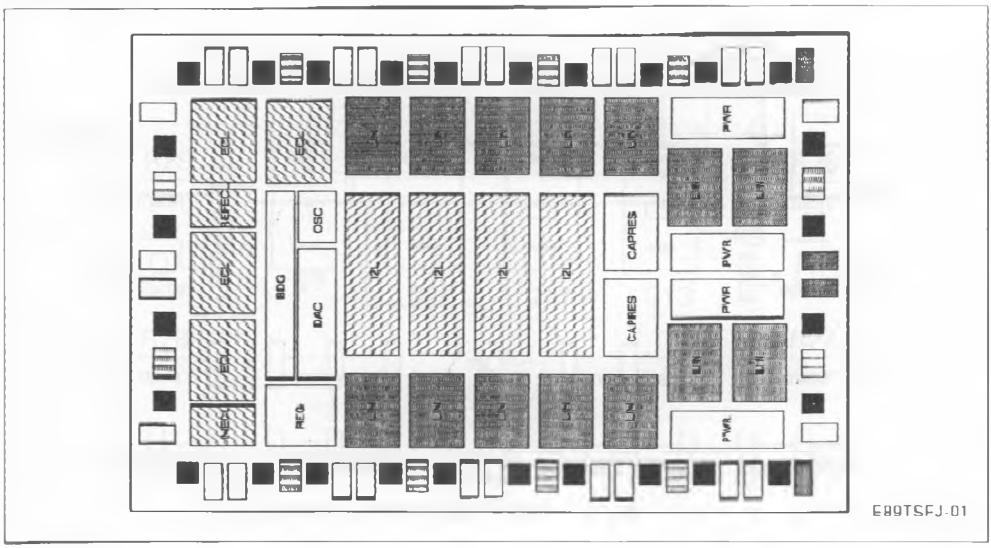
- ADVANCED BIPOLAR TECHNOLOGY :
  - NPN, F_T = 3GHz
  - 2 METAL LAYER
  - 100MHz, ECL FUNCTIONS
- FULL ESD PROTECTION
- POWER SUPPLY :
  MAXIMUM RATINGS = UP TO 15V
  OPERATING CONDITIONS = 3 TO 12V
- ANALOG - DIGITAL ARRAYS :
  - ANALOG TILES
  - ECL TILE FOR HIGH SPEED LOGIC
  - I2L CORE FOR LOW FREQUENCY RANDOM LOGIC
  - POWER TILE WITH 200mA CAPABILITY
- 5 ARRAYS AVAILABLE :
  J4, J6, J9, J13, J23 FROM 600 TO 3000 COMPONENTS
- CAD SOFTWARE SUPPORT :
  - ADS-PC (analog design system - PC)
  - FULLY INTEGRATED IN PC ENVIRONMENT
  - P-CAD* SOFTWARE, FOR SCHEMATIC CAPTURE, SIMULATION, AND LAYOUT
- OPERATING TEMPERATURE RANGE :
  COMMERCIAL : 0 TO 70C
  INDUSTRIAL : - 40 TO + 85C
  MILITARY : - 55 TO + 125C
- PACKAGE OPTIONS
  DIL : PLASTIC OR CERAMIC
  SMD : SO, PLCC, LCCC, QFP

USIC PRODUCTS DESCRIPTION

SGS-THOMSON Microelectronics introduces the mixed analog-digital arrays developped on a 3GHz process. Using the expertise in bipolar arrays, SGS-THOMSON has developped this new series to offer a product taking the leading edge of any technology :

- High speed process (NPN, F_T = 3GHz)
- Architecture with tile concept to improve the efficiency of the placement and routing
- 2 customized metal layers with 4 masks to personalize (contact, M1, via, M2)
- Complete CAD system on a PC from schematic capture up to the layout.

Figure 1 : Example of TSFJ13 architecture.



TSFJ ARCHITECTURE

TECHNOLOGY

TSFJ series developped by SGS-THOMSON is using an advanced bipolar process with high frequency performance (NPN, F_t = 3GHz). With a double metal layer the parasitic elements are minimized to improve the layout density and to increase the performances.

The process is very well suited for accurate analog bipolar design. The other key feature is introduced with the digital capability using either ECL functions or I2L ones.

Thanks to protection network placed on each input pad, the complete TSFJ series is protected against ESD parasitic effects.

TILE ARCHITECTURE

The TSFJ series has an architecture based on a tile concept in order to take advantage of efficient layout.

For SGS-THOMSON a tile is an optimized placement of basic components such as transistors, resistors, and capacitors, with no routing done in advance. When customisation is prepared, the designer optimized the routing of each tile according to his needs.

6 different types of tiles have been developped :

- LINEAR TILE, optimized for analog functions (op amps, comparators, ...)
  - 6 standard NPN (h_{FE} = 105, and I_c = 100A)
  - 2 low noise NPN
  - 7 lateral PNP (h_{FE} = 52, and I_c = 1A)
  - 44 resistances from 100 ohms to 50KΩ
- POWER TILE, optimized for power interface capability ;
  - 4 standard substrate PNP
  - 1 power substrate PNP (I_{KF} = 10mA)
  - 1 power NPN (I_{KF} = 314mA)
  - 1 medium power NPN (I_{KF} = 78mA)
  - 3 std NPN
- I2L LOGIC TILE, optimized to implement random logic using standard I2L functions (NAND, AND, NOR, OR, Flip-flop, ...)
  - row of I2L operators
- ECL LOGIC TILE, optimized for high speed logic up to 100MHz
  - equivalent to 1 D flip-flop or 5 NOR gates
- BUILT-IN FUNCTION TILES, a certain number of predefined tile have been created to fulfill some specific analog requests such as ;
  - 1 bandgap voltage reference
  - 1 oscillator (RC or quartz)
  - 1 voltage regulator
  - 1 R-2R resistor ladder for 6 bits DAC
- RESISTOR/CAPACITOR TILE, optimized for RC network or compensation capacitor purpose
  - 2.5pF and 7pF capacitor available

Figure 2 : Example of a symbolic Linear Tile.

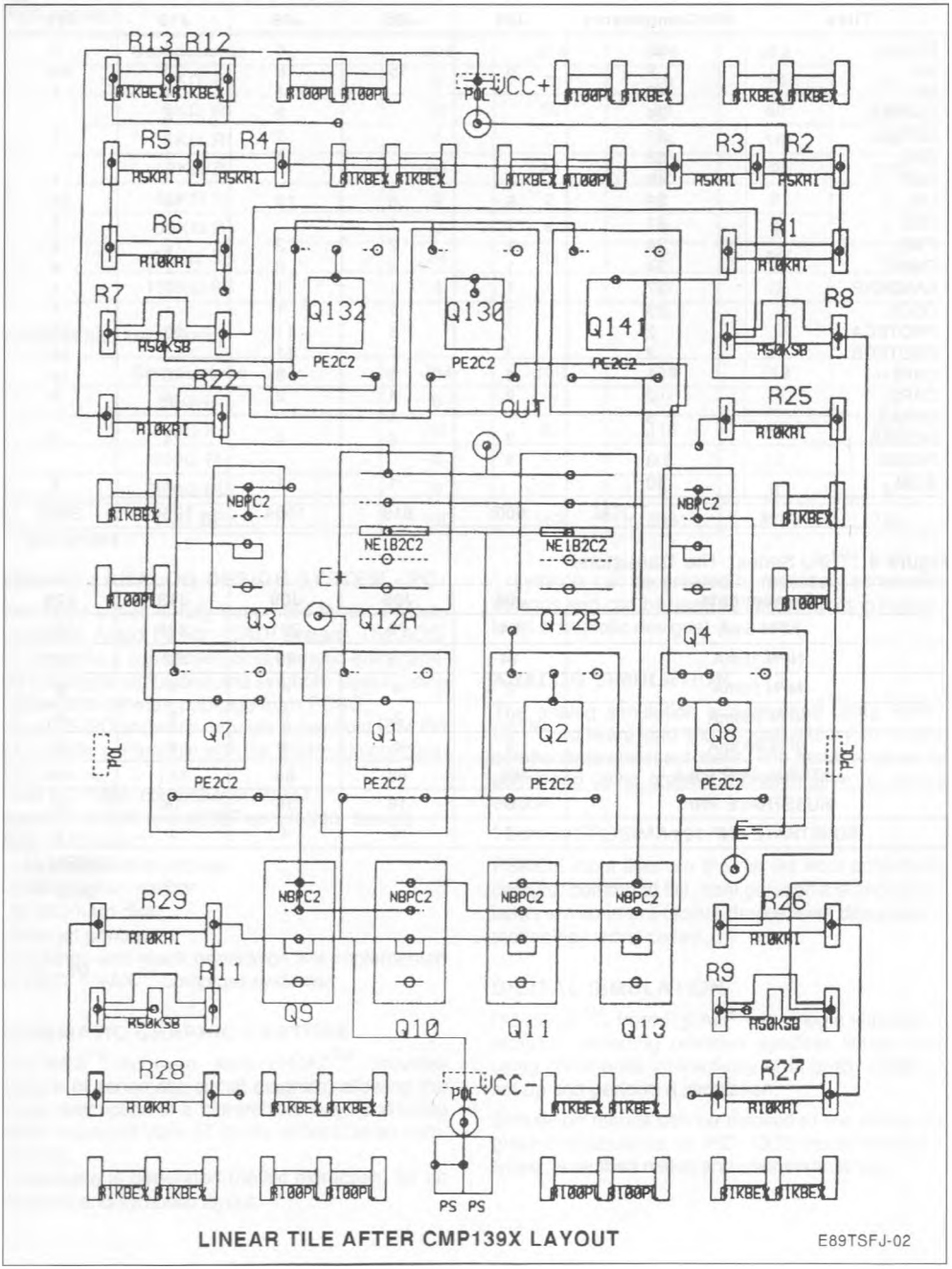


Figure 3 : TSFJ Series : The Available Tiles.

Tiles	Nb Components	J04	J06	J09	J13	J23
ECL	86			4	4	5
I2L	9	6	15	18	36	54
HF	46			1	1	1
CAPRES	24			2	2	
REFECL	31			1	1	1
DAC	33			1	1	
R2R	46					1
LIN	59	6	8	10	14	24
RES	21	1	1			4
PWR	34	1	2	2	2	4
PWR1	34	1	2	2	2	4
BANDGAP	37	1	1	1	1	1
OSCIL	23	1	1	1	1	1
PROTECA	2	7	8	11	13	18
PROTECB	2	7	7	11	13	18
CAP1	1	4	6	8	8	10
CAP2	2	2	4	2	4	9
CAPAS	3		1			
DIODES	2	2	4	4	4	8
PUISS	3	1				
ALIM	40		1	1	1	2
	TOTAL :	600	919	1554	1964	3067

E88TSFJ-03

Figure 4 : TSFJ Series : The Transistors.

Components	J04	J06	J09	J13	J23
NPN 5mA	54	79	201	225	331
NPN 16mA	14	18	24	32	52
NPN 50mA	2	4	4	4	8
NPN 100mA	2	2	2	2	4
NPN 200mA	2	4	4	4	8
LATERAL PNP 60µA	50	68	83	111	184
SUBSTRATE PNP	8	16	16	16	32
SUBSTRATE PNP 10mA	2	4	4	4	8

E88TSFJ-04

Figure 5 : TSFJ Series : The Resistors.
(high values)

Components	J04	J06	J09	J13	J23
3KΩ RI	0	0	10	10	10
5KΩ RI	36	56	64	80	136
8KΩ RI	0	0	18	18	18
10KΩ RI	64	80	96	128	202
40KΩ RI	0	2	2	2	2
50KΩ RI	0	4	4	4	4
50KΩ SB	24	32	40	56	88
100KΩ SB	4	4	12	12	20

(medium and low values)

Components	J04	J06	J09	J13	J23
30Ω PL	9	17	17	17	33
100Ω PL	60	80	116	156	260
200Ω PL	0	0	16	16	20
300Ω PL	0	0	9	9	8
1KΩ BEX	130	182	398	470	720

E68TSFJ-05

ADS-PC : ANALOG DESIGN SYSTEM - PC

The TSFJ series is fully supported by a complete Computer Aided Design (CAD) system. The ADS-PC tool offers capabilities of schematic entry, analog and digital simulation and symbolic layout, using a standard software package from PCAD.
The ADS-PC software requires a low cost IBM PC AT3 or fully compatible with the following configuration :
- 640 KO RAM, coprocessor 80287
optional : 80386 and 80387 accelerator boards
2MB EMS board
- microsoft parallel mouse
- EGA graphic monitor
- 30 MO hard disk
- laser jet printer
Checkings and mask generation are implemented on DEC™ VAX™ computer systems.

SCHEMATIC GRAPHIC CAPTURE

PC-CAPS™ software, from P-CAD™, provides capture of schematic circuit diagram, allowing the circuit description in a hierarchical way* and using either macrocell from ST library or basic array components.
A database is generated (netlist extraction) for simulation and symbolic layout.

* (symbols can be created to represent schematic designs and can be used as components in higher-level schematic designs)

ANALOG SIMULATION

The analog simulation is performed using PSPICE™* software and the models library for basic components and macrocells. The result analysis is performed using graphic representation on listing edition.

* from MICROSIM

PSPICE input files are the net list from schematic capture, command file, configuration file and simulation environment (active device level description, technology worst cases...).

DIGITAL SIMULATION

PC-LOGS™, from P-CAD™, is a logic simulation program providing primitive symbols library and using commands interactively or in batch mode to set up and perform a simulation.

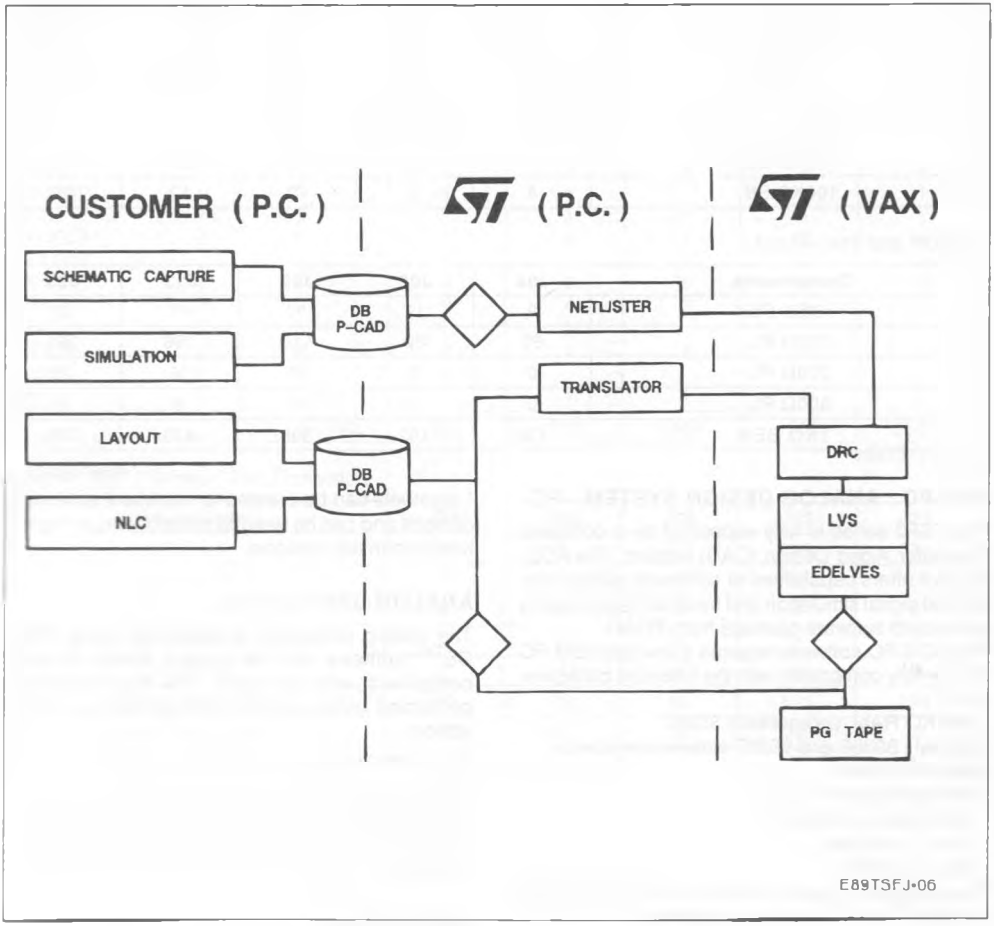
Simulation results can be displaid to the screen in graphic or tabular forms. PC-LOGS inputs are of two types : a verified netlist and user commands.

PLACEMENT AND ROUTING

PC-CARDS™, from P-CAD™, is built around an intelligent database that continually keeps track of components and connectivities.

The on-screen menu includes commands to draw, edit, move, delete, zoom in and out, view selected window.

Figure 6 : ADS - PC Design Flow.



CUSTOMER DESIGN INTERFACE

SGS-THOMSON has developped several interfaces for customers, giving them easy and flexible design approaches for TSFJ mixed analog/ digital bipolar arrays.

User can access ADS-PC system ;
- via the SGS-THOMSON Design centers
- via CAE workstations using a PC configuration and the P-CAD™ software package

According to all of these design possibilities, SGS-THOMSON defined 2 main customer interfaces. Next figure outlines these interfaces. Each interface delimits the responsabilities of customer and SGS-THOMSON during circuit development flow.

	Interface 2	Interface 3
Definition of Circuit Specifications	Customer	Customer
Electrical Description (analog + digital)	Customer	Customer
Test Procedure	Customer	Customer
Graphic Capture + Input Signal Entry	ST	Customer
Design Verification	ST	Customer
Simulation (analog + digital)	ST	Customer
Approval	Customer	Customer/ST
Place and Route	ST	Customer
Final Design Release	Customer	Customer/ST
Test Program Generation + Test Tooling	ST	ST
Mask Tooling	ST	ST
Prototype Manufacturing	ST	ST
Prototype Delivery	ST	ST

With interface 3, design can be done either at SGS-THOMSON Microelectronics design center facilities or at customer location.

ABSOLUTE MAXIMUM RATINGS (note 1) T_{amb} = 25°C, Voltage Referenced to V-

Symbol	Parameter	Value		Unit
		Min.	Max.	
V+	Supply Voltage	− 0.5	+ 15	V
T_{stg}	Storage Temperature (ceramic)	− 60	+ 150	°C
	Storage Temperature (plastic)	− 40	+ 125	°C

Note : 1. Stresses above those listed order "maximum rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these on any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS, Voltage Referenced to V-

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
V+	Operating Supply Voltage		3		12	V
T_{amb}	Operating Ambient Temperature	Military	− 55		+ 125	°C
		Industrial	− 40		+ 85	
		Commercial	0		+ 70	

DC GENERAL ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
	Resistors					
P_*	P_* Diffusion	Resistor Value Range	30		420	Ω
		Absolute Accuracy			± 25	%
		Matching (note 1)			± 2	%
		Matching (note 2)			± 6	%
		Temperature Coefficient (1^{st} order)			0.12	%/°C
B_{ext}	Extrinsec Base Region	Resitor Value Range	270		5000	Ω
		Absolute Accuracy			± 15	%
		Matching (1)			± 2	%
		Matching (2)			± 6	%
		Temperature Coefficient (1^{st} order)			0.09	%/°C
R_I	Implanted Resitor	Resitor Value Range	5		50	KΩ
		Absolute Accuracy			± 15	%
		Matching (1)			± 2	%
		Matching (2)			± 6	%
		Temperature Coefficient (1^{st} order)			0.21	%/°C
B_{INT}	Intrinsec Base Region	Resitor Value Range	50		100	KΩ
		Absolute Accuracy			± 25	%
		Matching (1)			± 2	%
		Matching (2)			± 6	%
	Capacitors	Capacitor Value Range	2.5		7	pF
		Absolute Accuracy			± 20	%
V_*		Maximum Operating Voltage			20	V
N_{BPC1}		std NPN Transistor (note 3)				
V_{BCB0}	Breakdown Voltage	Collector-base	40			V
V_{BCE0}	Breakdown Voltage	Collector-emitter	18			V
V_{BCS0}	Breakdown Voltage	Collector-substrate	40			V
H_{FE}	Current Gain	@ I_c = 100µA		100		
I_{KF}	Knee Current			5.6		mA
NPWR		Power NPN Transistor (note 3)				
V_{BCB0}	Breakdown Voltage	Collector-base	40			V
V_{BCE0}	Breakdown Voltage	Collector-emitter	18			V
V_{BCS0}	Breakdown Voltage	Collector-substrate	40			V
H_{FE}	Current Gain	@ I_c = 10mA		140		
I_{KF}	Knee Current			314		mA

Notes=
1. matching between 2 resistors of the same value, closed to each other and with the same orientation on the die.
2. matching between 2 resistors of different values, close one from the other and with the same orientation on the die.
3. for more informations refer to the TSFJ user's manual.
4. voltage references are provided by an "ECL reference" macrocell (REFECL) built on a specific tile.
5. input voltages could be supplied by a specific tile called HFECL.
6. output levels are not compatible with standard 10K, 100K ECL series.

DC GENERAL ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
PNPS		Substrate PNP Transistor (note 3)				
V_{BCB0}	Breakdown Voltage	Collector-base	40			V
V_{BCE0}	Breakdown Voltage	Collector-emitter	18			V
V_{BCS0}	Breakdown Voltage	Collector-substrate	40			V
H_{FE}	Current Gain	@ I_c = 1µA		160		
I_{KF}	Knee Current			40		µA
		ECL Cells (V_+ = 5V ± 10%)				
V_R	$V_{reference}$	Voltage Reference (note 4)		.97		V
V_{T1}	$V_{reference}$	Voltage Reference (note 4)		3.92		V
V_{T2}	$V_{reference}$	Voltage Reference (note 4)		3.20		V
V_{IL}	Input Voltage	(note 5)			3.6	V
V_{IH}	Input Voltage	(note 5)	4.3			V
V_{OL}	Output Voltage	(note 6)			3.6	V
V_{OH}	Output Voltage	(note 6)	4.3			V

Notes : 1. matching between 2 resistors of the same value, closed to each other and with the same orientation on the die.
2. matching between 2 resistors of different values, close one from the other and with the same orientation on the die.
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5. input voltages could be supplied by a specific tile called HFECL.
6. output levels are not compatible with standard 10K, 100K ECL series.

DIGITAL LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT

(unless otherwise specified, T_{amb} = 25°C, typical process)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
		ECL CELLS				
V_S	Voltage Swing			600		mV
T_G	Toggle Frequency	D Type Flip-flop			100	MHz
t_{PLH}	Propagation Delay	NAND2, (FO = 1)		1.1		ns
t_{PHL}	Propagation Delay	NAND2, (FO = 1)		3.2		ns
		I2L CELLS (note 7)				
T_G	Toggle Frequency	D Type Flip-flop				
		@ Injection = 0.1µA			20	KHz
		@ Injection = 1µA			160	KHz
		@ Injection = 10µA			600	KHz

Note : 7. I2L cells have been caracterised between 0.1µA and 100µA.

ANALOG LIBRARY, AC ELECTRICAL CHARACTERISTICS ABSTRACT

(unless otherwise specified, T_{amb} = 25°C, typical process)

JOPA1 (programmable operationnal amplifier) $V_{CC} \pm 6V$, $I_{set} = 20\mu A$

Symbol	Parameter	Test Conditions	Typical Value	Unit
B	Unity Gain Bandwidth	RL = 5KΩ ; CL = 20pF	1	MHz
ϕM	Phase Margin	Av = 1 ; RL = 5KΩ ; CL = 20pF	60	
Svo	Slew Rate	Av = 1 ; RL = 5KΩ ; CL = 20pF	0.35	V/µs
Av	Open-loop Voltage Gain	RL = 5KΩ ; CL = 20pF	90	dB

JCOMP1 (programmable voltage comparator - LM139 type)

Symbol	Parameter	Test Conditions	Typical Value	Unit
tref	Large Signal Response Time	RL = 5KΩ ; CL = 2pF with Overdrive : 100mV	300	ms
tre	Small Signal Response Time	RL = 5KΩ ; CL = 2pF with Overdrive : 5mV	1	µs
AVD	Large Signal Voltage Gain		87	dB