SGS-THOMSON MICROELECTRONICS

TS93C46

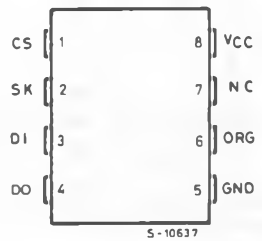
1K BIT SERIAL CMOS EEPROM

- HIGHLY RELIABLE CMOS FLOATING GATE TECHNOLOGY.
- SINGLE 5-VOLT SUPPLY
- EIGHT PIN PACKAGE.
- 64 x 16 OR 128 x 8 USER SELECTABLE SERIAL MEMORY
- COMPATIBLE WITH NATIONAL SEMICONDUCTOR NMC 9346 and NMC 9306
- SELF TIMED PROGRAMMING CYCLE.
- WORD AND CHIP ERASABLE
- 10,000 ERASE/WRITE CYCLES.
- TEN YEARS DATA RETENTION
- POWER-ON DATA PROTECTION

P
DIP-8
(Plastic Package)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS



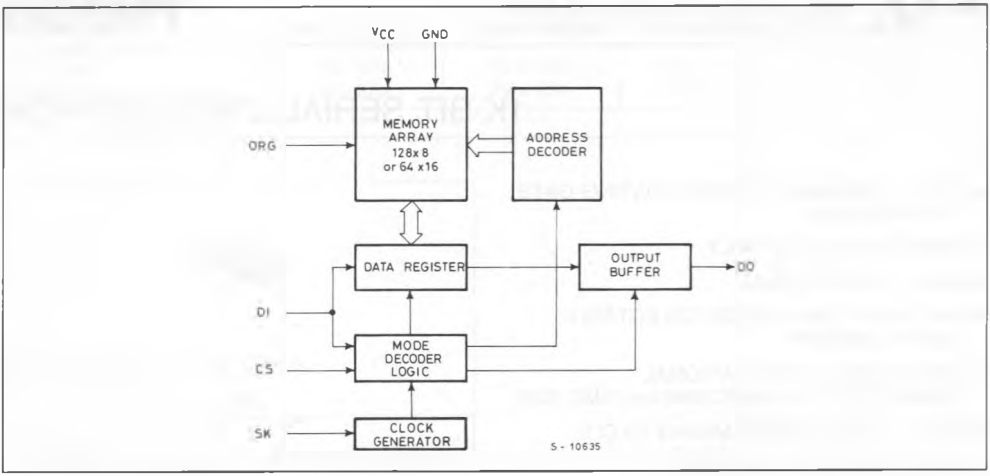
PIN NAMES

CS	CHIP SELECT
SK	CLOCK INPUT
DI	SERIAL DATA INPUT
DO	SERIAL DATA OUTPUT
ORG	ORGANIZATION INPUT
V_{CC}	+5V POWER SUPPLY
GND	GROUND
NC	NO CONNECT

PIN DESCRIPTION

Name	No	Description
CS	1	Chip Select
SK	2	Clock Input
DI	3	Serial Data Input
DO	4	Serial Data Output
GND	5	Ground
ORG	6	Memory Array Organization Selection Input. When the ORG pin is connected to +5, the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull up device will select the 64 x 16 organization.
V_{CC}	8	+5V Power Supply

BLOCK DIAGRAM



INSTRUCTION SET

Instruction	Start bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	10	A_6-A_0	A_5-A_0			Read Address A_N-A_0
ERASE	1	11	A_6-A_0	A_5-A_0			Erase Address A_N-A_0
WRITE*	1	01	A_6-A_0	A_5-A_0	D_7-D_0	D_{15}-D_0	Write Address A_N-A_0
EWEN	1	00	11xxxxx	11xxxx			Program Enable
EWDS	1	00	00xxxxx	00xxxx			Program Disable
ERAL	1	00	10xxxxx	10xxxx			Erase All Addresses
WRAL	1	00	01xxxxx	01xxxx	D_7-D_0	D15-D_0	Program All Addresses

* Write instruction is a self timed program instruction. The selected byte (word) gets erased before being written.

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it si possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

POWER-ON DATA PROTECTION CIRCUITRY: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	+7	V
	Voltage on any input pin	GND −0.3 to +7	V
	Voltage or any output pin	V_{CC} +0.3 GND −0.3	V
T_{STG}	Storage temperature range	−65 to +150	°C
	Lead temperature (Soldering: 10 seconds)	+300	°C

READ OPERATION

DC CHARACTERISTICS
(T_{amb} = 0° to 70°C for CP, T_{amb} = −40 to +85°C for VP, V_{CC} = 5V ± 10%; Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
V_{CC}	Operating voltage		4.5		5.5	V
I_{CC1}	Operating current	V_{CC} = 5.5V, CS = V_{IH} CP range VP range			 4 4	mA
I_{CC2}	Standby current	V_{CC} = 5.5V, CS = DI = SK = GND + 0.1V)			100	µA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC} + 1	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA			0.4	V
V_{OH}	Output high voltage	I_{OH} = −400µA	2.4			V
I_{LI}	Input leakage current	V_{in} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{out} = 5.5V, CS = 0			10	µA

AC ELECTRICAL CHARACTERISTICS

(T_{amb} = 0° to 70°C for CP T_{amb} = −40 to +85°C for VP, V_{CC} = 5V ± 10%; Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
	SK max (Maximum frequency)				250	KHz
	SK duty cycle		25	50	75	%
T_{CSS}	CS setup time		0.2			µs
T_{CSH}	CS hold time		0			µs
T_{DIS}	DI Setup time		0.4			µs
T_{DIH}	Data input hold time		0.4			µs
T_{PD1} T_{PD0}	Data output delay	CL = 100pF, V_{OL} = 0.8V, V_{OH} = 2.0V and V_{IH} = 2.4V, V_{IL} = 0.45V			2.0 2.0	µs
T_{HZ}	Output delay to Hi Z				0.4	µs
$T_{E/W}$	Erase/write pulse width				10	ms
T_{CS}	Min. CS low time		1			µs
T_{SKHI}	SK high time		1			µs
T_{SKLOW}	SK low time		1			µs
T_{SV}	Output delay to status valid				1	µs

DEVICE OPERATION

The TS93C46 is a serial Eeprom memory featuring a software programmable organization: 128 x 8 bit or 64 x 16 bit. It has 7 instructions that allow it to read, erase or write.

Each instruction consists of a start bit (logical "1"), an opcode field (2 bits), an address field (6 or 7 bits) and optionaly a data field (8 or 16 bits) — Address and data fields length depending on organization x 8 or x 16.

The DO pin is a multiplexed pin. It is used as data out during the read mode. It can also be used as a ready/busy indicator in programming mode. In all other modes, DO is tri-stated.

During power-up, all modes of operation are disabled, and the device comes up in a program-disabled state. An EWEN instruction has to be issued before starting programming.

READ

The READ instruction reads the content of the addressed register. It outputs data serially on the DO pin. After the instruction is decoded, a dummy bit (logical "0") precedes the output data string.

ERASE/WRITE ENABLE AND DISABLE

After power-up and before starting any programming instruction, the EWEN instruction has to be issued. Once it has been issued, it will remain active until an EWDS instruction takes place. The EWDS instruction is provided to avoid any accidental programming of the part. The read instruction is independent from the EWEN and EWDS instructions.

ERASE

After an ERASE instruction has been shifted in, CS is dropped low. This will set the beginning of the self timed erase sequence. If CS is then brought high (after observing TCS spec), the DO pin will act as a status indicator. It will remain low as long as the chip is programming. It will go high after all the bits of the addressed register have been set to al logical "1".

WRITE

After a WRITE instruction has been shifted in with the corresponding 8 bits or 16 bits of data, CS is dropped low. This will set the beginning of the self timed programming cycle. The addressed register will first be automatically erased and then the previously shifted data will be written in the register. If CS is brought high during the programming time (after observing the TCS spec), the DO pin will act as a status indicator-it will remain low a long as the chip is programming. It will go high after all the bits of the addressed register have been set to the proper value.

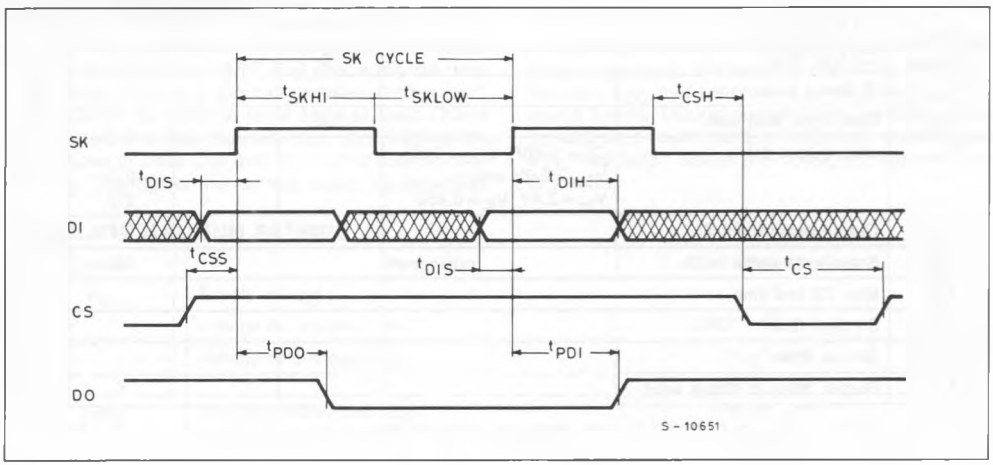
ERASE ALL

This instruction is provided to erase the whole chip. It works the same way as the erase instruction does.

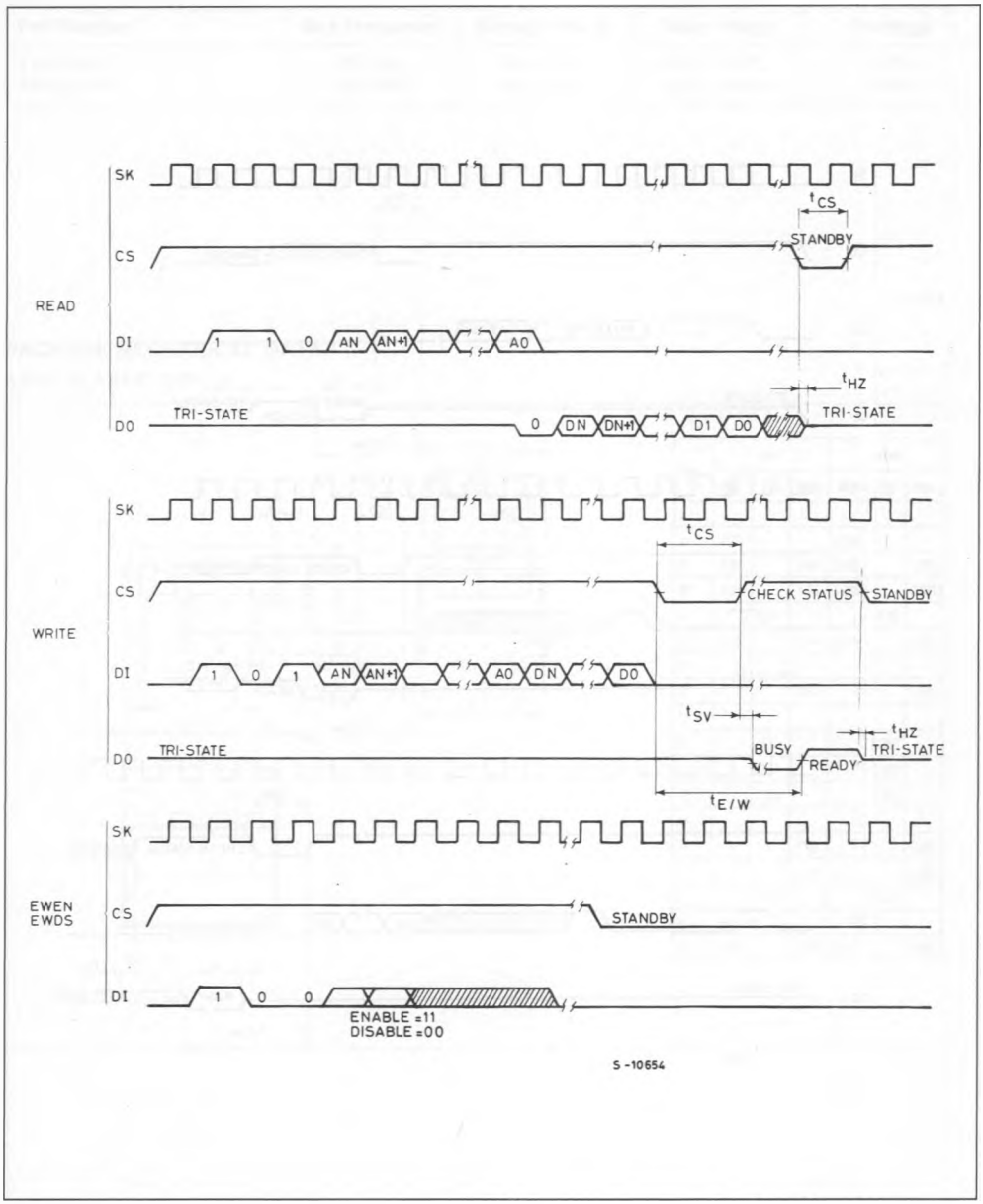
WRITE ALL

This instruction is provided to write simultaneously all the registers. All the registers must be erased before doing a WRAL operation. The WRAL instruction works the same way as the write instruction does.

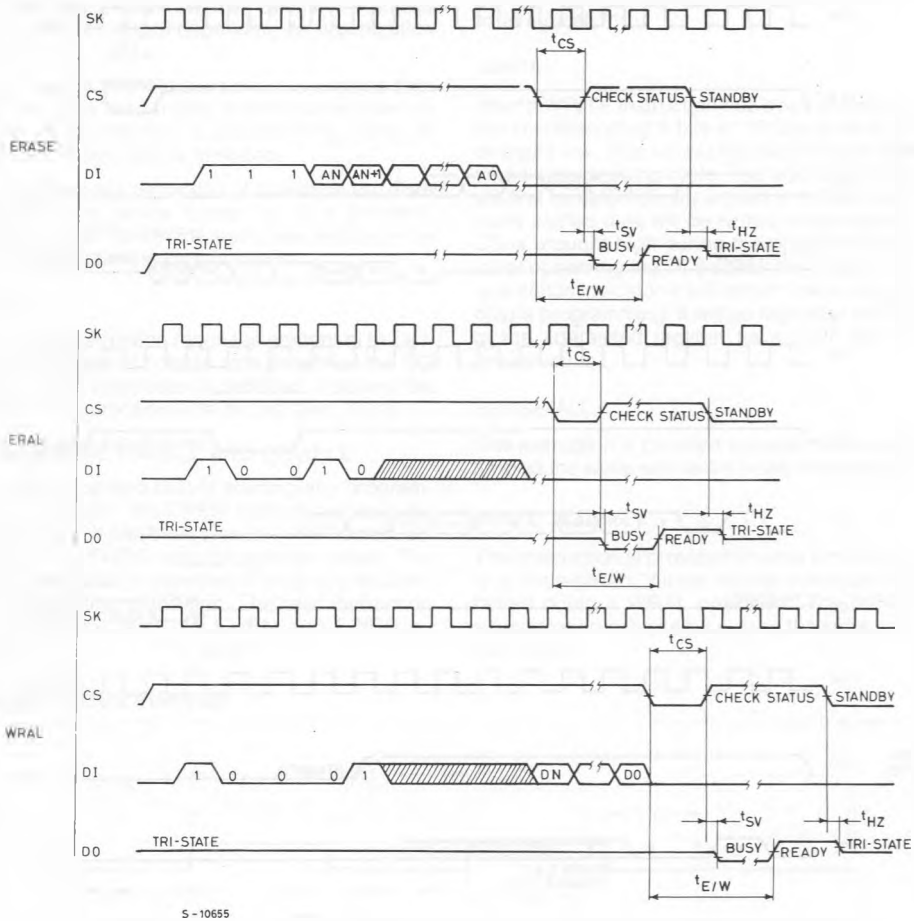
SYNCHRONOUS TIMINGS



INSTRUCTION TIMINGS



INSTRUCTION TIMINGS (Continued)

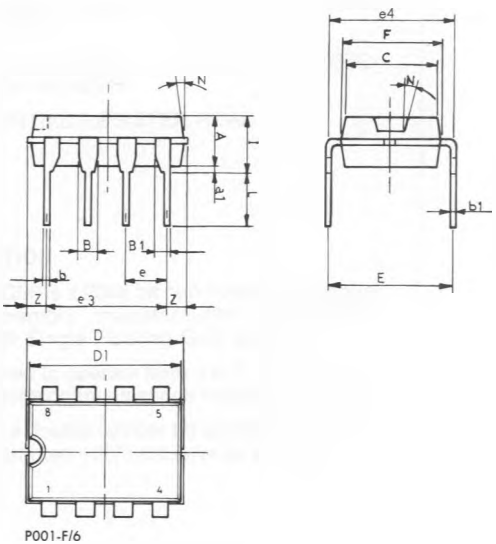


ORDERING INFORMATION

Part Number	Max Frequency	Supply Voltage	Temp. Range	Package
TS93C46CP	250 KHz	5V ± 10%	0 to +70°C	DIP-8
TS93C46VP	250 KHz	5V ± 10%	−40 to +85°C	DIP-8

PACKAGE MECHANICAL DATA

8-PIN PLASTIC DIP



P001-F/6

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1	0.70			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.50			0.02	
b1	0.38		0.50	0.015		0.020
C						
D			9.80			0.386
D1						
E		8.90			0.350	
e		2.54			0.100	
e3		7.62			0.300	
e4						
F			7.10			0.280
I			4.80			0.189
L		3.30			0.130	
N						
Z	0.44		1.60	0.017		0.063