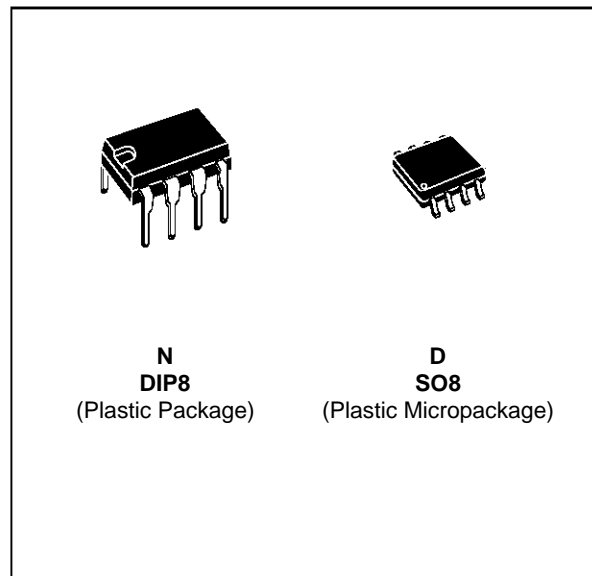


## 3V INPUT/OUTPUT RAIL TO RAIL DUAL CMOS OPERATIONAL AMPLIFIER

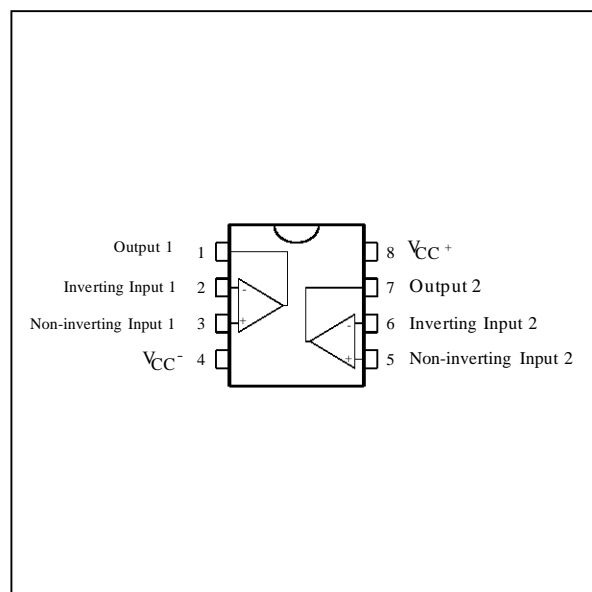
- DEDICATED TO **3.3V** OR **BATTERY SUPPLY** (specified at 3V and 5V)
- RAIL TO RAIL INPUT AND OUTPUT VOLTAGE RANGES
- SINGLE SUPPLY OPERATION FROM **2.7V TO 16V**
- EXTREMELY LOW INPUT BIAS CURRENT : **1pA TYP**
- LOW INPUT OFFSET VOLTAGE : **2mV max.**
- SPECIFIED FOR **600Ω** AND **100Ω** LOADS
- LOW SUPPLY CURRENT : 200μA/Ampli (V<sub>CC</sub> = 3V)
- ESD TOLERANCE : 3KV
- LATCH-UP IMMUNITY



### ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3V912I/AI/BI	-40, +125°C	•	•

### PIN CONNECTIONS (top view)



### DESCRIPTION

The TS3V912 is a RAIL TO RAIL dual CMOS operational amplifier designed to operate with a single 3V supply voltage.

The input voltage range  $V_{icm}$  includes the two supply rails  $V_{CC}^+$  and  $V_{CC}^-$ .

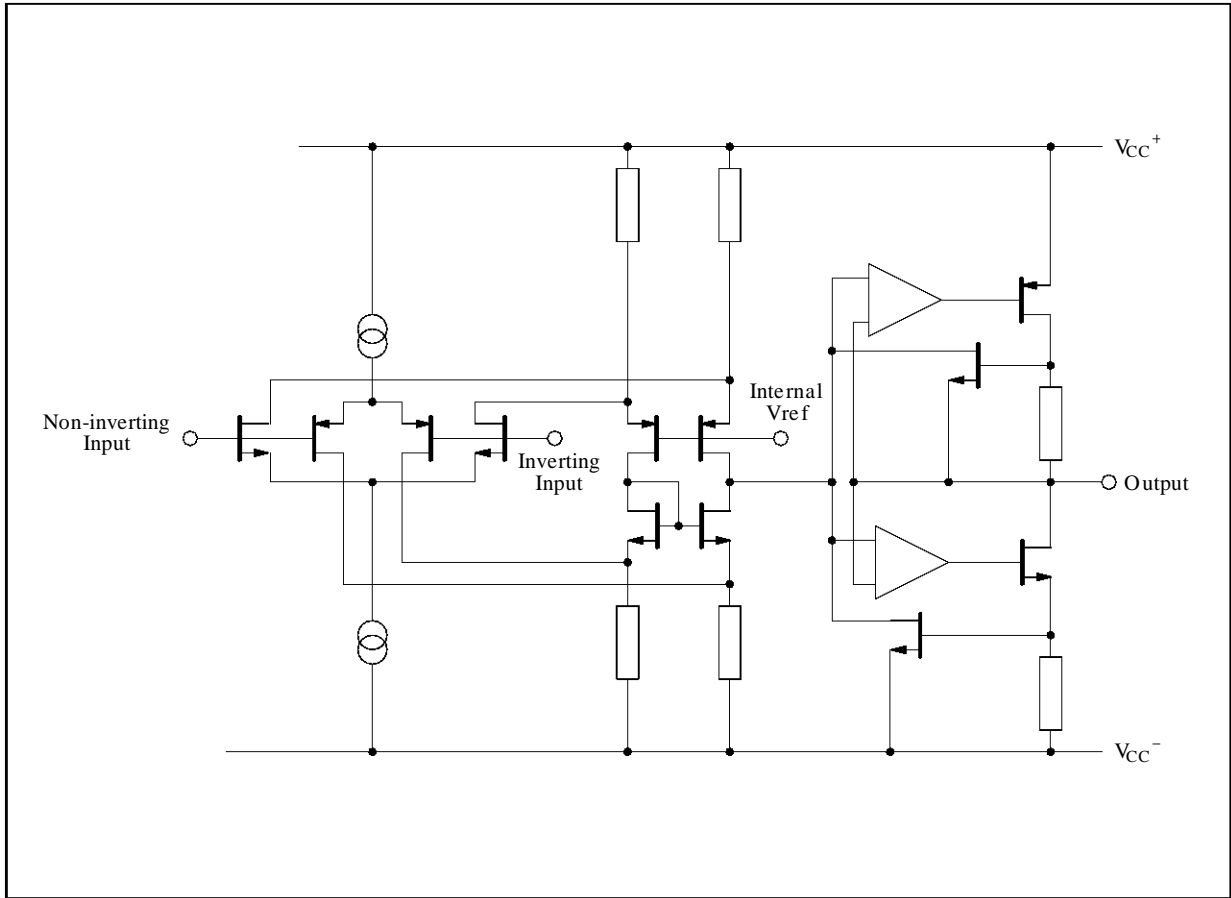
The output reaches :

- $V_{CC}^- + 50mV$      $V_{CC}^+ - 50mV$     with  $R_L = 10k\Omega$
- $V_{CC}^- + 350mV$      $V_{CC}^+ - 350mV$     with  $R_L = 600\Omega$

This product offers a broad supply voltage operating range from 2.7V to 16V and a supply current of only 200μA/amp. (V<sub>CC</sub> = 3V).

Source and sink output current capability is typically 40mA (at V<sub>CC</sub> = 3V), fixed by an internal limitation circuit.

**SCHEMATIC DIAGRAM (1/2 TS3V912)**



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage - (note 1)	18	V
V <sub>id</sub>	Differential Input Voltage - (note 2)	±18	V
V <sub>i</sub>	Input Voltage - (note 3)	-0.3 to 18	V
I <sub>in</sub>	Current on Inputs	±50	mA
I <sub>o</sub>	Current on Outputs	±130	mA
T <sub>oper</sub>	Operating Free Air Temperature Range	-40 to +125	°C
	TS3V912I/AI/BI		
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

**Notes :**

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V<sub>CC</sub><sup>+</sup> +0.3V.

**OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	2.7 to 16	V
V <sub>icm</sub>	Common Mode Input Voltage Range	V <sub>CC</sub> <sup>-</sup> -0.2 to V <sub>CC</sub> <sup>+</sup> +0.2	V

**ELECTRICAL CHARACTERISTICS**

$V_{CC}^+ = 3V$ ,  $V_{CC}^- = 0V$ ,  $R_L, C_L$  connected to  $V_{CC}/2$ ,  $T_{amb} = 25^\circ C$  (unless otherwise specified)

Symbol	Parameter	TS3V912/AI/BI			Unit	
		Min.	Typ.	Max.		
$V_{io}$	Input Offset Voltage ( $V_{ic} = V_o = V_{CC}/2$ ) $T_{min.} \leq T_{amb} \leq T_{max.}$	TS3V912 TS3V912A TS3V912B TS3V912 TS3V912A TS3V912B			10 5 2 12 7 3	mV
$DV_{io}$	Input Offset Voltage Drift		5			$\mu V/^\circ C$
$I_{io}$	Input Offset Current - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$		1		100 200	pA
$I_{ib}$	Input Bias Current - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$		1		150 300	pA
$I_{CC}$	Supply Current (per amplifier, $A_{VCL} = 1$ , no load) $T_{min.} \leq T_{amb} \leq T_{max.}$		200		300 400	$\mu A$
CMR	Common Mode Rejection Ratio $V_{ic} = 0$ to $3V$ , $V_o = 1.5V$		50	80		dB
SVR	Supply Voltage Rejection Ratio ( $V_{CC}^+ = 2.7$ to $3.3V$ , $V_o = V_{CC}/2$ )		50	80		dB
$A_{vd}$	Large Signal Voltage Gain ( $R_L = 10k\Omega$ , $V_o = 1.2V$ to $1.8V$ ) $T_{min.} \leq T_{amb} \leq T_{max.}$		3 3	10		V/mV
$V_{OH}$	High Level Output Voltage ( $V_{id} = 1V$ ) $T_{min.} \leq T_{amb} \leq T_{max.}$	$R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$  $R_L = 10k\Omega$ $R_L = 600\Omega$	2.95 2.9 2.3  2.8 2.1	2.96 2.6 2		V
$V_{OL}$	Low Level Output Voltage ( $V_{id} = -1V$ ) $T_{min.} \leq T_{amb} \leq T_{max.}$	$R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$  $R_L = 10k\Omega$ $R_L = 600\Omega$		30 300 900	50 70 400  100 600	mV
$I_o$	Output Short Circuit Current ( $V_{id} = \pm 1V$ )	Source ( $V_o = V_{CC}^-$ ) Sink ( $V_o = V_{CC}^+$ )	20 20	40 40		mA
GBP	Gain Bandwidth Product ( $A_{VCL} = 100$ , $R_L = 10k\Omega$ , $C_L = 100pF$ , $f = 100kHz$ )			0.8		MHz
$SR^+$	Slew Rate ( $A_{VCL} = 1$ , $R_L = 10k\Omega$ , $C_L = 100pF$ , $V_i = 1.3V$ to $1.7V$ )			0.3		V/ $\mu s$
$SR^-$	Slew Rate ( $A_{VCL} = 1$ , $R_L = 10k\Omega$ , $C_L = 100pF$ , $V_i = 1.3V$ to $1.7V$ )			0.4		V/ $\mu s$
$\phi_m$	Phase Margin			30		Degrees
$e_n$	Equivalent Input Noise Voltage ( $R_s = 100\Omega$ , $f = 1kHz$ )			30		$\frac{nV}{\sqrt{Hz}}$
$V_{O1}/V_{O2}$	Channel Separation ( $f = 1kHz$ )			120		dB

**Note 1** : Maximum values including unavoidable inaccuracies of the industrial test.

**ELECTRICAL CHARACTERISTICS**

$V_{CC}^+ = 5V, V_{CC}^- = 0V, R_L, C_L$  connected to  $V_{CC}/2, T_{amb} = 25^\circ C$  (unless otherwise specified)

Symbol	Parameter	TS3V912/AI/BI			Unit	
		Min.	Typ.	Max.		
$V_{io}$	Input Offset Voltage ( $V_{ic} = V_o = V_{CC}/2$ ) $T_{min.} \leq T_{amb} \leq T_{max.}$	TS3V912 TS3V912A TS3V912B TS3V912 TS3V912A TS3V912B			10 5 2 12 7 3	mV
$DV_{io}$	Input Offset Voltage Drift		5			$\mu V/^\circ C$
$I_{io}$	Input Offset Current - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$		1		100 200	pA
$I_{ib}$	Input Bias Current - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$		1		150 300	pA
$I_{CC}$	Supply Current (per amplifier, $A_{VCL} = 1$ , no load) $T_{min.} \leq T_{amb} \leq T_{max.}$		230		350 450	$\mu A$
CMR	Common Mode Rejection Ratio $V_{ic} = 1.5$ to $3.5V, V_o = 2.5V$		60	85		dB
SVR	Supply Voltage Rejection Ratio ( $V_{CC}^+ = 3$ to $5V, V_o = V_{CC}/2$ )		55	80		dB
$A_{vd}$	Large Signal Voltage Gain ( $R_L = 10k\Omega, V_o = 1.5V$ to $3.5V$ ) $T_{min.} \leq T_{amb} \leq T_{max.}$		10 7	50		V/mV
$V_{OH}$	High Level Output Voltage ( $V_{id} = 1V$ ) $T_{min.} \leq T_{amb} \leq T_{max.}$	$R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$  $R_L = 10k\Omega$ $R_L = 600\Omega$	4.95 4.9 4.25  4.8 4.1	4.95 4.55 3.7		V
$V_{OL}$	Low Level Output Voltage ( $V_{id} = -1V$ ) $T_{min.} \leq T_{amb} \leq T_{max.}$	$R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$  $R_L = 10k\Omega$ $R_L = 600\Omega$		40 350 1400	50 100 500  150 750	mV
$I_o$	Output Short Circuit Current ( $V_{id} = \pm 1V$ )	Source ( $V_o = V_{CC}^-$ ) Sink ( $V_o = V_{CC}^+$ )	45 45	65 65		mA
GBP	Gain Bandwidth Product ( $A_{VCL} = 100, R_L = 10k\Omega, C_L = 100pF, f = 100kHz$ )			1		MHz
$SR^+$	Slew Rate ( $A_{VCL} = 1, R_L = 10k\Omega, C_L = 100pF, V_i = 1V$ to $4V$ )			0.8		V/ $\mu s$
$SR^-$	Slew Rate ( $A_{VCL} = 1, R_L = 10k\Omega, C_L = 100pF, V_i = 1V$ to $4V$ )			0.6		V/ $\mu s$
$e_n$	Equivalent Input Noise Voltage ( $R_s = 100\Omega, f = 1kHz$ )			30		$\frac{nV}{\sqrt{Hz}}$
$V_{O1}/V_{O2}$	Channel Separation ( $f = 1kHz$ )			120		dB
$\phi_m$	Phase Margin			30		Degrees

**Note 1** : Maximum values including unavoidable inaccuracies of the industrial test.

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage

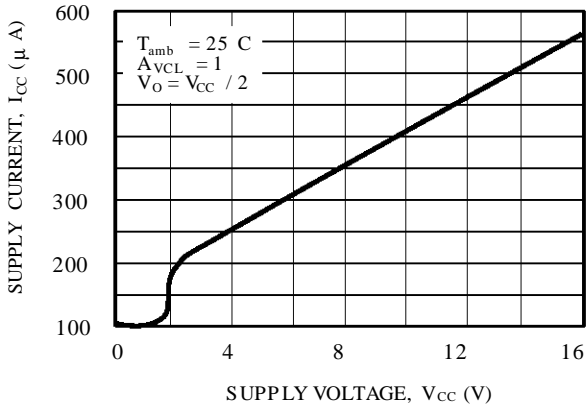


Figure 2 : Input Bias Current versus Temperature

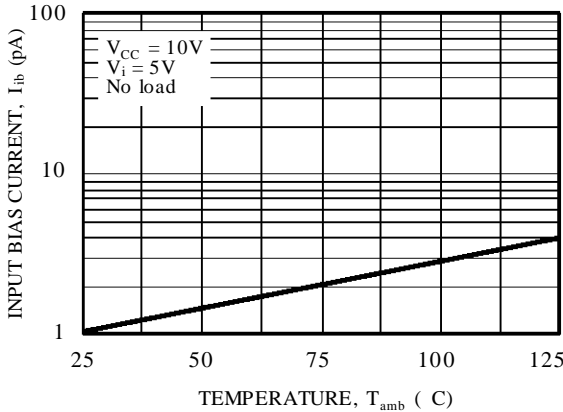


Figure 3a : High Level Output Voltage versus High Level Output Current

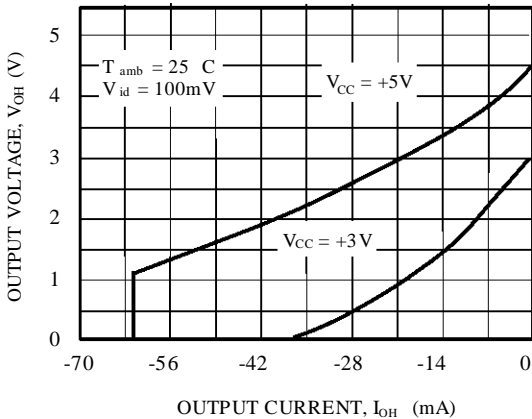


Figure 3b : High Level Output Voltage versus High Level Output Current

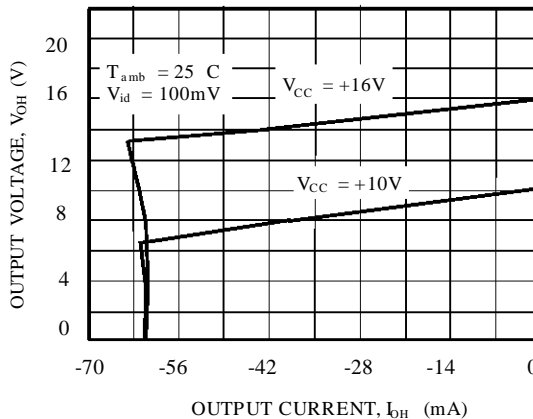


Figure 4a : Low Level Output Voltage versus Low Level Output Current

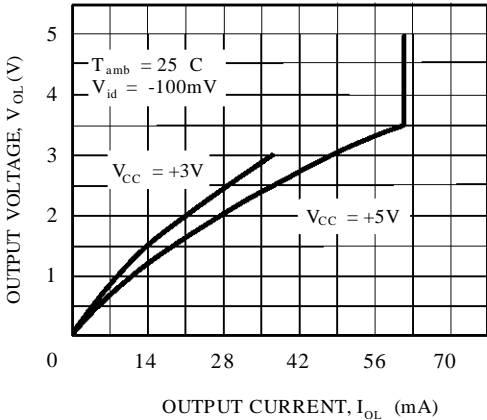
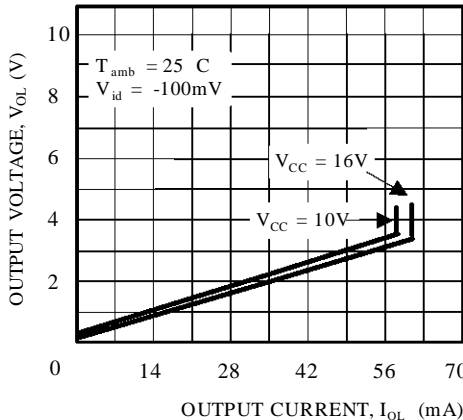
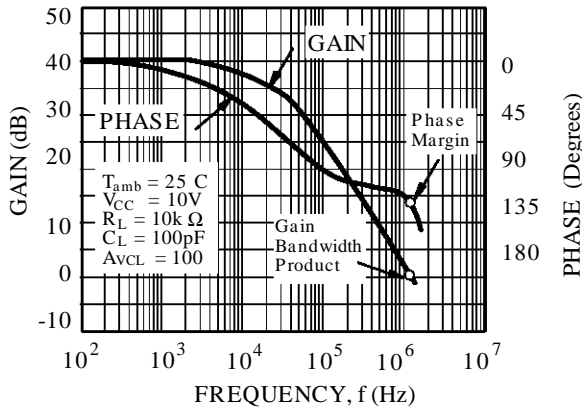


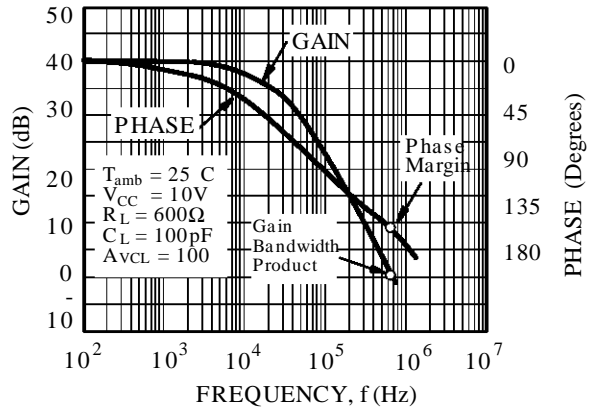
Figure 4b : Low Level Output Voltage versus Low Level Output Current



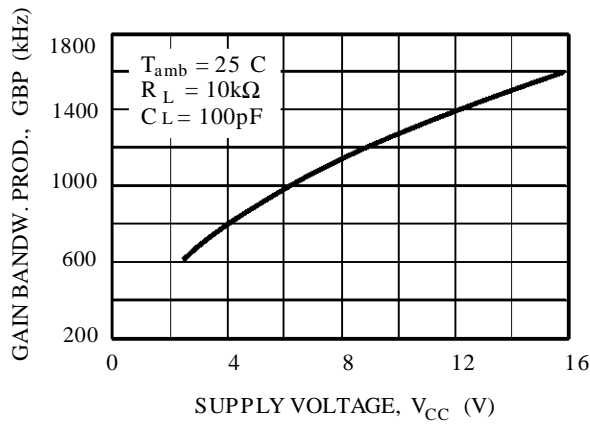
**Figure 5a :** Open Loop Frequency Response and Phase Shift



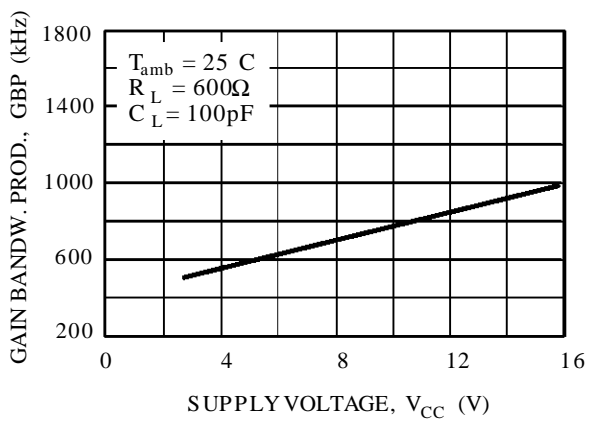
**Figure 5b :** Open Loop Frequency Response and Phase Shift



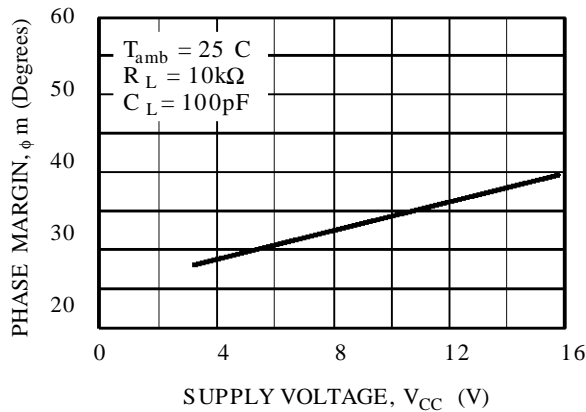
**Figure 6a :** Gain Bandwidth Product versus Supply Voltage



**Figure 6b :** Gain bandwidth Product versus Supply Voltage



**Figure 7a :** Phase Margin versus Supply Voltage



**Figure 7b :** Phase Margin versus Supply Voltage

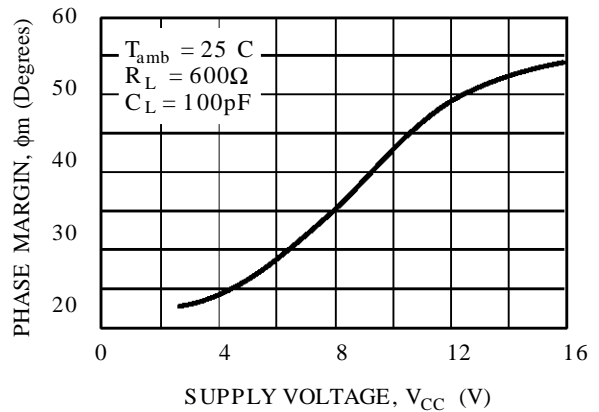
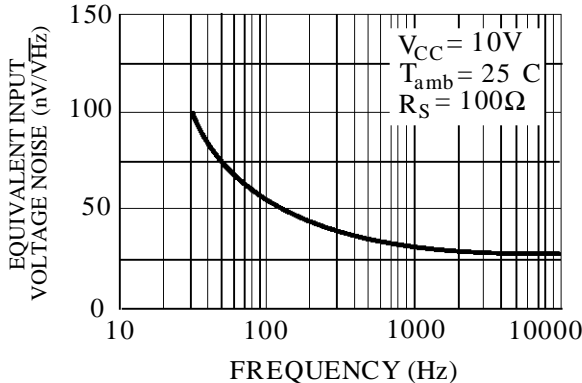
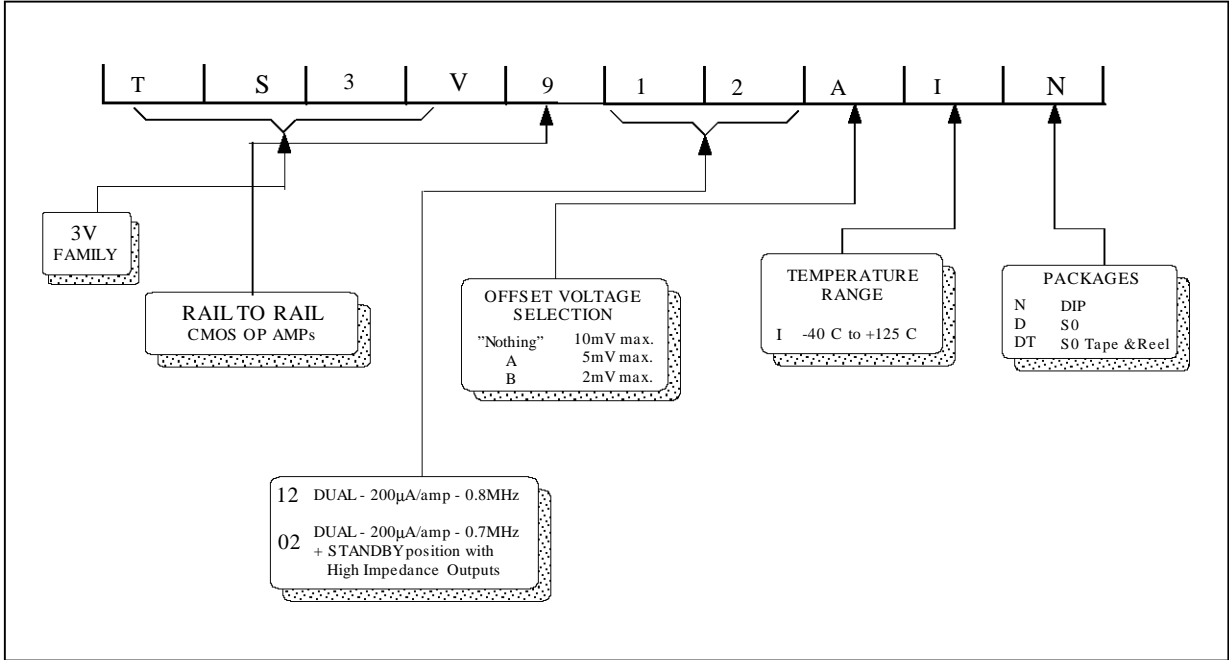


Figure 8 : Input Voltage Noise versus Frequency

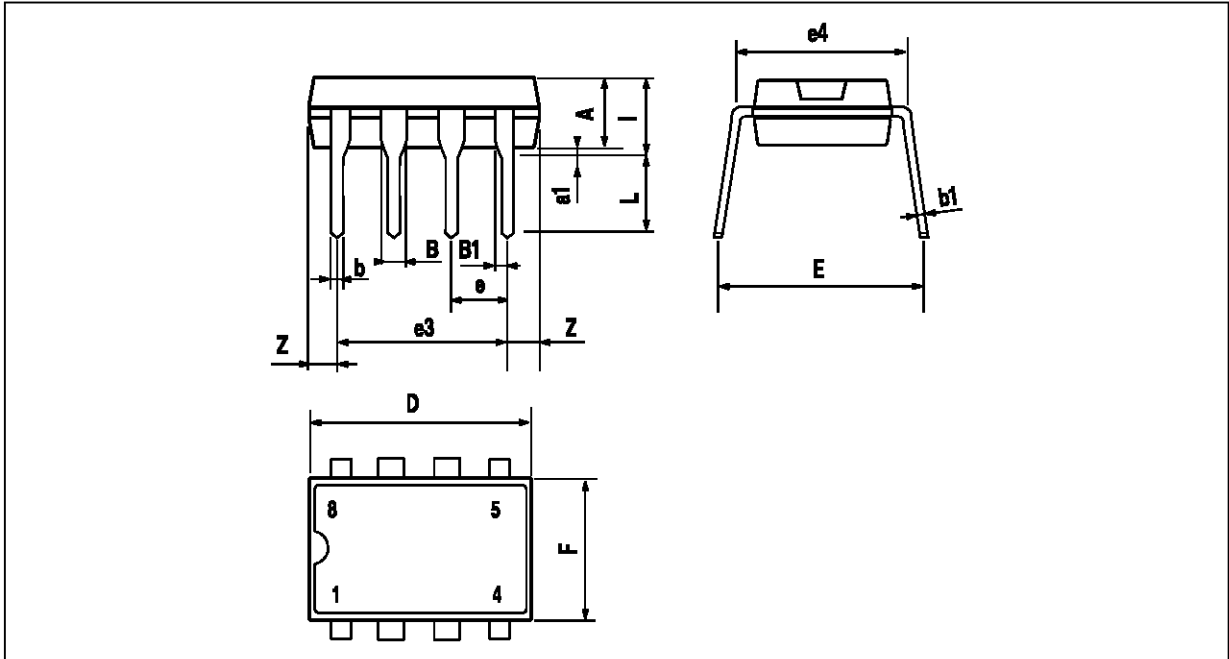


ORDERING INFORMATION



**TS3V912**

**PACKAGE MECHANICAL DATA**  
8 PINS - PLASTIC DIP



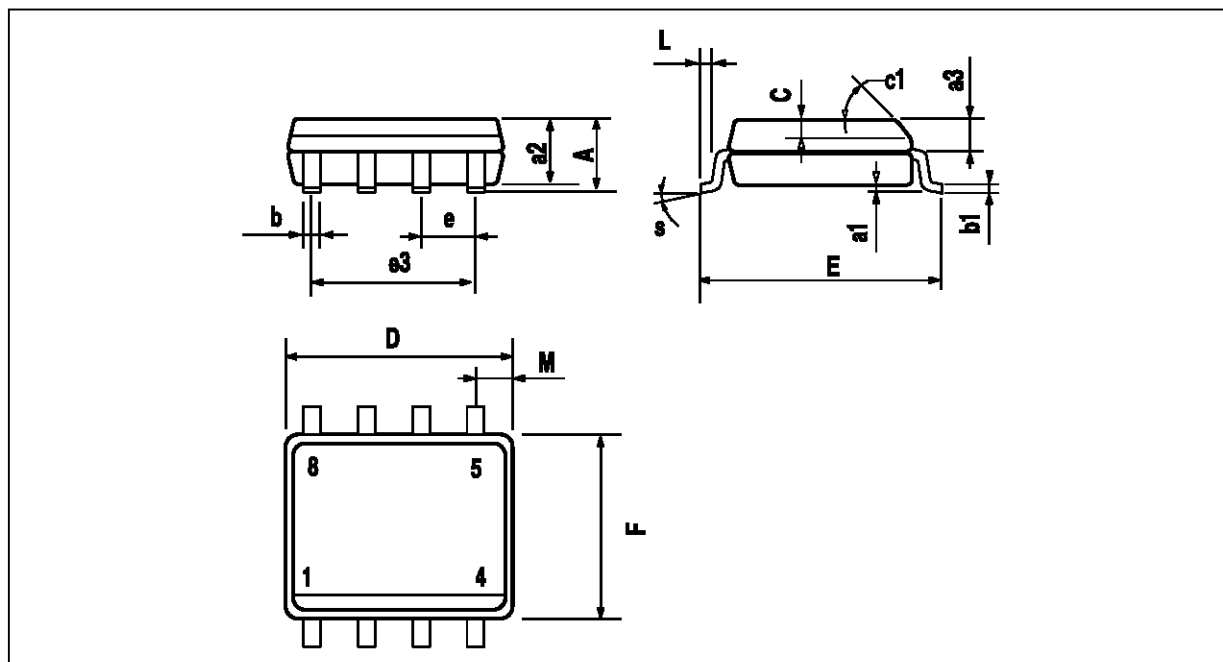
PM-DIP8-EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

DIP8.TBL



**PACKAGE MECHANICAL DATA**  
8 PINS - PLASTIC MICROPACKAGE (SO)



PM-SOR-EP-S

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

SOR-TEL

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