

5-V DUAL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV ESD PROTECTION

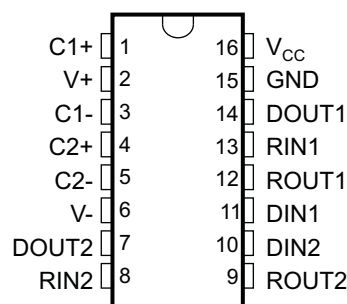
Check for Samples: [TRS202E](#)

FEATURES

- IEC61000-4-2 (Level 4) ESD Protection for RS-232 Bus Pins
 - ±8-kV Contact Discharge
 - ±15-kV Air-Gap Discharge
 - ±15-kV Human-Body Model
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates at 5-V V_{CC} Supply
- Operates Up To 120 kbit/s
- External Capacitors . . . $4 \times 0.1 \mu\text{F}$ or $4 \times 1 \mu\text{F}$
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

APPLICATIONS

- Battery-Powered Systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

D, DW, N, OR PW PACKAGE
(TOP VIEW)


DESCRIPTION/ORDERING INFORMATION

The TRS202E device consists of two line drivers, two line receivers, and a dual charge-pump circuit. TRS202E has IEC61000-4-2 (Level 4) ESD protection pin-to-pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. The device operates at data signaling rates up to 120 kbit/s and a maximum of 30-V/ μs driver output slew rate.

The TRS202E can work with both 0.1- μF or 1- μF external capacitors.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾ (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 25	TRS202ECN	TRS202ECN
	SOIC – D	Tube of 40	TRS202ECD	TRS202EC
		Reel of 2500	TRS202ECDR	
	SOIC – DW	Tube of 40	TRS202ECDW	TRS202EC
		Reel of 2000	TRS202ECDWR	
	TSSOP – PW	Tube of 90	TRS202EPW	RU02EC
Reel of 2000		TRS202EPWR		
–40°C to 85°C	PDIP – N	Tube of 25	TRS202EIN	TRS202EIN
	SOIC – D	Tube of 40	TRS202EID	TRS202EI
		Reel of 2500	TRS202EIDR	
	SOIC – DW	Tube of 40	TRS202EIDW	TRS202EI
		Reel of 2000	TRS202EIDWR	
	TSSOP – PW	Tube of 90	TRS202EIPW	RU02EI
Reel of 2000		TRS202EIPWR		

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

Each Driver⁽¹⁾

INPUT D _{IN}	OUTPUT D _{OUT}
L	H
H	L

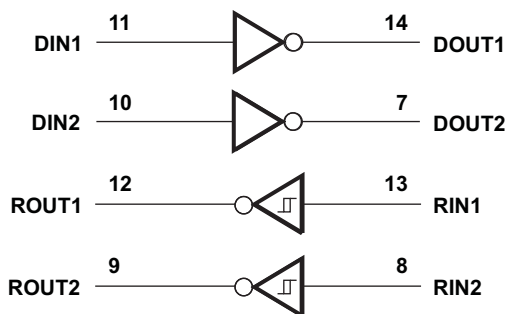
(1) H = high level, L = low level

Each Receiver⁽¹⁾

INPUT R _{IN}	OUTPUT R _{OUT}
L	H
H	L
Open	H

(1) H = high level, L = low level, Open = input disconnected or connected driver off

Figure 1. LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings^{(1) (2)}

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾	-0.3	6	V
V+	Positive charge pump voltage range ⁽²⁾	V _{CC} - 0.3	14	V
V-	Negative charge pump voltage range	-14	0.3	V
V _I	Input voltage range	Drivers	V+ + 0.3	V
		Receivers	±30	
V _O	Output voltage range	Drivers	V- - 0.3	V
		Receivers	-0.3	
D _{OUT}	Short-circuit duration	Continuous		
T _J	Operating virtual junction temperature	150		°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

Package Thermal Impedance

over operating free-air temperature range (unless otherwise noted)

		UNIT		
θ _{JA}	Package thermal impedance ^{(1) (2)}	D package	73	°C/W
		DW package	57	
		N package	67	
		PW package	108	

- (1) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is PD = (T_{J(max)} - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

(see [Figure 5](#))

		MIN	NOM	MAX	UNIT
Supply voltage		4.5	5	5.5	V
V _{IH}	Driver high-level input voltage	D _{IN}	2		V
V _{IL}	Driver low-level input voltage	D _{IN}		0.8	V
V _I	Driver input voltage	D _{IN}	0	5.5	V
	Receiver input voltage		-30	30	
T _A	Operating free-air temperature	TRS202EC	0	70	°C
		TRS202EI	-40	85	

- (1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 5 V ±0.5 V.

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT	
I _{CC}	Supply current	No load, V _{CC} = 5 V		8	15	mA

- (1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 5 V + 0.5 V.
- (2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

DRIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	D _{OUT} at R _L = 3 kΩ to GND, D _{IN} = GND	5	9		V
V _{OL}	Low-level output voltage	D _{OUT} at R _L = 3 kΩ to GND, D _{IN} = V _{CC}	-5	-9		V
I _{IH}	High-level input current	V _I = V _{CC}		15	200	μA
I _{IL}	Low-level input current	V _I at 0 V		-15	-200	μA
I _{OS} ⁽³⁾	Short-circuit output current	V _{CC} = 5.5 V V _O = 0 V		±10	±60	mA
r _o	Output resistance	V _{CC} , V+, and V- = 0 V V _O = ±2 V	300			Ω

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 5 V + 0.5 V.

(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
	Maximum data rate	C _L = 50 to 1000 pF, R _L = 3 kΩ to 7 kΩ, One D _{OUT} switching, See Figure 2	120			kbit/s
t _{PLH(D)}	Propagation delay time, low- to high-level output	C _L = 2500 pF, R _L = 3 kΩ, All drivers loaded, See Figure 2		2		μs
t _{PHL(D)}	Propagation delay time, high- to low-level output	C _L = 2500 pF, R _L = 3 kΩ, All drivers loaded, See Figure 2		2		μs
t _{sk(p)}	Pulse skew ⁽³⁾	C _L = 150 to 2500 pF, R _L = 3 kΩ to 7 kΩ, See Figure 3		300		ns
SR(tr)	Slew rate, transition region (see Figure 2)	C _L = 50 to 1000 pF, V _{CC} = 5 V, R _L = 3 kΩ to 7 kΩ,	3	6	30	V/μs

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 5 V + 0.5 V.

(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

ESD Protection

PIN	TEST CONDITIONS	TYP	UNIT
D _{OUT} , R _{IN}	Human-Body Model	±15	kV
	Contact Discharge	±8	
	Air-gap Discharge	±15	

RECEIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	3.5	V _{CC} - 0.4		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 5 V, T _A = 25°C		1.7	2.4	V
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 5 V, T _A = 25°C	0.8	1.2		V
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})		0.2	0.5	1	V
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 5 V + 0.5 V.

(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 4](#))

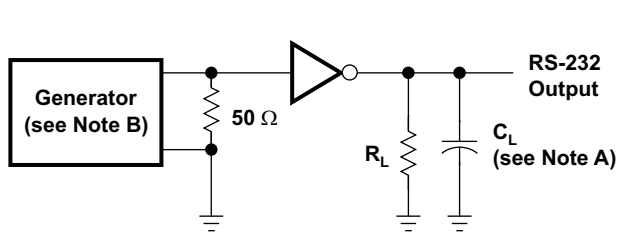
PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
t _{PLH(R)}	Propagation delay time, low- to high-level output	C _L = 150 pF		0.5	10	μs
t _{PHL(R)}	Propagation delay time, high- to low-level output	C _L = 150 pF		0.5	10	μs
t _{sk(p)}	Pulse skew ⁽³⁾			300		ns

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 5 V + 0.5 V.

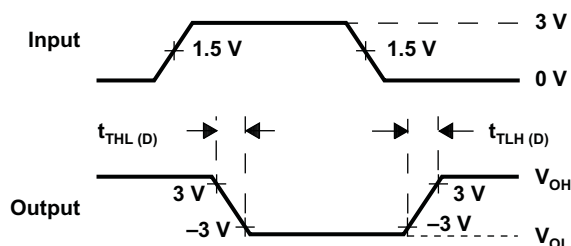
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

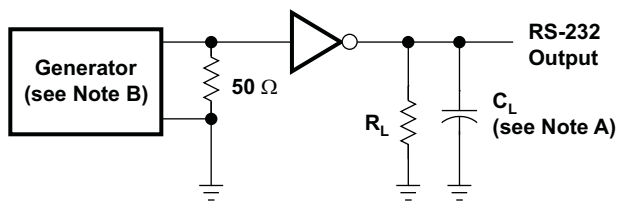


VOLTAGE WAVEFORMS

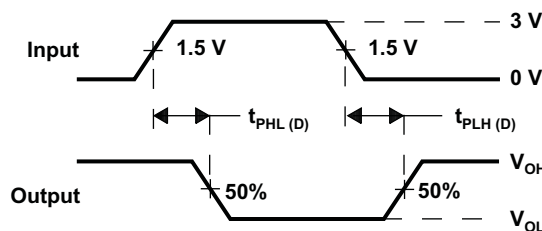
$$SR(t_f) = \frac{6\text{ V}}{t_{THL(D)} \text{ or } t_{TLH(D)}}$$

- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 120 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 2. Driver Slew Rate



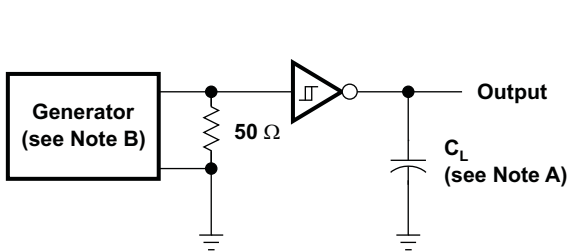
TEST CIRCUIT



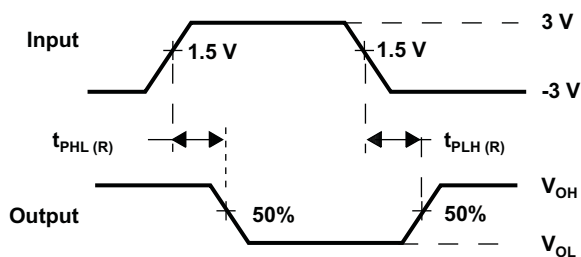
VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 120 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Driver Pulse Skew



TEST CIRCUIT

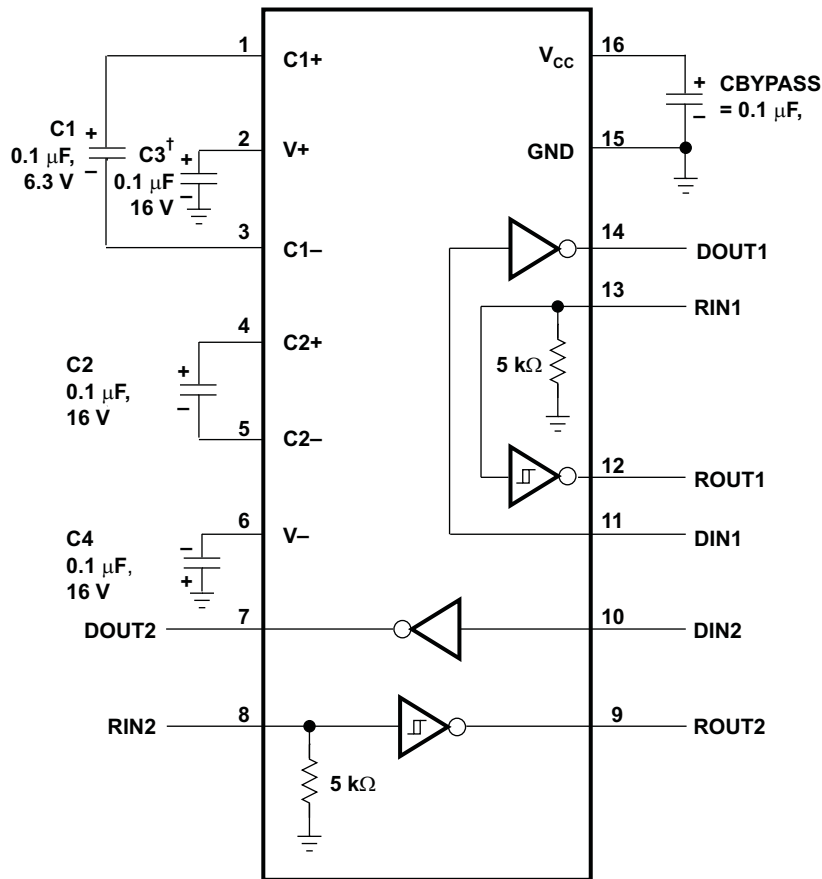


VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 4. Receiver Propagation Delay Times

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 5. Typical Operating Circuit and Capacitor Values

Capacitor Selection

The capacitor type used for C1-C4 is not critical for proper operation. The TRS202E requires 0.1-μF capacitors, although capacitors up to 10 μF can be used without harm. Ceramic dielectrics are suggested for the 0.1-μF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Use larger capacitors (up to 10 μF) to reduce the output impedance at V+ and V-.

Bypass V_{CC} to ground with at least 0.1 μF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1-C4).

ESD Protection

TI TRS202E devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15-kV when powered down.

ESD Test Conditions

Stringent ESD testing is performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 6. Figure 7 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the device under test (DUT) through a 1.5-kΩ resistor.

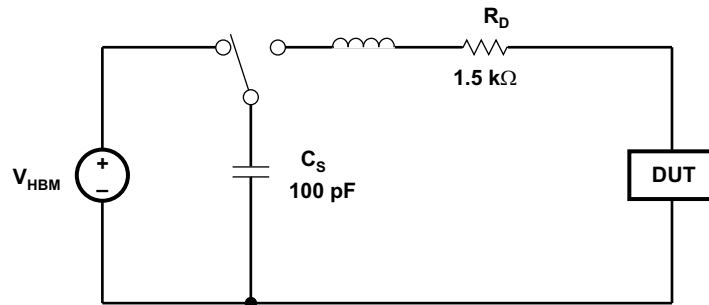


Figure 6. HBM ESD Test Circuit

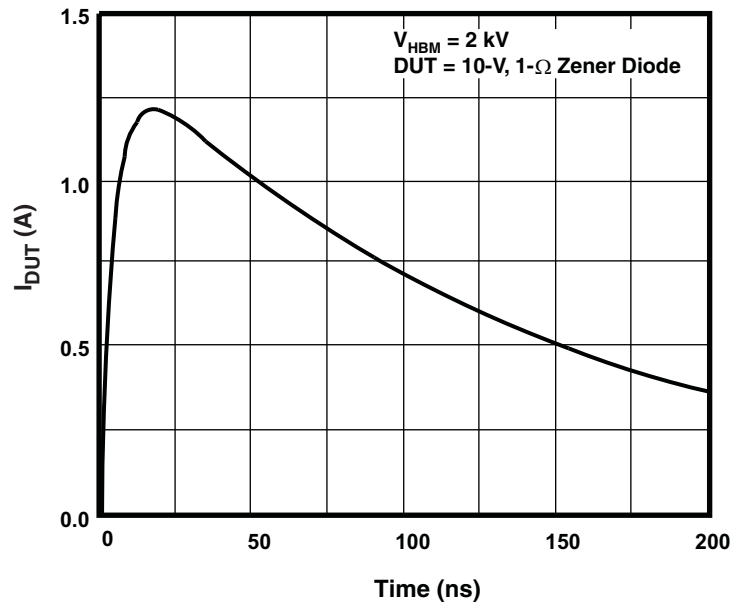


Figure 7. Typical HBM Current Waveform

Machine Model (MM)

The MM ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

REVISION HISTORY

Changes from Revision C (May 2010) to Revision D	Page
<hr/> <ul style="list-style-type: none">Fixed I_{OS} values typo in Electrical Characteristics table, changed – to ±.	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TRS202ECD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202ECDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202ECDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202ECDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202ECDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202ECDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202ECDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202ECDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202ECN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TRS202ECNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TRS202ECPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202ECPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202ECPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202ECPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202EID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202EIDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202EIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TRS202EIDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202EIDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202EIDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202EIDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202EIDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202EIN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TRS202EINE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TRS202EIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202EIPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202EIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TRS202EIPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS202ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS202ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS202ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS202EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS202EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS202EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS202ECDR	SOIC	D	16	2500	367.0	367.0	38.0
TRS202ECDWR	SOIC	DW	16	2000	367.0	367.0	38.0
TRS202ECPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TRS202EIDR	SOIC	D	16	2500	367.0	367.0	38.0
TRS202EIDWR	SOIC	DW	16	2000	367.0	367.0	38.0
TRS202EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

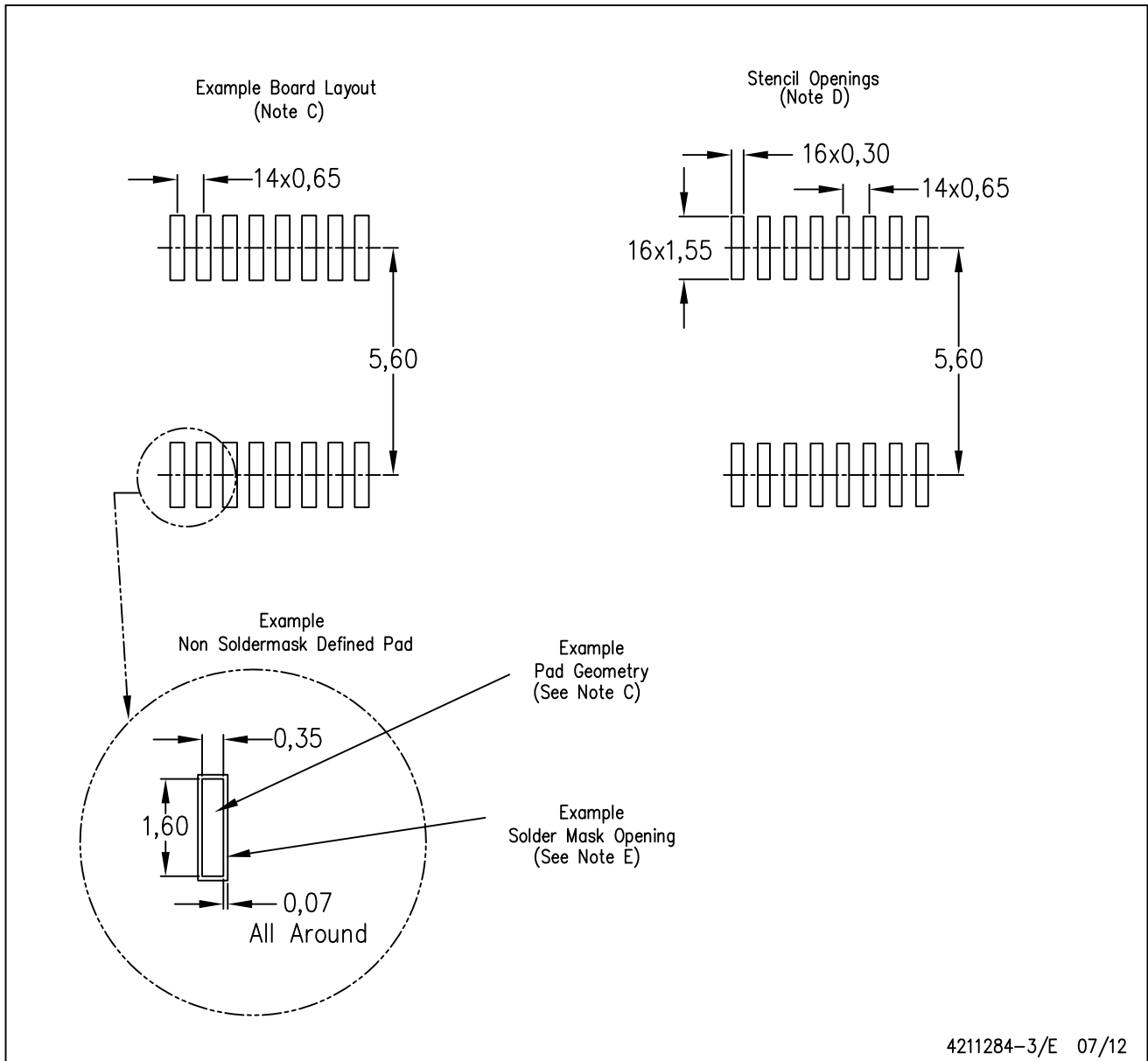


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

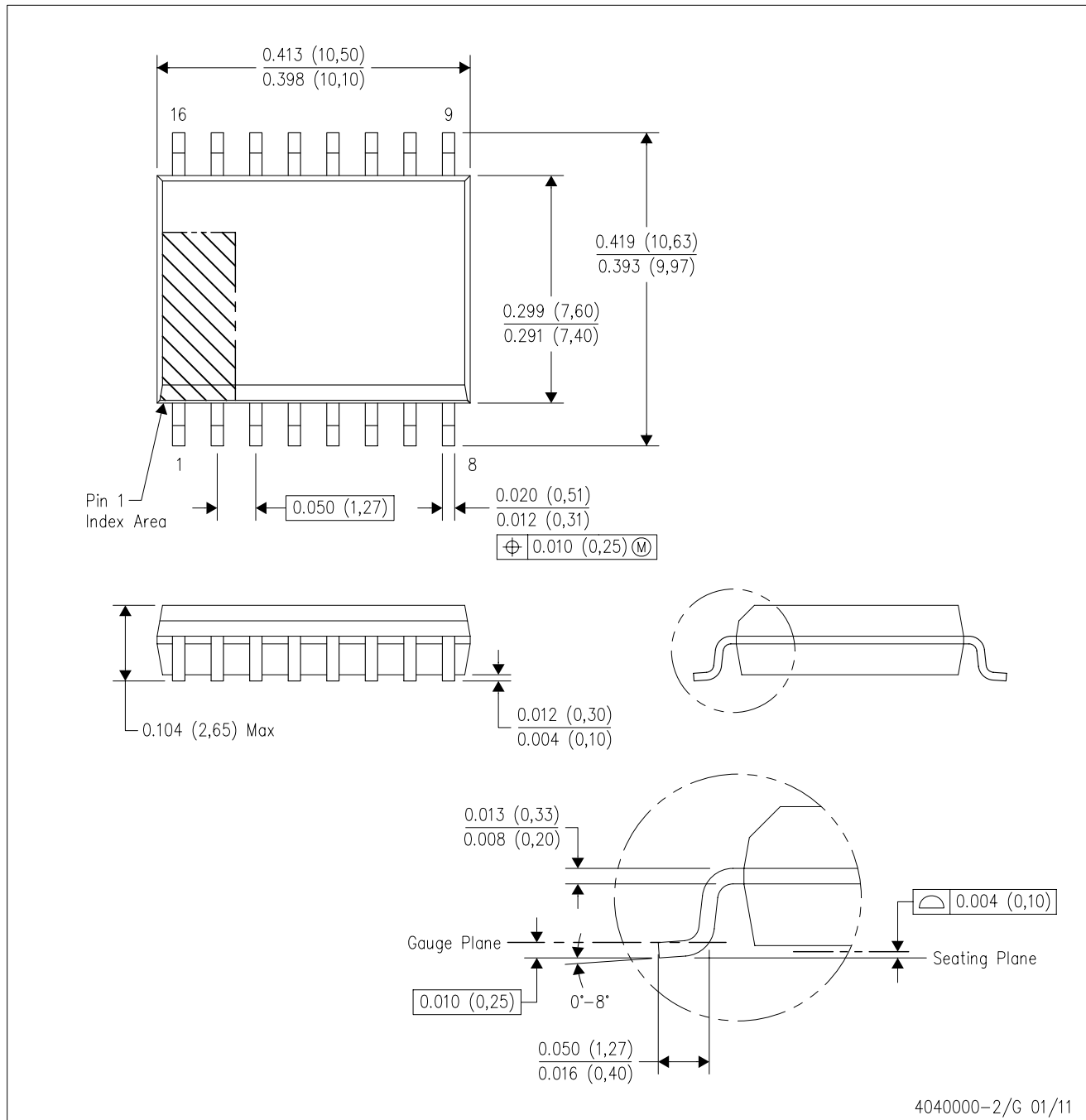
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R-PDSO-G16)

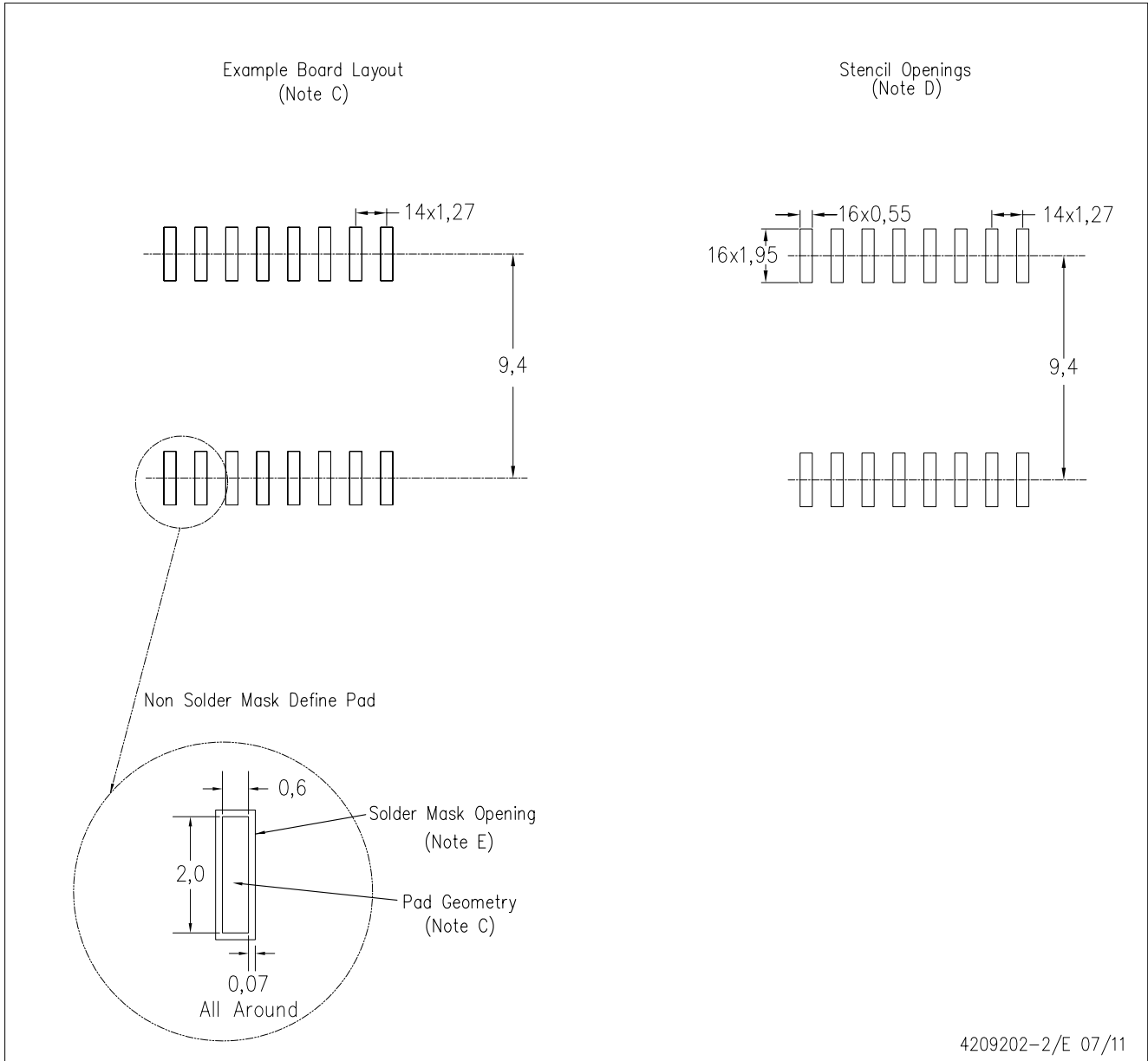
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AA.

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4209202-2/E 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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