Single-Channel, Push-Button Controller with Configurable Delay and Reset Pulse

Check for Samples: TPS3422

FEATURES

- **Very Small Package: 1.45-mm × 1-mm SON**
- **Single Input with Internal Pull-Up Resistor**
- **Low Supply Current: 250 nA**
  - **Two-State Logic User-Selectable Input Delay: 7.5 s and 0 s (for example) and so forth**
  - **Multiple Timing Options Available**
- **Fixed Timeout Pulse at $\overline{\text{RST}}$: 400 ms**
  - **Multiple Timing Options Available**
- **Active Low, Open-Drain Output**

APPLICATIONS

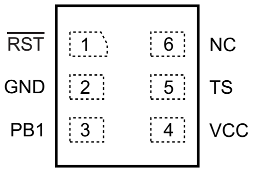
- **Smart Phones**
- **Tablets, Ultrabooks™**
- **Gaming Consoles**
- **Portable Consumer**
- **Navigation Devices**
- **Consumer Medical**
- **Network Routers**

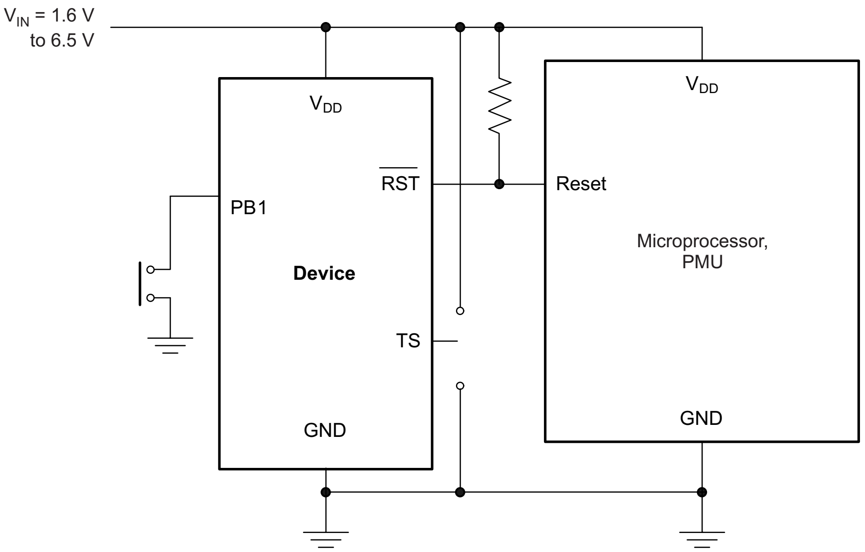
DESCRIPTION

The TPS3422 is a single-input, low-current, ultra small push-button reset timer device with a long timing setup delay to provide the intended system reset and avoid reset from short push-button closures or key presses. This reset configuration also allows for differentiation between software interrupts and hard system resets. The TPS3422 monitors one input ($\overline{\text{PB1}}$) and outputs an active low reset pulse signal ($\overline{\text{RST}}$) when PB1 is low for the selected time delay.

The TPS3422 has an open-drain input that can be wire-or'ed with other open-drain devices. The TPS3422 operates from 1.6 V to 6.5 V, over the –40°C to +125°C temperature range, and provides a precise, space-conscious micropower solution for system resetting needs.

DRY PACKAGE
1.45-mm x 1-mm SON
(TOP VIEW)





NOTE: Connect TS to V_{DD} or ground for different PB time delays.

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ORDERING INFORMATION

PRODUCT	DESCRIPTION
TPS3422**x y zzz a**	**X** is the push-button timer option. **Y** is the different reset timeout pulse option. **ZZZ** is the package designator. **A** is the tape or reel quantity.

ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Voltage	VCC	–0.3 to +7	V
	$\overline{\text{RST}}$	–0.3 to +7	V
	PB1	–0.3 to +7	V
	TS	–0.3 to VCC + 0.3	V
Current	$\overline{\text{RST}}$ pin	±20	mA
Temperature[2]	Operating junction, T_J	–40 to +125	°C
	Storage, T_{stg}	–65 to +150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)	2	kV
	Charge device model (CDM)	500	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute maximum- rated conditions for extended periods my affect device reliability.

(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

THERMAL INFORMATION

THERMAL METRIC[1]		TPS3422	UNITS
		DRY (µSON)	
		6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	TBD	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	TBD	
θ_{JB}	Junction-to-board thermal resistance	TBD	
ψ_{JT}	Junction-to-top characterization parameter	TBD	
ψ_{JB}	Junction-to-board characterization parameter	TBD	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	TBD	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

All specifications are over the operating temperature range of –40°C < T_J < +125°C and 1.6 V ≤ V_{CC} ≤ 6.5 V, unless otherwise noted. Typical values are at T_J = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Input supply range		1.6		6.5	V
I_{CC}	Supply current (standby)	V_{CC} = 3.3 V		250		nA
		V_{CC} = 6.5 V, T_J = –40°C to +85°C			1	µA
		V_{CC} = 6.5 V, T_J = –40°C to +125°C			TBD	µA
	Supply current (active timer)[1]	PB1 = 0 V, V_{CC} = 6.5 V, T_J = –40°C to +85°C		6	12	µA
		PB1 = 0 V, V_{CC} = 6.5 V, T_J = –40°C to +125°C			TBD	µA
V_{IH}	High-level input voltage	PB1	0.65 V_{CC}			V
V_{IL}	Low-level input voltage	PB1	0		0.25 V_{CC}	V
R_{PB1}	PB1 internal pull-up resistance		TBD	65	TBD	kΩ
V_{OL}	Low-level output voltage	V_{CC} > 4.5 V, I_{SINK} = 8 mA			0.3	V
		V_{CC} > 3.3 V, I_{SINK} = 5 mA			0.3	V
		V_{CC} > 1.6 V, I_{SINK} = 3 mA			0.3	V
$I_{lkg(OD)}$	Open-drain output leakage current	High impedance, $V_{\overline{RST}}$ = 6.5 V	–0.35		0.35	µA

(1) Excludes current through the pull-up resistor between the input and supply.

TIMING REQUIREMENTS

All specifications are over the operating temperature range of –40°C < T_J < +125°C and 1.6 V ≤ V_{CC} ≤ 6.5 V, unless otherwise noted. Typical values are at T_J = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{timer}	Push-button timer[1]		–10%		10%	
		TPS3422Ey: TS = GND	6.75	7.5	8.25	s
		TPS3422Ey: TS = V_{CC}		0		s
t_{rst}	Reset pulse		–10%		10%	
		TPS3422xG	360	400	440	ms
t_{dd}	Detection delay (from input to $\overline{RST}$)[2]	For 0-s t_{timer} condition		150		µs
	Start-up time[2]	V_{CC} rising		150		µs

(1) For the TPS3422xy devices with a 0-s delay while TS = V_{CC}, this option is only for factory testing and is not intended for normal operation. In normal operation, TS should be tied to GND.
(2) For the TPS3422xy devices with a 0-second delay when TS = V_{CC}, reset asserts in t_{dd} time when the PB1 input goes low in this configuration. During start up, if the PB1 input is low, reset asserts after a (t_{dd} + Start-up time) delay. This value is specified by design.

PRODUCT PREVIEW

PARAMETRIC MEASUREMENT INFORMATION

TIMING DIAGRAM

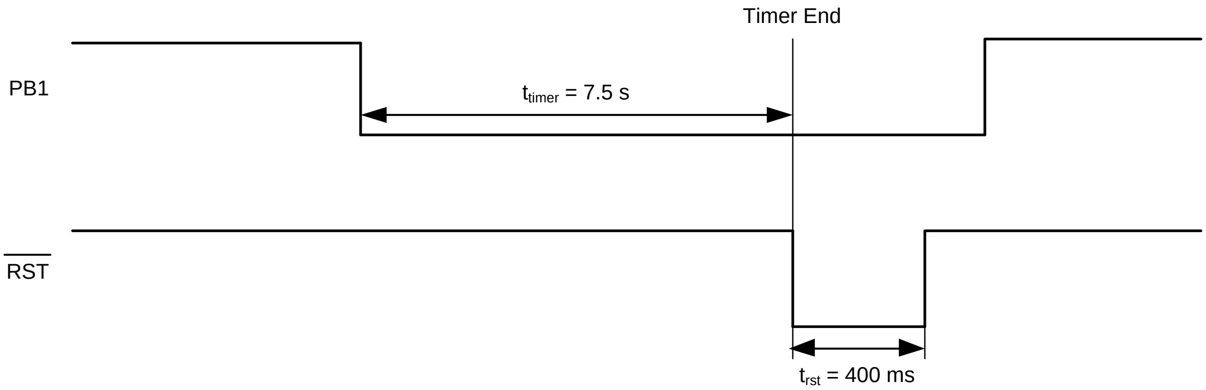
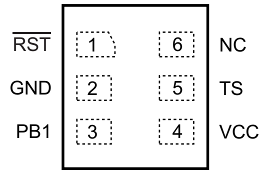


Figure 1. Timing Diagram

PIN CONFIGURATION

DRY PACKAGE
1.45-mm × 1-mm SON
(Top View)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	**NO.**	
GND	2	Ground
PB1	3	Push-button input. PB1 must be held low for greater than t_{timer} time to assert the reset output.
NC	6	No connection
$\overline{\text{RST}}$	1	Active low, open-drain output. Reset is asserted (goes low) for t_{rst} time when the push-button input is held low for greater than the t_{timer} time.
TS	5	Time delay selection input. Connect to V_{CC} or GND for different t_{timer} selections. In normal operation, the TS pin state should not be changed because it is intended to be either permanently at GND or V_{CC}. If switching the TS pin is required, it should only be done during power off.
VCC	4	Supply voltage input. Connect a 1.6-V to 5.5-V supply to VCC to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

FUNCTIONAL BLOCK DIAGRAM

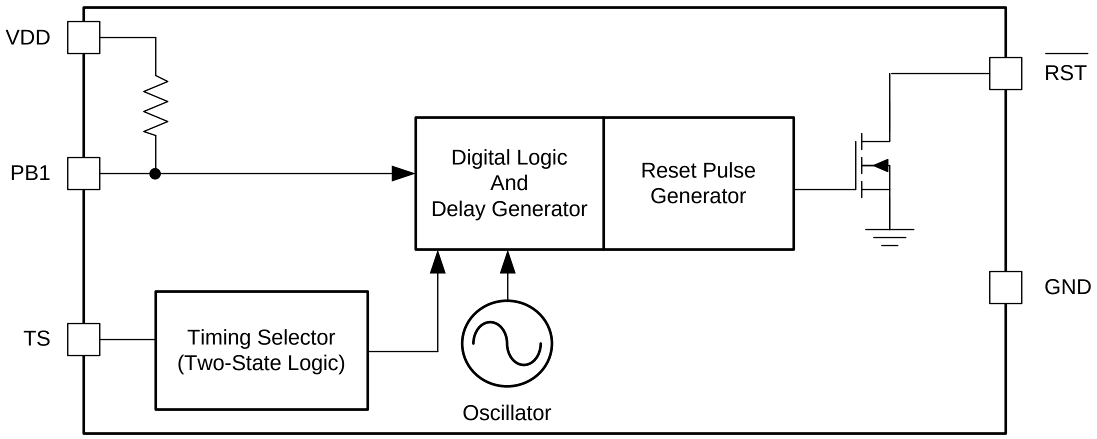


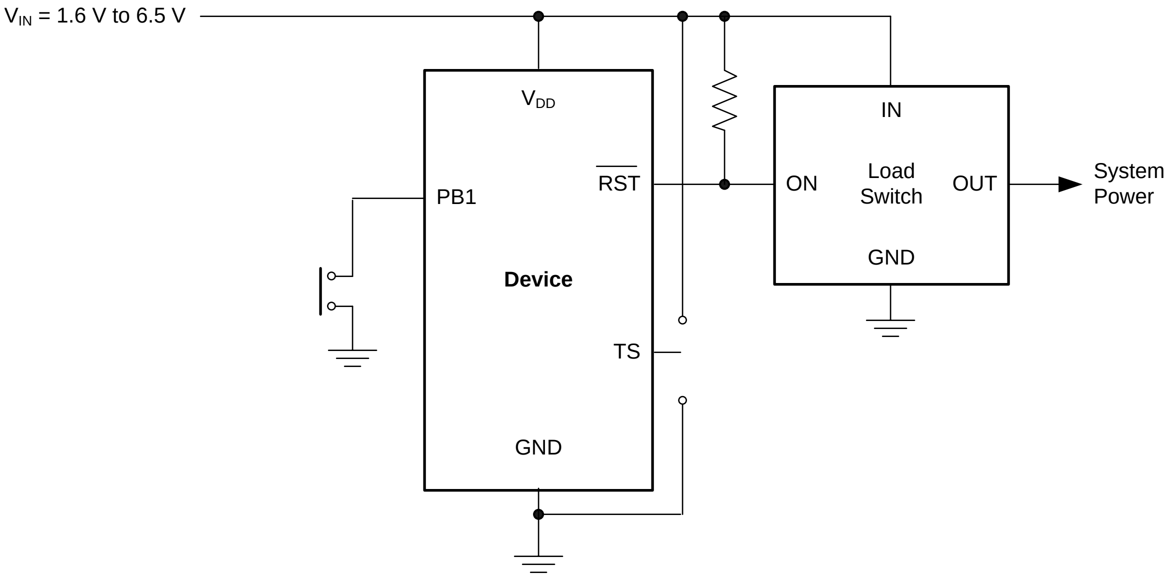
Figure 2. Block Diagram

GENERAL DESCRIPTION

The TPS3422 is a single-channel, push-button reset device with an extended setup period to prevent resets occurring from short-duration switch closures. The TPS3422 has an open-drain output that asserts for the reset timeout period when the PB1 input is held low for the push-button timer period. The TPS3422 also has a TS pin that selects between two different push-button timing options by connecting the pin to either GND or V_{CC}.

INPUT (PB1)

The TPS3422 has one input, PB1. PB1 has an internal pull-up resistor to V_{CC}. When input conditions are met (that is, when the input is held low for the push-button timer period, t_{timer}), the device asserts a single reset pulse of a fixed time (t_{rst}), as shown in Figure 3. Because t_{rst} is a fixed time pulse, reset de-assertion is independent of the input. A reset pulse occurs only one time after each valid input condition. The input pin must be released (goes high) and then driven low for the t_{timer} period before $\overline{RST}$ asserts again.



NOTE: Connect TS to V_{DD} or ground for different PB time delays.

Figure 3. Application Diagram

PUSH-BUTTON TIMER SELECTION (TS)

The TPS3422 offers two different t_{timer} options for system flexibility, with the use of the TS pin. Based on pin connection, connecting to GND or V_{CC} results in two different timing options.

During normal operation, the TS pin state should not be changed because TS is intended to be either permanently connected to GND or V_{CC}. The state of the TS pin is checked during power-up; therefore, if a different timing option is desired the state must be changed during power-off to avoid false operation.

OUTPUT ($\overline{\text{RST}}$)

The TPS3422 has an open-drain output. A pull-up resistor must be used to hold the line high when the output is in a high-impedance state (not asserted). By connecting a pull-up resistor to the proper voltage rail, the output can be connected to other devices at the correct interface voltage levels. The TPS3422 output can be pulled up to 6.5 V, independent of the device supply voltage. To ensure proper voltage levels, some thought should be given while choosing the pull-up resistor values. The pull-up resistor value is determined by V_{OL}, sink current capability, and output leakage current ($I_{lkg(OD)}$). These values are specified in the Electrical Charactersitcs table.

The *Input (PB1)* section describes how the output is asserted or deasserted. Refer to Figure 1 for a timing diagram that describes the relationship between the PB1 input and the output.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS3422EGDRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS3422EGDRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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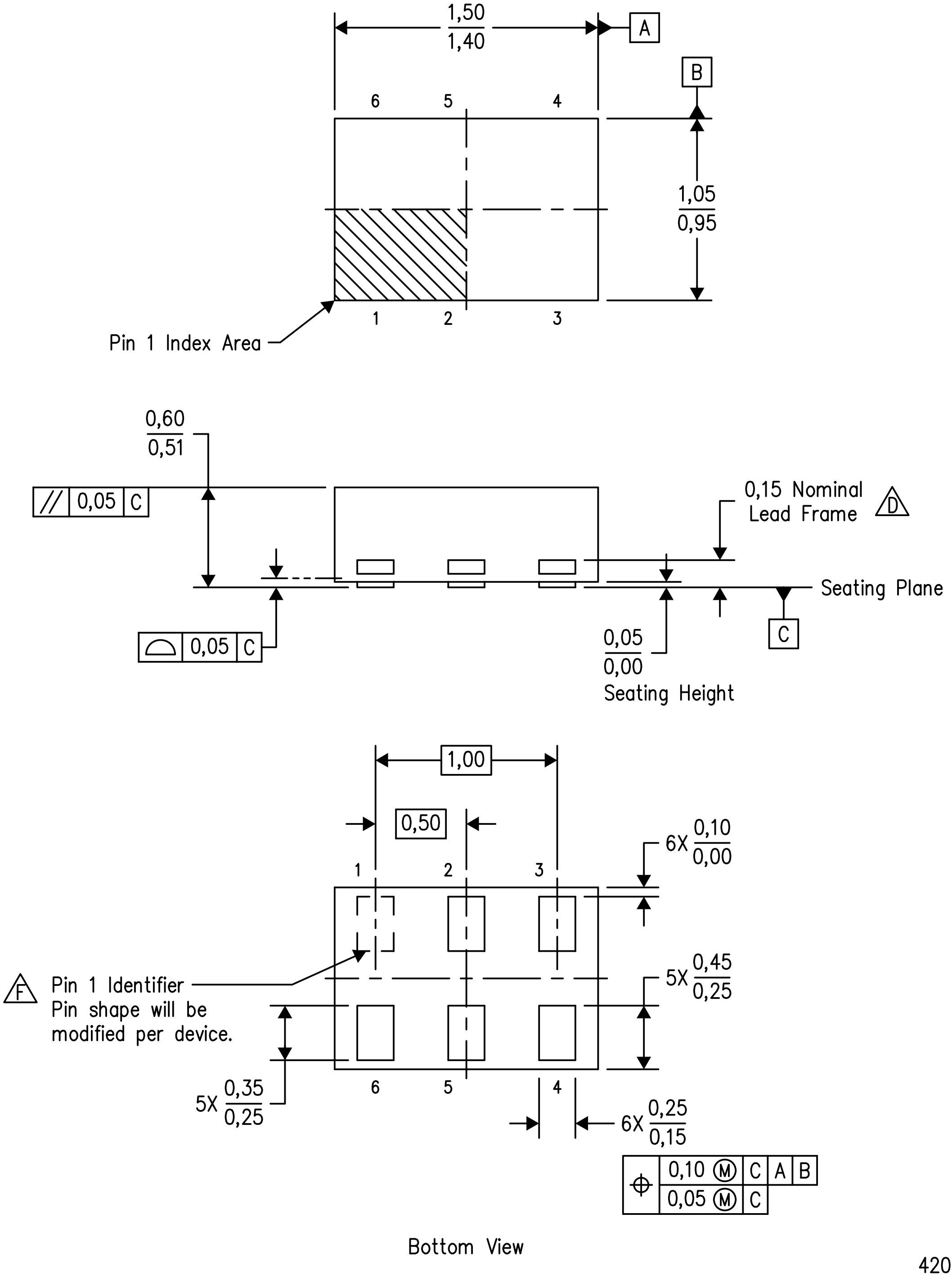
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No–Lead) package configuration.
- D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
- E. This package complies to JEDEC MO–287 variation UFAD.
- F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

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