# Dual-Channel, Push-Button Controller with Configurable Delay

**Check for Samples: TPS3420**

## FEATURES

- **Very Small Package: 1.45-mm × 1-mm SON**
- **Operating Range: 1.6 V to 6.5 V**
- **Dual Push-Button Inputs**
- **Two-State Logic User-Selectable Input Delay:**
  - **7.5 s and 0 s (for example) and so forth**
  - **Multiple Timing Options Available**
- **Low Supply Current: 450 nA**
- **Active Low, Open-Drain Output**

## APPLICATIONS

- **Smart Phones**
- **Tablets, Ultrabooks™**
- **Gaming Consoles**
- **Portable Consumer**
- **Navigation Devices**
- **Consumer Medical**
- **Network Routers**

## DESCRIPTION

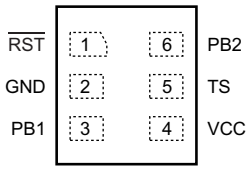
The TPS3420 is a dual-input, low-current, ultra small push-button reset timer device with a long timing setup delay to provide the intended system reset and avoid reset from short push-button closures or key presses. This reset configuration also allows for differentiation between software interrupts and hard system resets.

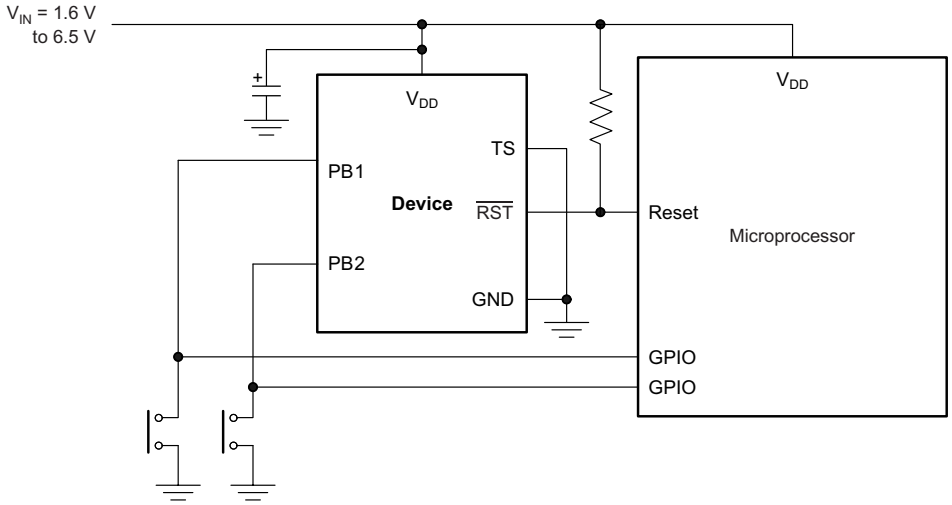
The TPS3420 monitors two inputs (PB1 and PB2) and outputs an active low reset pulse signal ($\overline{RST}$) when both inputs are low for the selected time delay. $\overline{RST}$ remains low until one of the PBx inputs is released. Using two inputs for ensuring reset also eliminates the need for a dedicated reset button.

The TPS3420 has two open-drain inputs that can be wire-or'ed with other open-drain devices. The TPS3420 operates from 1.6 V to 6.5 V, over the –40°C to +125°C temperature range, and provides a precise, space-conscious micropower solution for system resetting needs.

PRODUCT PREVIEW

**DRY PACKAGE**
**1.45-mm x 1-mm SON**
**(TOP VIEW)**




NOTE: Connect TS to $V_{DD}$ or GND for different PB time delays. Connect one of the PBx inputs to GND for use as a single-channel device.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

| PRODUCT | DESCRIPTION |
|---|---|
| TPS3420**x zzz a** | **X** is the push-button timer option.<br>**ZZZ** is the package designator.<br>**A** is the tape or reel quantity. |

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

| | | VALUE | UNIT |
|---|---|---|---|
| Voltage | VCC | –0.3 to +7 | V |
| | $\overline{RST}$ | –0.3 to +7 | V |
| | PB1, PB2 | –0.3 to +7 | V |
| | TS | –0.3 to VCC + 0.3 | V |
| Current | $\overline{RST}$ pin | ±20 | mA |
| Temperature(2) | Operating junction, $T_J$ | –40 to +125 | °C |
| | Storage, $T_{stg}$ | –65 to +150 | °C |
| Electrostatic discharge (ESD) ratings | Human body model (HBM) | 2 | kV |
| | Charge device model (CDM) | 500 | V |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute maximum- rated conditions for extended periods my affect device reliability.

(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TPS3420 DRY (µSON) 6 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | TBD | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | TBD | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | TBD | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | TBD | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | TBD | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | TBD | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PRODUCT PREVIEW

## ELECTRICAL CHARACTERISTICS

All specifications are over the operating temperature range of –40°C < $T_J$ < +125°C and 1.6 V ≤ $V_{CC}$ ≤ 6.5 V, unless otherwise noted. Typical values are at $T_J$ = +25°C and $V_{CC}$ = 3.3 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Input supply range | | 1.6 | | 6.5 | V |
| $I_{CC}$ | Supply current (standby) | $V_{CC}$ = 3.3 V | | 450 | | nA |
| | | $V_{CC}$ = 6.5 V, $T_J$ = –40°C to +85°C | | | 1.2 | µA |
| | | $V_{CC}$ = 6.5 V, $T_J$ = –40°C to +125°C | | | TBD | µA |
| | Supply current (active timer) | PB1, PB2 = 0 V, $V_{CC}$ = 6.5 V, $T_J$ = –40°C to +85°C | | 6 | 12 | µA |
| | | PB1, PB2 = 0 V, $V_{CC}$ = 6.5 V, $T_J$ = –40°C to +125°C | | | TBD | µA |
| $V_{IH}$ | High-level input voltage | PB1, PB2 | 0.85 | | | V |
| $V_{IL}$ | Low-level input voltage | PB1, PB2 | 0 | | 0.4 | V |
| $I_{PB}$ | Input current (PB1, PB2) | PB1, PB2 = 0 V to 6.5 V | –50 | | 50 | nA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ > 4.5 V, $I_{SINK}$ = 8 mA | | | 0.3 | V |
| | | $V_{CC}$ > 3.3 V, $I_{SINK}$ = 5 mA | | | 0.3 | V |
| | | $V_{CC}$ > 1.6 V, $I_{SINK}$ = 3 mA | | | 0.3 | V |
| $I_{lkg(OD)}$ | Open-drain output leakage current | High impedance, $V_{\overline{RST}}$ = 6.5 V | –0.35 | | 0.35 | µA |

## TIMING REQUIREMENTS

All specifications are over the operating temperature range of –40°C < $T_J$ < +125°C and 1.6 V ≤ $V_{CC}$ ≤ 6.5 V, unless otherwise noted. Typical values are at $T_J$ = +25°C and $V_{CC}$ = 3.3 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{timer}$ | Push-button timer | | –10% | | 10% | |
| | | TPS3420Ey: TS = GND | 6.75 | 7.5 | 8.25 | s |
| | | TPS3420Ey: TS = $V_{CC}$ | 11.25 | 12.5 | 13.75 | s |

## PARAMETRIC MEASUREMENT INFORMATION

### TIMING DIAGRAM

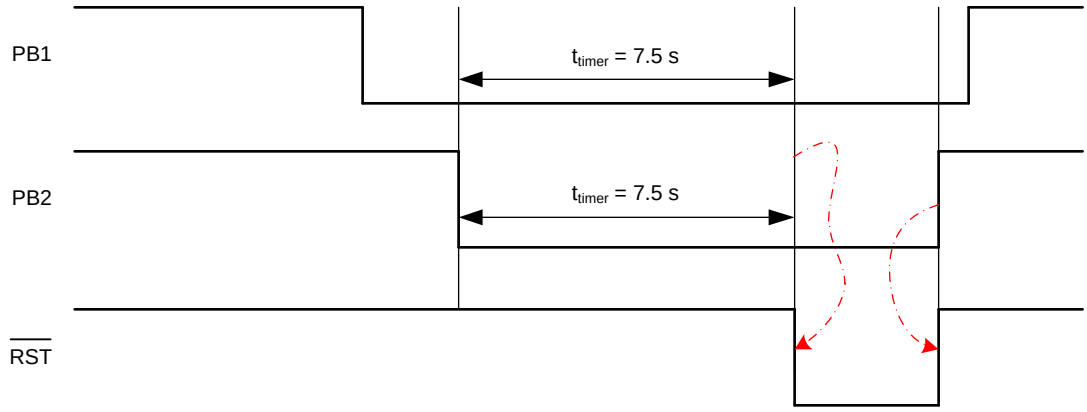
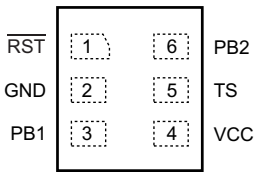



**Figure 1. Timing Diagram**

PRODUCT PREVIEW

## PIN CONFIGURATION

**DRY PACKAGE**
**1.45-mm × 1-mm SON**
**(Top View)**




## PIN DESCRIPTIONS

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| GND | 2 | Ground |
| PB1 | 3 | Push-button input. PB1 and PB2 must be held low for greater than $t_{timer}$ time to assert the reset output ($V_{IH}$ > 0.85 V, $V_{IL}$ < 0.4 V). |
| PB2 | 6 | Second push-button input. PB1 and PB2 must be held low for greater than $t_{timer}$ time to assert the reset output ($V_{IH}$ > 0.85 V, $V_{IL}$ < 0.4 V). |
| $\overline{RST}$ | 1 | Active low, open-drain output. Reset is asserted (goes low) when both push-button inputs are held low for greater than the $t_{timer}$ time. Reset is then de-asserted when either PBx input is high. |
| TS | 5 | Time delay selection input. Connect to $V_{CC}$ or GND for different $t_{timer}$ selections. In normal operation, the TS pin state should not be changed because it is intended to be either permanently at GND or $V_{CC}$. If switching the TS pin is required, it should only be done during power off. |
| VCC | 4 | Supply voltage input. Connect a 1.6-V to 5.5-V supply to VCC to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin. |

## FUNCTIONAL BLOCK DIAGRAM

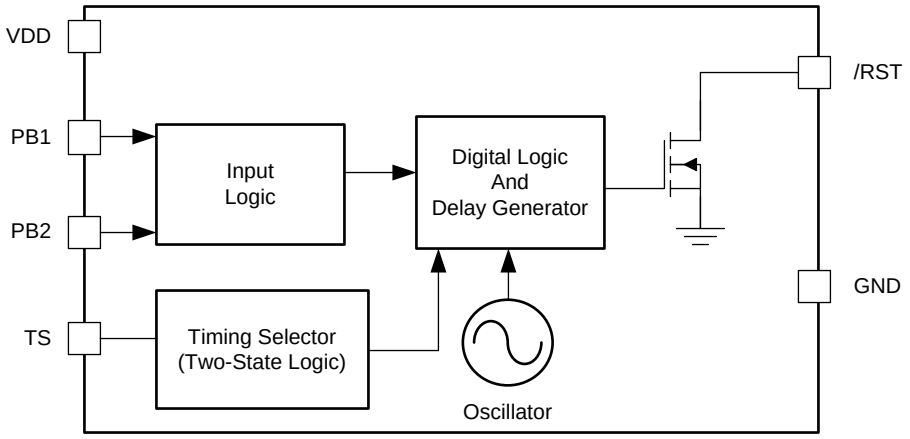



**Figure 2. Block Diagram**

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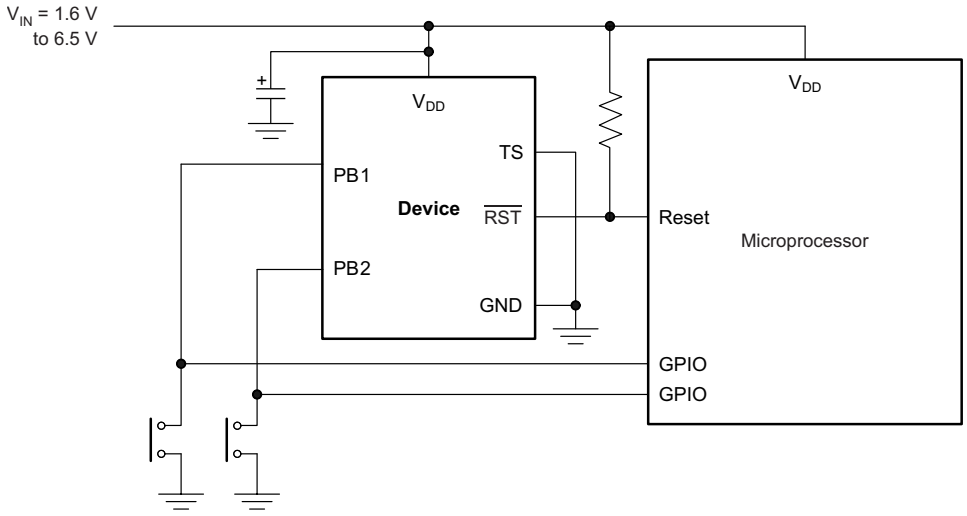
## GENERAL DESCRIPTION

The TPS3420 is a dual-channel, push-button reset device with an extended setup period to prevent resets occurring from short-duration switch closures. The TPS3420 has an open-drain output that asserts for the reset timeout period when both PB1 and PB2 inputs are held low for the push-button timer period. The TPS3420 also has a TS pin that selects between two different push-button timing options by connecting the pin to either GND or $V_{CC}$.

## INPUTS (PB1, PB2)

The TPS3420 has two inputs, PB1 and PB2. When input conditions are met (that is, when both inputs are simultaneously held low for the push-button timer period, $t_{timer}$), the device asserts a reset low, as shown in Figure 3. Reset de-assertion is dependent on either input going high. The reset pulse occurs only one time after each valid input condition. At least one input pin must be released (goes high) and then driven low for the $t_{timer}$ period before $\overline{RST}$ asserts again. One of the input pins can be permanently grounded for use as a single-channel device.




NOTE: Connect TS to $V_{DD}$ or ground for different PB time delays. Connect one PB input to ground for use as a single channel.

**Figure 3. Application Diagram**

PRODUCT PREVIEW

## PUSH-BUTTON TIMER SELECTION (TS)

The TPS3420 offers two different $t_{timer}$ options for system flexibility, with the use of the TS pin. Based on pin connection, connecting to GND or $V_{CC}$ results in two different timing options, as shown in Table 1.

During normal operation, the TS pin state should not be changed because TS is intended to be either permanently connected to GND or $V_{CC}$. The state of the TS pin is checked during power-up; therefore, if a different timing option is desired the state must be changed during power-off to avoid false operation.

**Table 1. Example Push-Button Timer Options**

| PRODUCT | PUSH-BUTTON TIMER (TS Pin) |
|---|---|
| TPS3420DDRYR | $V_{CC}$ = 12.5 s, GND = 7.5 s |
| TPS3420DDRYT | $V_{CC}$ = 12.5 s, GND = 7.5 s |

## OUTPUT ($\overline{RST}$)

The TPS3420 has an open-drain output. A pull-up resistor must be used to hold the line high when the output is in a high-impedance state (not asserted). By connecting a pull-up resistor to the proper voltage rail, the output can be connected to other devices at the correct interface voltage levels. The TPS3420 output can be pulled up to 6.5 V, independent of the device supply voltage. To ensure proper voltage levels, some thought should be given while choosing the pull-up resistor values. The pull-up resistor value is determined by $V_{OL}$, sink current capability, and output leakage current ($I_{lkg(OD)}$). These values are specified in the Electrical Charactersitcs table.

The *Inputs (PB1, PB2)* section describes how the output is asserted or deasserted. Refer to Figure 1 for a timing diagram that describes the relationship between the PB1 and PB2 inputs and the output.

PRODUCT PREVIEW

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| TPS3420DDRYR | PREVIEW | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TPS3420DDRYT | PREVIEW | SON | DRY | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

**(1)** The marketing status values are defined as follows:
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**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
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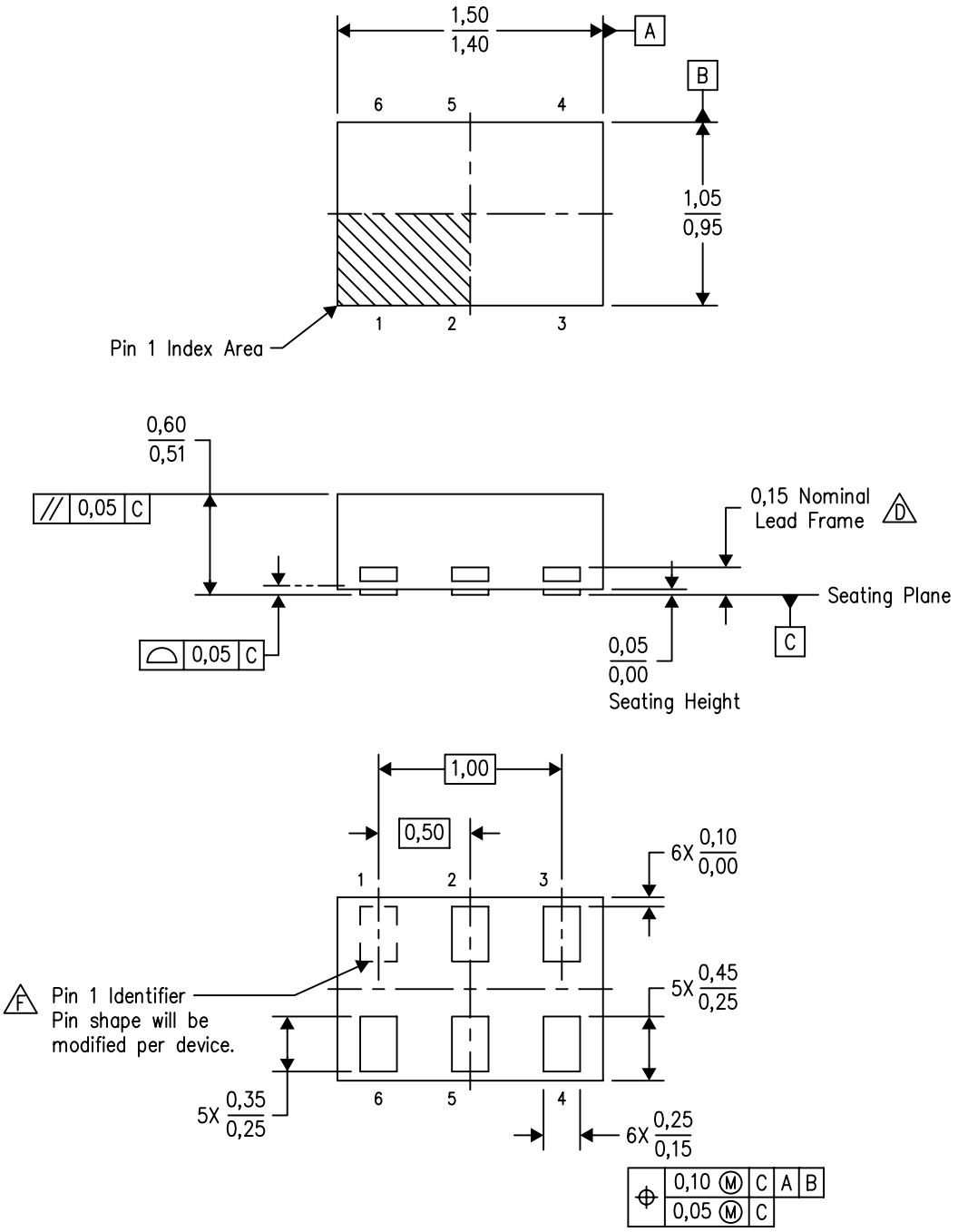
**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

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