National Semiconductor

TP3020, TP3020-1, TP3021, TP3021-1 Monolithic CODECs

General Description

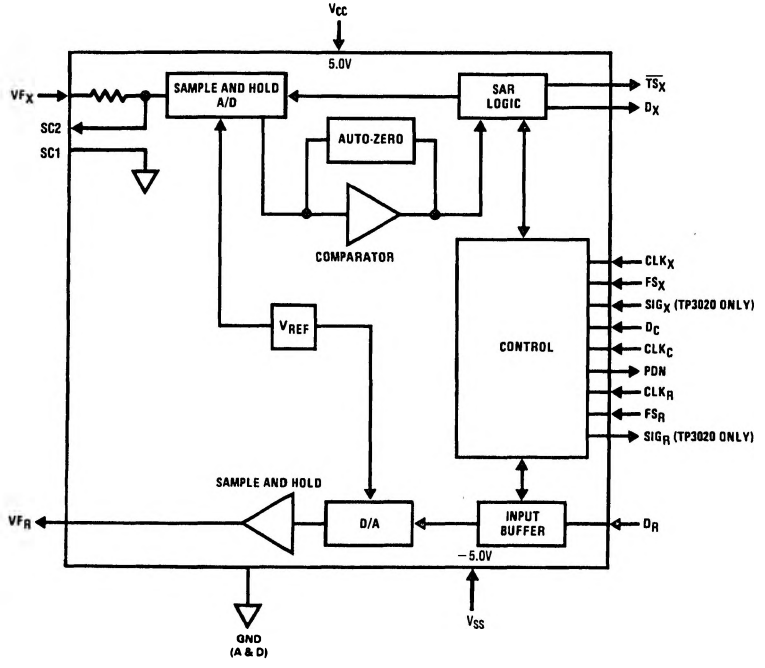
The TP3020 and TP3021 are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP3020 is intended for μ-law applications and contains logic for μ-law signaling insertion and extraction. The TP3021 is intended for A-law applications.

Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, a precision voltage reference and internal auto-zero circuit. A serial control port allows an external controller to individually assign the PCM input and output ports to one of up to 32 time slots or to place the CODEC into a power-down mode. Alternately, the TP3020/TP3021 may be operated in a fixed time slot mode. Both devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smoothes the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

- Low operation power—45 mW typical
- Low standby power—1 mW typical
- ±5V operation
- TTL compatible digital interface
- Time slot assignment or alternate fixed time slot modes
- Internal precision reference
- Internal sample and hold capacitors
- Internal auto-zero circuit
- TP3020—μ-law coding with signaling capabilities
- TP3021—A-law coding
- Synchronous or asynchronous operation

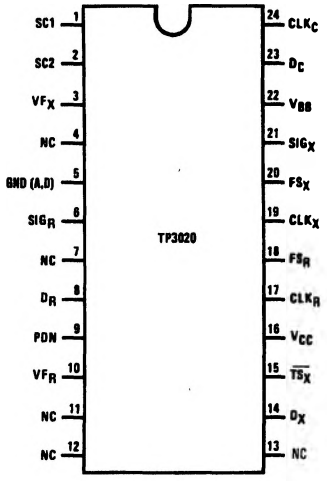
Simplified Block Diagram



TL/H/5538–1

Connection Diagrams

Dual-In-Line Package

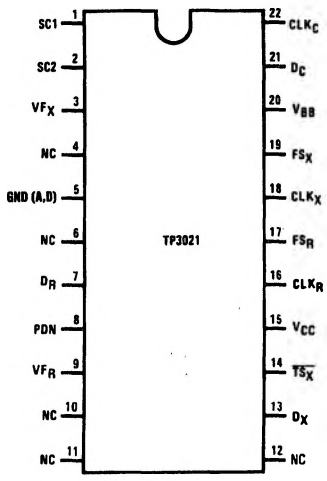


TL/H/5536–3

Top View

Order Number TP3020J or TP3020J-1
See NS Package Number J24A

Dual-In-Line Package



TL/H/5538–4

Top View

Order Number TP3021J or TP3021J-1
See NS Package Number J22A

Description of Pin Functions

Symbol	Function
SC1	Internally connected to GNDA.
SC2	Connects VF_X to an external sample/hold capacitor if fitted for use with pin-compatible NMOS CODECs. Ensures gain compatibility.
VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
GND	Analog and digital ground. All analog and digital signals are referenced to this pin.
SIG_R	Receive signaling bit output. During receive signaling frames the least significant (last) bit shifted into D_R is internally latched and appears at this output—SIG_R will then remain valid until changed during a subsequent receive signaling frame or reset by a power-down command.
D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
PDN	TTL output level which goes high when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel.
VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15 μS after the end of the decode time slot.

Symbol	Function
NC	Unused
D_X	Serial PCM TRI-STATE® output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external TRI-STATE bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
V_{CC}	5V ($\pm$5%) Power Supply.
CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536 MH_z, 1.544 MH_z or 2048 MHz. May be asynchronous with CLK_X or CLK_C.
FS_R	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_R cycle wide. Extending the width of FS_R to two or more cycles of CLK_R signifies a receive signaling frame.
CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with CLK_R or CLK_C.
FS_X	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_X cycle wide. Extending the width of FS_X to two or more cycles of CLK_X signifies a transmit signaling frame.

Description of Pin Functions (Continued)

Symbol	Function
SIG_X	Transmit signaling input. During a transmit signaling frame, the signal at SIG_X is shifted out of D_X in place of the least significant (last) bit of PCM data.
V_{BB}	−5V (±5%) input.
D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the TP3020/TP3021 into the fixed time slot mode.

Absolute Maximum Ratings

Operating Temperature	−25°C to + 125°C
Storage Temperature	−65°C to + 150°C
V_{CC} with Respect to GND	7V
V_{BB} with Respect to GND	−7V
ESD rating is to be determined.	
Voltage at Any Analog Input or Output	V_{BB} −0.3V to V_{CC} + 0.3V
Voltage at Any Digital Input or Output	GND −0.3V to V_{CC} + 0.3V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V and T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
I_I	Input Current	$0 < V_{IN} < V_{CC}$	**−10**		**10**	μA
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	D_X, I_{OL} = 4.0 mA			**0.4**	V
		SIG_R, I_{OL} = 0.5 mA			**0.4**	V
		$\overline{TS}_X$, I_{OL} = 3.2 mA, Open Drain			**0.4**	V
		PDN, I_{OL} = 1.6 mA			**0.4**	V
V_{OH}	Output High Voltage	D_X, I_{OH} = 6 mA	**2.4**			V
		SIG_R, I_{OH} = 0.6 mA	**2.4**			V
ANALOG INTERFACE						
Z_I	VF_X Input Impedance when Sampling	Resistance in Series with Approximately 70 pF	2.0			kΩ
Z_O	Output Impedance at VF_R	$-3.1V < VF_R < 3.1V$		10	20	Ω
V_{OS}	Output Offset Voltage at VF_R	D_R = PCM Zero Code (TP3020) or Alternating ± 1 Code (TP3021)	**−25**		**25**	mV
I_{IN}	Analog Input Bias Current	V_{IN} = 0V	−0.1		0.1	μA
R1 × C1	DC Blocking Time Constant		4.0			ms
C1	DC Blocking Capacitor		0.1			μF
R1	Input Bias Resistor				160	kΩ
POWER DISSIPATION						
I_{CC0}	Standby Current, V_{CC}			0.1	**0.4**	mA
I_{BB0}	Standby Current, V_{BB}			0.03	**0.1**	mA
I_{CC1}	Operating Current, V_{CC}			4.5	**8.0**	mA
I_{BB1}	Operating Current, V_{BB}			4.5	**8.0**	mA

AC Electrical Characteristics

Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected. Limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Absolute Level	The nominal 0 dBm0 levels for the TP3020 and TP3021 are 1.520 Vrms and 1.525 Vrms respectively. The resulting nominal overload level is 3.096V peak for both devices. All gain measurements for the encode and decode portions of the TP3020/TP3021 are based on these nominal levels after the necessary sin x/x corrections are made.				
G_{RA}	Receive Gain, Absolute TP3020, TP3021 TP3020-1, TP3021-1	T = 25°C, V_{CC} = 5V, V_{BB} = −5V	 **−0.125** **−0.175**		 **0.125** **0.175**	 dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	T = 0°C to 70°C	−0.05		0.05	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	V_{CC} = 5V ±5%, V_{BB} = −5V ±5%	**−0.07**		**0.07**	dB
G_{XA}	Transmit Gain, Absolute TP3020, TP3021 TP3020-1, TP3021-1	T = 25°C, V_{CC} = 5V, V_{BB} = −5V	 **−0.325** **−0.375**		 **−0.075** **−0.025**	 dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	T = 0°C to 70°C	−0.05		0.05	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	V_{CC} = 5V ±5%, V_{BB} = −5V ±5%	**−0.07**		**0.07**	dB
G_{RAL}	Absolute Receive Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 **−0.3** **−0.2** **−0.4** **−1.0**		 **0.3** **0.2** **0.4** **1.0**	 dB dB dB dB
G_{XAL}	Absolute Transmit Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 **−0.3** **−0.2** **−0.4** **−1.0**		 **0.3** **0.2** **0.4** **1.0**	 dB dB dB dB
S/D_R	Receive Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 **35** **29** **25**			 dBc dBc dBc
S/D_X	Transmit Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 **35** **29** **25**			 dBc dBc dBc
N_R	Receive Idle Channel Noise	D_R = Steady State PCM Code			**6**	dBrnc0
N_X	Transmit Idle Channel Noise	TP3020, (No Signaling) TP3021 (Note 1)			**13** **−66***	dBrnc0 dBn0p
HD_R	Receive Harmonic Distortion	2nd or 3rd Harmonic			**−47**	dB
HD_X	Transmit Harmonic Distortion	2nd or 3rd Harmonic			**−47**	dB
$PPSR_X$	Positive Power Supply Rejection, Transmit	Input Level = 0V, V_{CC} = 5.0 V_{DC} + 300 mVrms, f = 1.02 kHz	**50**			dB

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0 level.

AC Electrical Characteristics (Continued)

Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected. Limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$PPSR_R$	Positive Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{CC} = 5.0 V_{DC} + 300 mVrms, F = 1.02 kHz	**40**			dB
$NPSR_X$	Negative Power Supply Rejection, Transmit	Input Level = 0V, V_{BB} = −5.0 V_{DC} + 300 mVrms, f = 1.02 kHz	**50**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{BB} = −5.0 V_{DC} + 300 mVrms, f = = 1.02 kHz	**45**			dB
CT_{XR}	Transmit to Receive Crosstalk	D_R = Steady PCM Code			**−75**	dB
CT_{RX}	Receive to Transmit Crosstalk	Transmit Input Level = 0V TP3020 TP3021			**−70** **−65** (Note 2)	dB dB

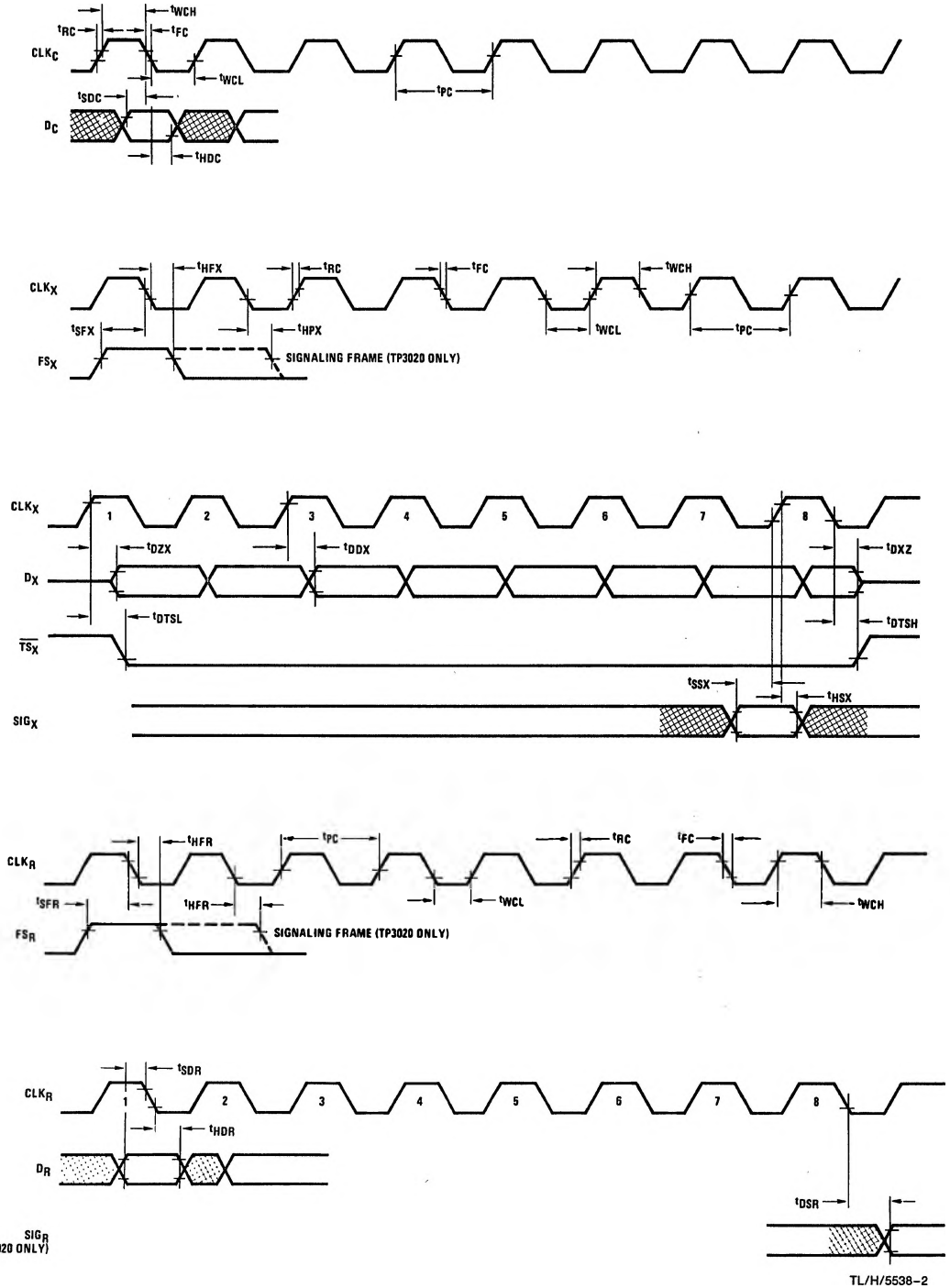
Note 2: Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.

Timing Specification

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All digital signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C. All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PC}	Period of Clock	CLK_C, CLK_R, CLK_X	**485**			ns
t_{RC}, t_{FC}	Rise and Fall Time of Clock	CLK_C, CLK_R, CLK_X			30	ns
t_{WCH}	Width of Clock High	CLK_C, CLK_R, CLK_X	**165**			ns
t_{WCL}	Width of Clock Low	CLK_C, CLK_R, CLK_X	**165**			ns
$t_{A/D}$	A/D Conversion Time	From End of Encoder Time Slot to Completion of Conversion			**16**	Time Slots
$t_{D/A}$	D/A Conversion Time	From End of Decoder Time Slot to Transition of VF_R			**2**	Time Slots
t_{SDC}	Set-Up Time, D_C to CLK_C		**100**			ns
t_{HDC}	Hold Time, CLK_C to DC		**100**			ns
t_{SFX}	Set-Up Time, FS_X to CLK_X		**100**			ns
t_{HFX}	Hold Time, CLK_X to FS_X		**100**			ns
t_{DZX}	Delay Time to Enable D_X on TS Entry	C_L = 150 pF	25		125	ns
t_{DDX}	Delay Time, CLK_X to D_X	C_L = 150 pF			**125**	ns
t_{DXZ}	Delay Time, D_X to High Impedance State on TS Exit	C_L = 0 pF	50		165	ns
t_{DTSL}	Delay to $\overline{TS}_X$ Low	0 ≤ C_L ≤ 150 pF	30		185	ns
t_{DTSH}	Delay to $\overline{TS}_X$ Off	C_L = 0 pF	30		185	ns
t_{SSX}	Set-Up Time, SIG_X to CLK_X		**100**			ns
t_{HSX}	Hold Time, CLK_X to SIG_X		**100**			ns
t_{SFR}	Set-Up Time, FS_R to CLK_R		**100**			ns
t_{HFR}	Hold Time, CLK_R to FS_R		**100**			ns
t_{SDR}	Set-Up Time, D_R to CLK_R		**40**			ns
t_{HDR}	Hold Time, CLK_R to D_R		**30**			ns
t_{DSR}	Delay Time, CLK_R to SIG_R	C_L = 100 pF			300	ns

Timing Waveforms



TL/H/5538–2

Functional Description

POWER-UP

Upon application of power, internal circuitry initializes the CODEC and places it into the power-down mode. No sequencing of 5V or −5V is required. In the power-down mode, all non-essential circuits are deactivated, the TRI-STATE PCM data output D_X is placed in the high impedance state and the receive signaling output of the TP3020, SIG_R, is reset to logical zero. Once in the power-down mode, the method of activating the TP3020/TP3021 depends on the chosen mode of operation, time slot assignment or fixed time slot.

TIME SLOT ASSIGNMENT MODE

The time slot assignment mode of operation is selected by maintaining CLK_C in a normally low state. The state of the CODEC is updated by pulsing CLK_C eight times within a period of 125 μS or less. The falling edge of each clock pulse shifts the data on the D_C input into the CODEC. The first two control bits determine if the subsequent control bits B3−B8 are to specify the time slot for the encoder (B1 = 0), the decoder (B2 = 0) or both (B1 and B2 = 0) or if the CODEC is to be placed into the power-down mode (B1 and B2 = 1). The desired action will take place upon the occurrence of the second frame sync pulse following the first pulse of CLK_C. Assigning a time slot to either the encoder or decoder will automatically power-up the entire CODEC circuit. The D_X output and D_R input, however, will be inhibited for one additional frame to allow the analog circuitry time to stabilize. If separate time slots are to be assigned to the encoder and the decoder, the encoder time slot should be assigned first. This is necessary because up to four frames are required to assign both time slots separately, but only three frames are necessary to activate the D_X output. If the encode time slot has not been updated the PCM data will be outputted during the previously assigned time slot which may now be assigned to another CODEC.

FIXED TIME SLOT MODE

There are several ways in which the TP3020/TP3021 may operate in the fixed time slot mode. The first and easiest method is to leave CLK_C disconnected or to connect CLK_C to V_{CC}. In this situation, D_C behaves as a power-down input. When D_C goes low, both encode and decode time slots are set to one on the second subsequent frame sync pulse. Time slot one corresponds to the eight CLK_X or CLK_R cycles starting one cycle from the nominal leading edge of FS_X or FS_R respectively. As in the time slot assignment mode, the D_X output is inhibited for one additional frame after the circuit is powered up. A logical "1" on D_C powers the CODEC down on the second subsequent FS_X pulse.

A second fixed time slot method is to operate CLK_C continuously. Placing a "1" on D_C will then cause the serial control register to fill up with ones. With B1 and B2 equal to "1" the CODEC will power-down. Placing a "0" on D_C will cause the serial control register to fill up with zeroes, assigning time slot one to both the encoder and decoder and powering up the device. One important restriction with this method of operation is that the rising transition of D_C must occur at least 8 cycles of CLK_c prior to FS_X. If this restriction is not followed, it is possible that on the frame prior to power-down, the encoder could be assigned to an incorrect time slot (e.g., 1, 3, 7, 15 or 31), resulting in a possible PCM bus conflict.

SERIAL CONTROL PORT

When the TP3020/TP3021 is operated in the time slot assignment mode or the fixed time slot mode with continuous clock, the data on D_C is shifted into the serial control register, bit 1 first. In the time slot assignment mode, depending on B1 and B2, the data in the RCV or XMT time slot registers is updated at the second FS_R or FS_X pulse after the first CLK_C pulse, or the CODEC is powered down. In the continuous clock fixed time slot mode, the CODEC is powered up or down at every second FS_R or FS_X pulse. The control register data is interpreted as follows:

B1	B2	Action
0	0	Assign time slot to encoder and decoder
0	1	Assign time slot to encoder
1	0	Assign time slot to decoder
1	1	Power-down CODEC

B3	B4	B5	B6	B7	B8	Time Slot
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	63
1	1	1	1	1	1	64

During the power-down command, bits 3 through 8 are ignored. Note that with 64 possible time slot assignments it is frequently possible to assign a time slot which does not exist. This can be useful to disable an encoder or decoder without powering down the CODEC.

SIGNALING

The TP3020 μ-law CODEC contains circuitry to insert and extract signaling information for the PCM data. The transmit signaling frame is signified by widening the FS_X pulse from one cycle of CLK_X to two or more cycles.

When this occurs, the data present on the SIG_X input at the eighth clock pulse of the encode time slot is inserted into the last bit of the PCM data stream. A receive signaling frame is indicated in a similar fashion by widening the FS_R pulse to two or more cycles of CLK_R.

During a receive signaling frame, the last PCM bit shifted in is latched into a flip-flop and appears at the SIG_R output. This output will remain unchanged until the next signaling frame, until a power-down is executed or until power is removed from the device. Since the least significant bit of the PCM data is lost during a signaling frame, the decoder interprets the bit as a "½" (i.e., half way between a "0" and a "1"). This minimizes the noise and distortion due to the signaling.

Functional Description (Continued)

ENCODING DELAY

The encoding process begins at the start of the encode time slot and is concluded no later than 17 time slots later. In normal applications, this PCM data is not shifted out until the next time slot 125 μS later, resulting in an encoding delay of 125 μS. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048 MHz clock, the FS rate could be increased to 15 kHz reducing the delay from 125 μS to 67 μS.

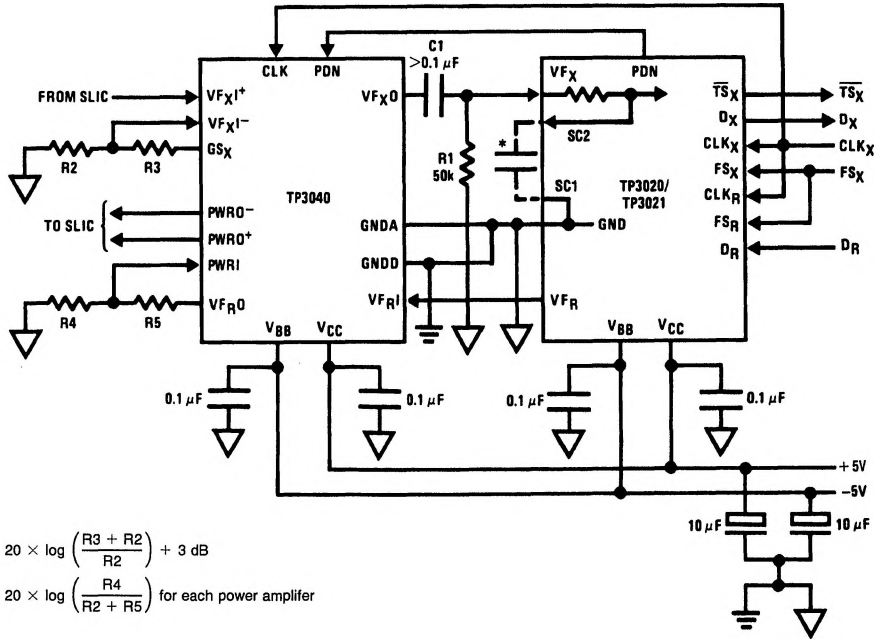
DECODING DELAY

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 CLK_R cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or 81 μS for a 1.544 MHz system with an 8 kHz frame rate or 76 μS for a 2.048 MHz system with an 8 kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

TYPICAL APPLICATION

A typical application of the TP3020/TP3021 used in conjunction with the TP3040 PCM filter is shown. The values of resistor R1 and DC blocking capacitor C1, are non-critical. The capacitor value should exceed 0.1 μF, R1 should not exceed 160 kΩ, and the product R1 × C1 should exceed 4 rms. 0.1 μf power supply bypass capacitors should be used and placed as close to the device as possible.

Typical Application



$$\text{XMT gain} = 20 \times \log\left(\frac{R3 + R2}{R2}\right) + 3\ \text{dB}$$

$$\text{RCV gain} = 20 \times \log\left(\frac{R4}{R2 + R5}\right) \text{ for each power amplifer}$$

TL/H/5538–5

The power supply decoupling capacitors should be 0.1 μF. In order to take advantage of the excellent noise performance of the TP3020/TP3021/TP3040, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines.

*The external sample/hold capacitor required for use with pin-compatible NMOS CODECs introduces attenuation due to the capacitive divider formed with C1. The SC pin connects VF_X to this sample/hold capacitor (via a 300Ω resistor) to ensure gain compatibility. The TP3020/TP3021 itself does not require an external sample/hold capacitor.