

# TL7757 SUPPLY-VOLTAGE SUPERVISOR AND PRECISION VOLTAGE DETECTOR

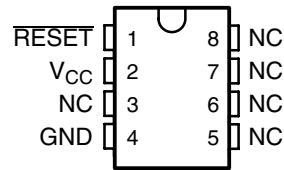
SLVS0411 – SEPTEMBER 1991 – REVISED AUGUST 2003

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- Low Standby Current . . . 20  $\mu$ A
- RESET Output Defined When  $V_{CC}$  Exceeds 1 V
- Precision Threshold Voltage 4.55 V  $\pm$ 120 mV
- High Output Sink Capability . . . 20 mA
- Comparator Hysteresis Prevents Erratic Resets

## description/ordering information

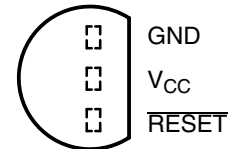
The TL7757 is a supply-voltage supervisor designed for use in microcomputer and microprocessor systems. The supervisor monitors the supply voltage for undervoltage conditions. During power up, when the supply voltage,  $V_{CC}$ , attains a value approaching 1 V, the RESET output becomes active (low) to prevent undefined operation. If the supply voltage drops below threshold voltage level ( $V_{IT-}$ ), the RESET output goes to the active (low) level until the supply undervoltage fault condition is eliminated.

**D PACKAGE  
(TOP VIEW)**

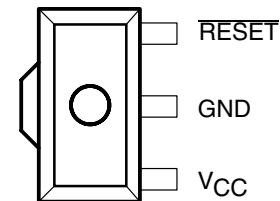


NC—No internal connection

**LP PACKAGE  
(TOP VIEW)**



**PK PACKAGE  
(TOP VIEW)**



GND is in electrical contact with the tab.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC (D)	Tube of 75	TL7757CD	7757C
		Reel of 2500	TL7757CDR	
	SOT (PK)	Reel of 1000	TL7757CPK	T7
	TO226 / TO-92 (LP)	Bulk of 1000	TL7757CLP	TL7757C
Reel of 2000		TL7757CLPR		
-40°C to 85°C	SOIC (D)	Tube of 75	TL7757ID	7757I
		Reel of 2500	TL7757IDR	
	SOT (PK)	Reel of 1000	TL7757IPK	7I
	TO226 / TO-92 (LP)	Bulk of 1000	TL7757ILP	TL7757I
Reel of 2000		TL7757ILPR		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

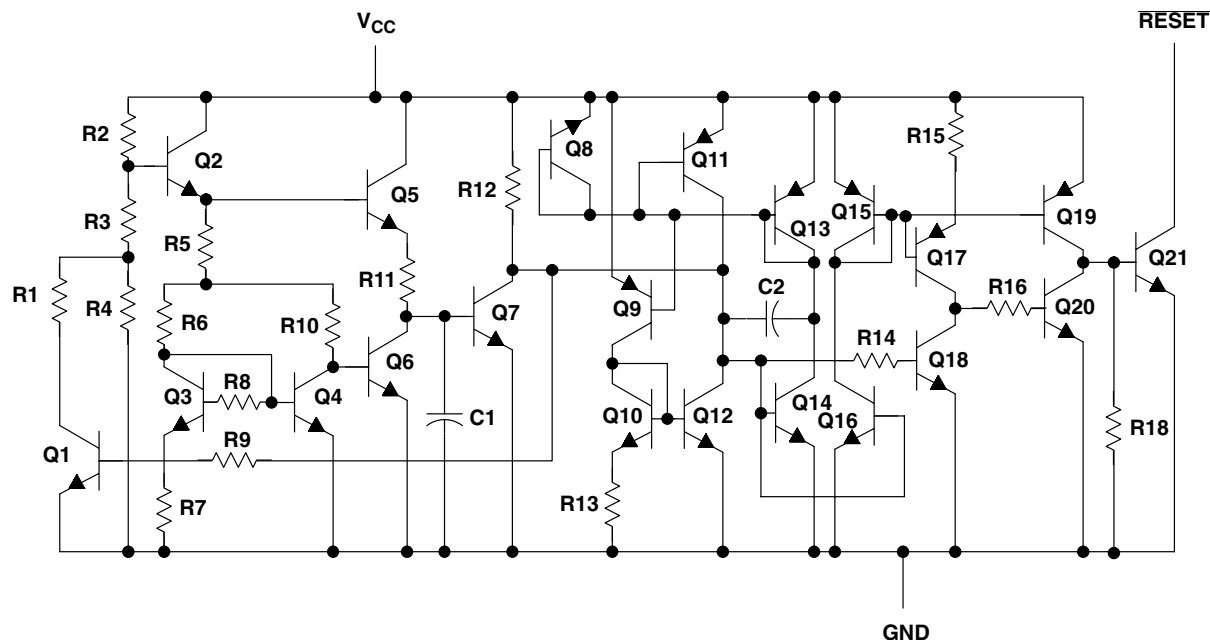
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# TL7757 SUPPLY-VOLTAGE SUPERVISOR AND PRECISION VOLTAGE DETECTOR

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## equivalent schematic



ACTUAL DEVICE COMPONENT COUNT	
Transistors	27
Resistors	20
Capacitors	2

## absolute maximum ratings over operating junction temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1)	-0.3 V to 20 V
Off-state output voltage range (see Note 1)	-0.3 V to 20 V
Output current, $I_O$	30 mA
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3):	
D package	97°C/W
LP package	140°C/W
PK package	52°C/W
Operating virtual junction temperature, $T_J$	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to network terminal ground.
  2. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A) / \theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  3. The package thermal impedance is calculated in accordance with JESD 51-7.

**TL7757**  
**SUPPLY-VOLTAGE SUPERVISOR**  
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**recommended operating conditions**

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	1	7	V	
$V_{OH}$	High-level output voltage		15	V	
$I_{OL}$	Low-level output current		20	mA	
$T_A$	Operating free-air temperature	TL7757C	0	70	°C
		TL7757I	-40	85	

**electrical characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	$T_A$	TL7757C			UNIT
			MIN	TYP	MAX	
$V_{IT-}$	Negative-going input threshold voltage at $V_{CC}$	25°C	4.43	4.55	4.67	V
		0°C to 70°C	4.4		4.7	
$V_{hys}^\dagger$	Hysteresis at $V_{CC}$	25°C	40	50	60	mV
		0°C to 70°C	30		70	
$V_{OL}$	Low-level output voltage $I_{OL} = 20$ mA, $V_{CC} = 4.3$ V	25°C		0.4	0.8	V
		0°C to 70°C			0.8	
$I_{OH}$	High-level output current $V_{CC} = 7$ V, $V_{OH} = 15$ V, See Figure 1	25°C			1	μA
		0°C to 70°C			1	
$V_{res}^\ddagger$	Power-up reset voltage $R_L = 2.2$ kΩ, $V_{CC}$ slew rate $\leq 5$ V/μs	25°C		0.8	1	V
		0°C to 70°C			1.2	
$I_{CC}$	Supply current $V_{CC} = 4.3$ V	25°C		1400	2000	μA
		0°C to 70°C			2000	
		$V_{CC} = 5.5$ V	0°C to 70°C			

<sup>†</sup> This is the difference between positive-going input threshold voltage,  $V_{IT+}$ , and negative-going input threshold voltage,  $V_{IT-}$ .

<sup>‡</sup> This is the lowest voltage at which RESET becomes active.

**switching characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	$T_A$	TL7757C			UNIT
			MIN	TYP	MAX	
$t_{PLH}$	Propagation delay time, low-to-high-level output $V_{CC}$ slew rate $\leq 5$ V/μs, See Figures 2 and 3	25°C		3.4	5	μs
		0°C to 70°C			5	
$t_{PHL}$	Propagation delay time, high-to-low-level output See Figures 2 and 3	25°C		2	5	μs
		0°C to 70°C			5	
$t_r$	Rise time $V_{CC}$ slew rate $\leq 5$ V/μs, See Figures 2 and 3	25°C		0.4	1	μs
		0°C to 70°C			1	
$t_f$	Fall time See Figures 2 and 3	25°C		0.05	1	μs
		0°C to 70°C			1	
$t_{w(min)}$	Minimum pulse duration at $V_{CC}$ for output response	25°C			5	μs
		0°C to 70°C			5	

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## electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL7757I			UNIT
			MIN	TYP	MAX	
V <sub>IT-</sub> Negative-going input threshold voltage at V <sub>CC</sub>		25°C	4.43	4.55	4.67	V
		-40°C to 85°C	4.4		4.7	
V <sub>hys</sub> <sup>†</sup> Hysteresis at V <sub>CC</sub>		25°C	40	50	60	mV
		-40°C to 85°C	30		70	
V <sub>OL</sub> Low-level output voltage	I <sub>OL</sub> = 20 mA, V <sub>CC</sub> = 4.3 V	25°C		0.4	0.8	V
		-40°C to 85°C			0.8	
I <sub>OH</sub> High-level output current	V <sub>CC</sub> = 7 V, V <sub>OH</sub> = 15 V, See Figure 1	25°C			1	μA
		-40°C to 85°C			1	
V <sub>res</sub> <sup>‡</sup> Power-up reset voltage	R <sub>L</sub> = 2.2 kΩ, V <sub>CC</sub> slew rate ≤ 5 V/μs	25°C		0.8	1	V
		-40°C to 85°C			1.2	
I <sub>CC</sub> Supply current	V <sub>CC</sub> = 4.3 V	25°C		1400	2000	μA
		-40°C to 85°C			2100	
		-40°C to 85°C			40	

<sup>†</sup> This is the difference between positive-going input threshold voltage, V<sub>IT+</sub>, and negative-going input threshold voltage, V<sub>IT-</sub>.

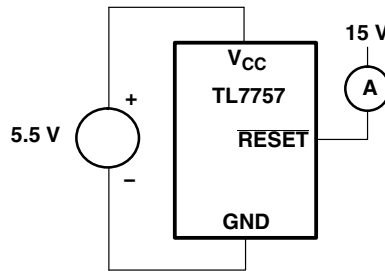
<sup>‡</sup> This is the lowest voltage at which RESET becomes active.

## switching characteristics at specified free-air temperature

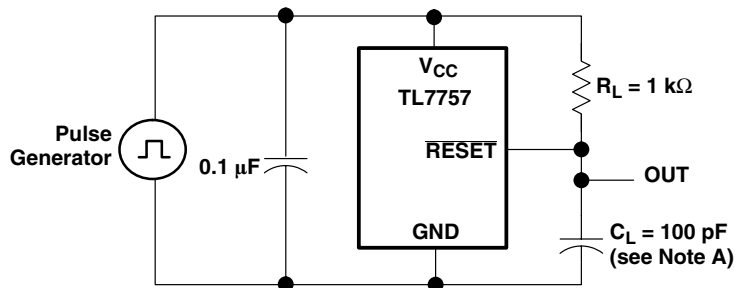
PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL7757I			UNIT
			MIN	TYP	MAX	
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	V <sub>CC</sub> slew rate ≤ 5 V/μs, See Figures 2 and 3	25°C		3.4	5	μs
		-40°C to 85°C			5	
t <sub>PHL</sub> Propagation delay time, high-to-low-level output	See Figures 2 and 3	25°C		2	5	μs
		-40°C to 85°C			5	
t <sub>r</sub> Rise time	V <sub>CC</sub> slew rate ≤ 5 V/μs, See Figures 2 and 3	25°C		0.4	1	μs
		-40°C to 85°C			1	
t <sub>f</sub> Fall time	See Figures 2 and 3	25°C		0.05	1	μs
		-40°C to 85°C			1	
t <sub>w(min)</sub> Minimum pulse duration at V <sub>CC</sub> for output response		25°C			5	μs
		-40°C to 85°C			5	



**PARAMETER MEASUREMENT INFORMATION**

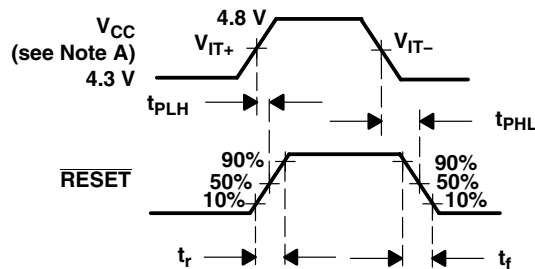


**Figure 1. Test Circuit for Output Leakage Current**



NOTE A: Includes jig and probe capacitance

**Figure 2. Test Circuit for  $\overline{\text{RESET}}$  Output Switching Characteristics**



NOTE A:  $V_{CC}$  slew rate  $\leq 5 \mu\text{s}$

**Figure 3. Switching Diagram**

**TL7757**  
**SUPPLY-VOLTAGE SUPERVISOR**  
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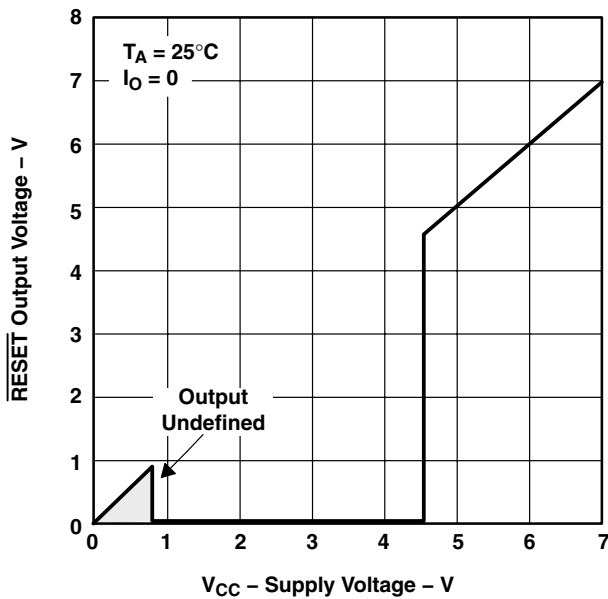
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**TYPICAL CHARACTERISTICS†**

**Table of Graphs**

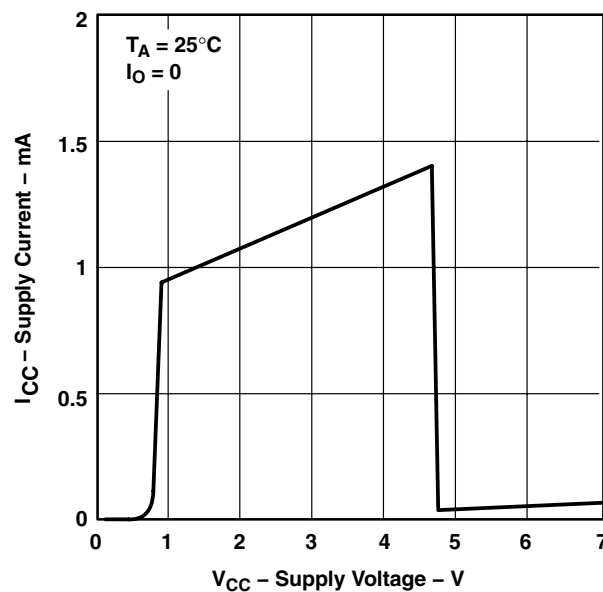
	FIGURE
V <sub>CC</sub> Supply voltage vs $\overline{\text{RESET}}$ output voltage	4
I <sub>CC</sub> Supply current vs Supply voltage	5
I <sub>CC</sub> Supply current vs Free-air temperature	6
V <sub>OL</sub> Low-level output voltage vs Low-level output current	7
V <sub>OL</sub> Low-level output voltage vs Free-air temperature	8
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V <sub>IT-</sub> Input threshold voltage (negative-going V <sub>CC</sub> ) vs Free-air temperature	10
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V <sub>res</sub> Power-up reset voltage and supply voltage vs Time	12
Propagation delay time	13

**SUPPLY VOLTAGE  
vs  
RESET OUTPUT VOLTAGE**



**Figure 4**

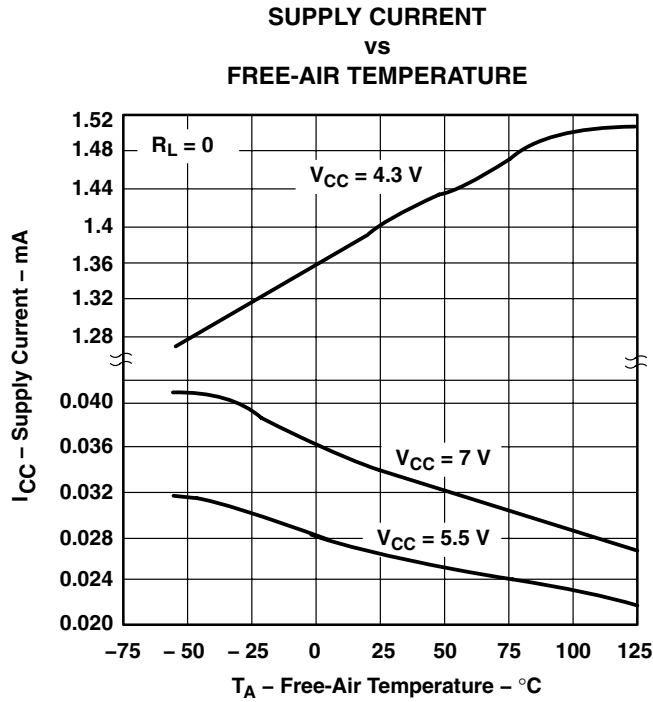
**SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE**



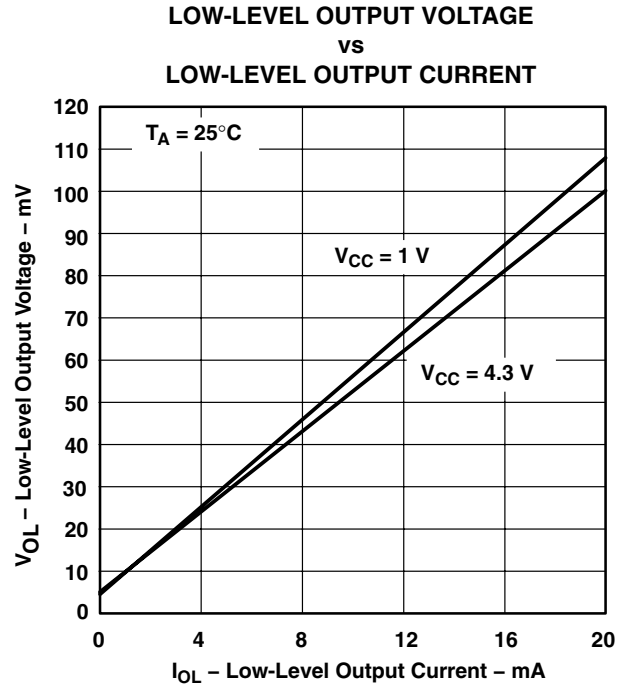
**Figure 5**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

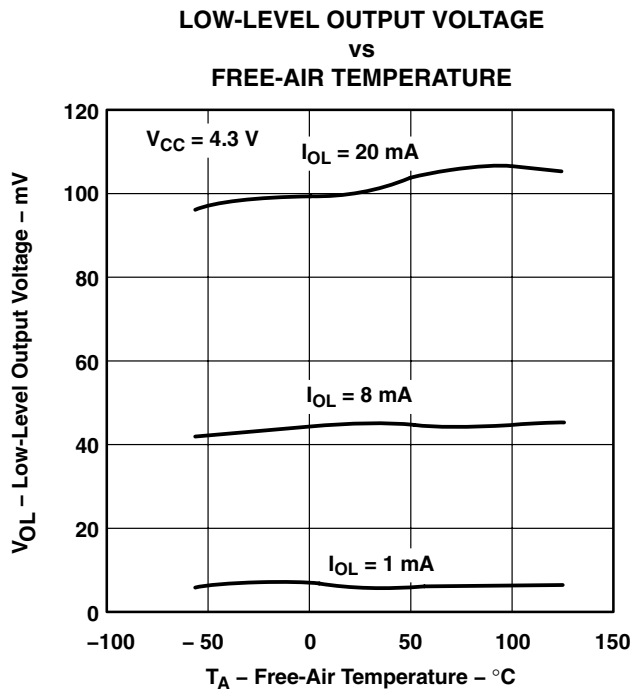
**TYPICAL CHARACTERISTICS†**



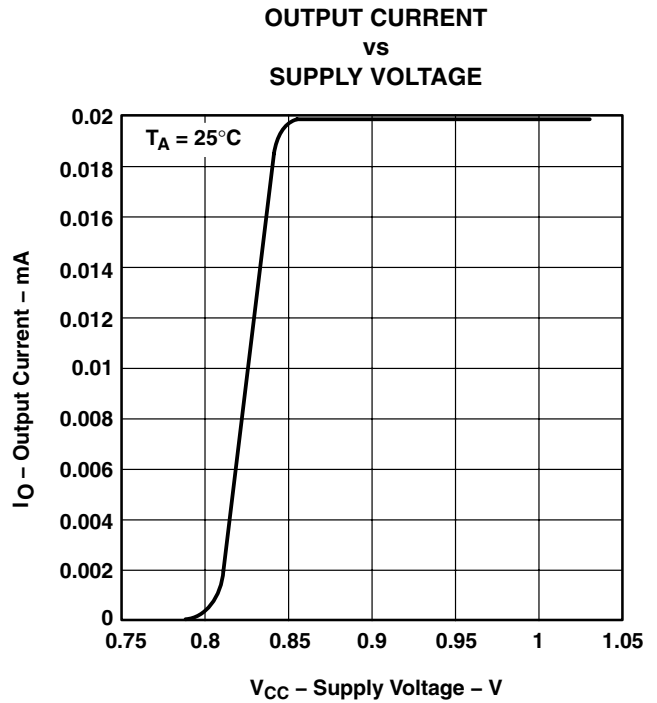
**Figure 6**



**Figure 7**



**Figure 8**



**Figure 9**

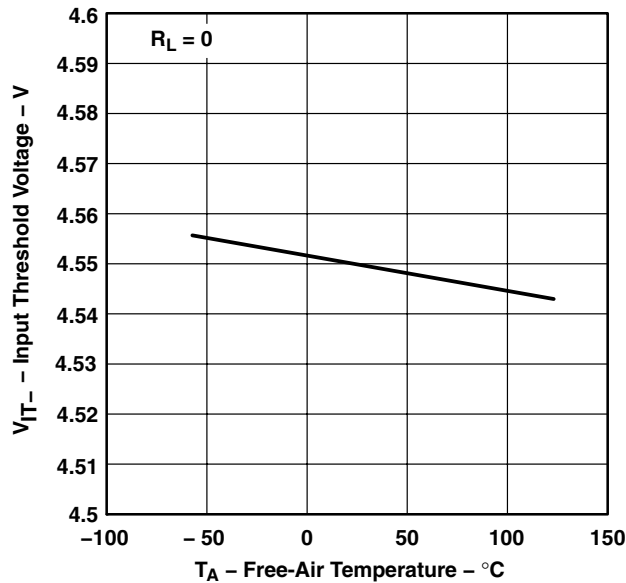
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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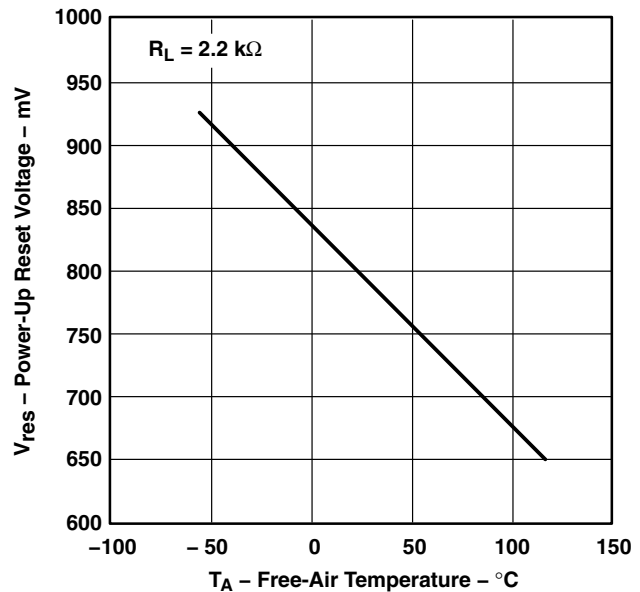
**TYPICAL CHARACTERISTICS†**

**INPUT THRESHOLD VOLTAGE  
 (NEGATIVE-GOING  $V_{CC}$ )  
 vs  
 FREE-AIR TEMPERATURE**



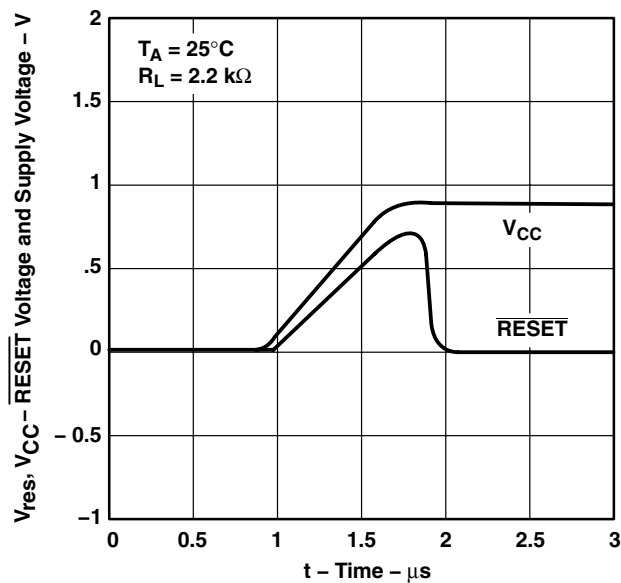
**Figure 10**

**POWER-UP RESET VOLTAGE  
 vs  
 FREE-AIR TEMPERATURE**



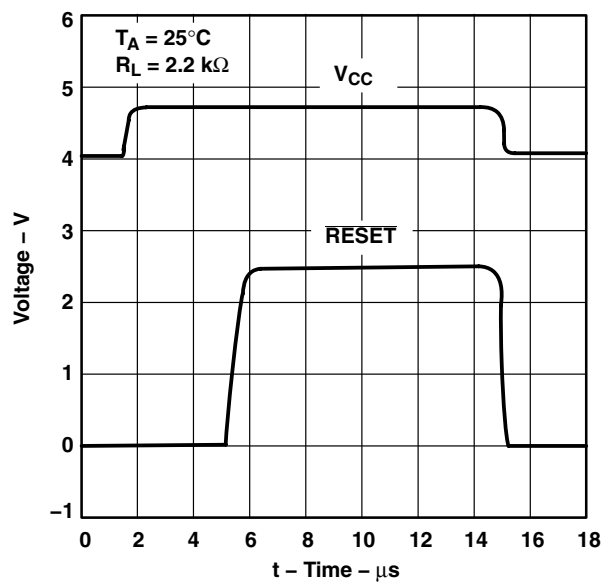
**Figure 11**

**POWER-UP RESET VOLTAGE  
 AND SUPPLY VOLTAGE  
 vs  
 TIME**



**Figure 12**

**PROPAGATION DELAY TIME**



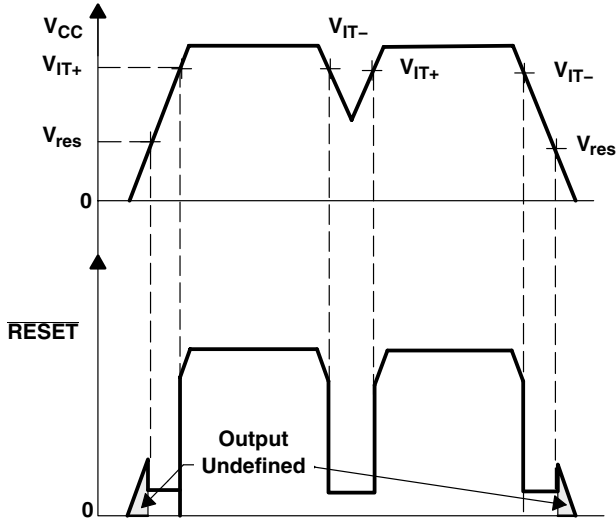
**Figure 13**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

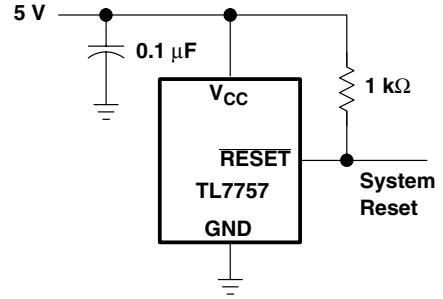


**APPLICATION INFORMATION**

**TYPICAL TIMING DIAGRAM**



**TYPICAL APPLICATION DIAGRAM**



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TL7757CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7757C	<a href="#">Samples</a>
TL7757CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7757C	<a href="#">Samples</a>
TL7757CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7757C	<a href="#">Samples</a>
TL7757CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7757C	<a href="#">Samples</a>
TL7757CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7757C	<a href="#">Samples</a>
TL7757CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7757C	<a href="#">Samples</a>
TL7757CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL7757C	<a href="#">Samples</a>
TL7757CLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL7757C	<a href="#">Samples</a>
TL7757CLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL7757C	<a href="#">Samples</a>
TL7757CLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL7757C	<a href="#">Samples</a>
TL7757CPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	T 7	<a href="#">Samples</a>
TL7757CPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	T 7	<a href="#">Samples</a>
TL7757ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7757I	<a href="#">Samples</a>
TL7757IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7757I	<a href="#">Samples</a>
TL7757IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7757I	<a href="#">Samples</a>
TL7757IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7757I	<a href="#">Samples</a>
TL7757IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7757I	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TL7757IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	77571	<a href="#">Samples</a>
TL7757ILP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	TL77571	<a href="#">Samples</a>
TL7757ILPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	TL77571	<a href="#">Samples</a>
TL7757IPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	71	<a href="#">Samples</a>
TL7757IPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	71	<a href="#">Samples</a>
TL7757MD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-55 to 125		
TL7757MDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-55 to 125		
TL7757MLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

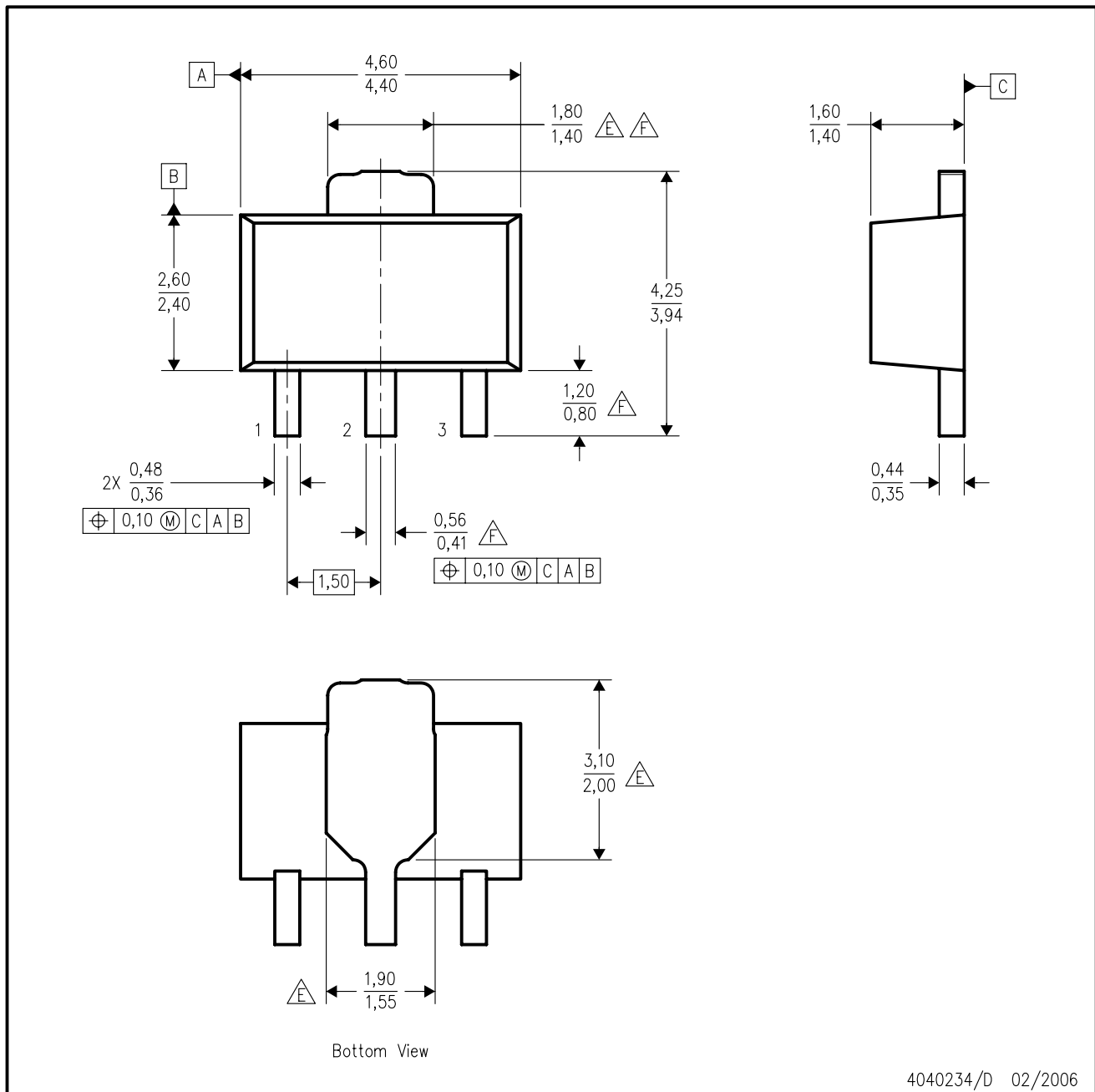
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PK (R-PSS0-F3)

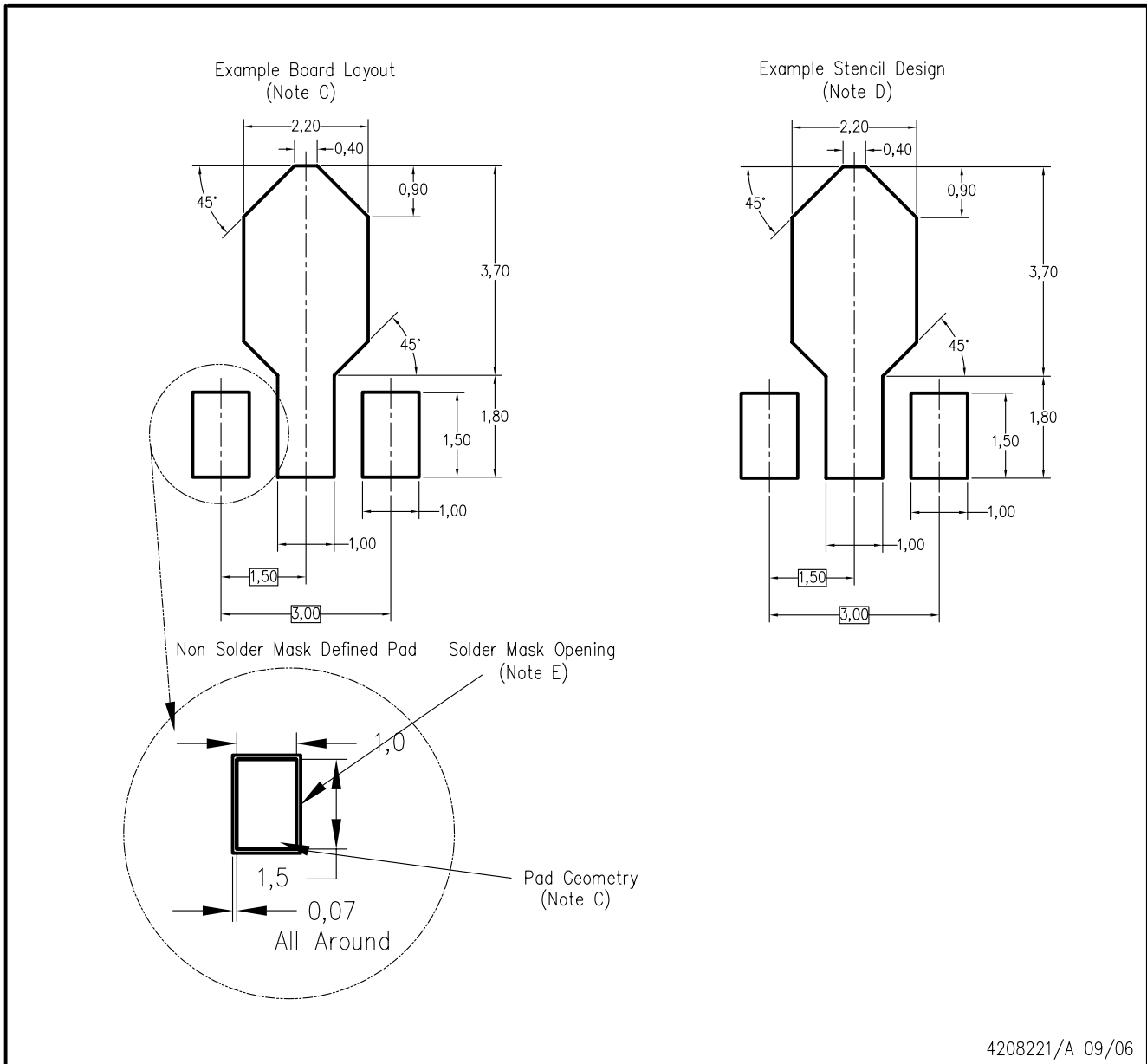
PLASTIC SINGLE-IN-LINE PACKAGE



4040234/D 02/2006

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - The center lead is in electrical contact with the tab.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
- $\triangle E$  Thermal pad contour optional within these dimensions.
- $\triangle F$  Falls within JEDEC TO-243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

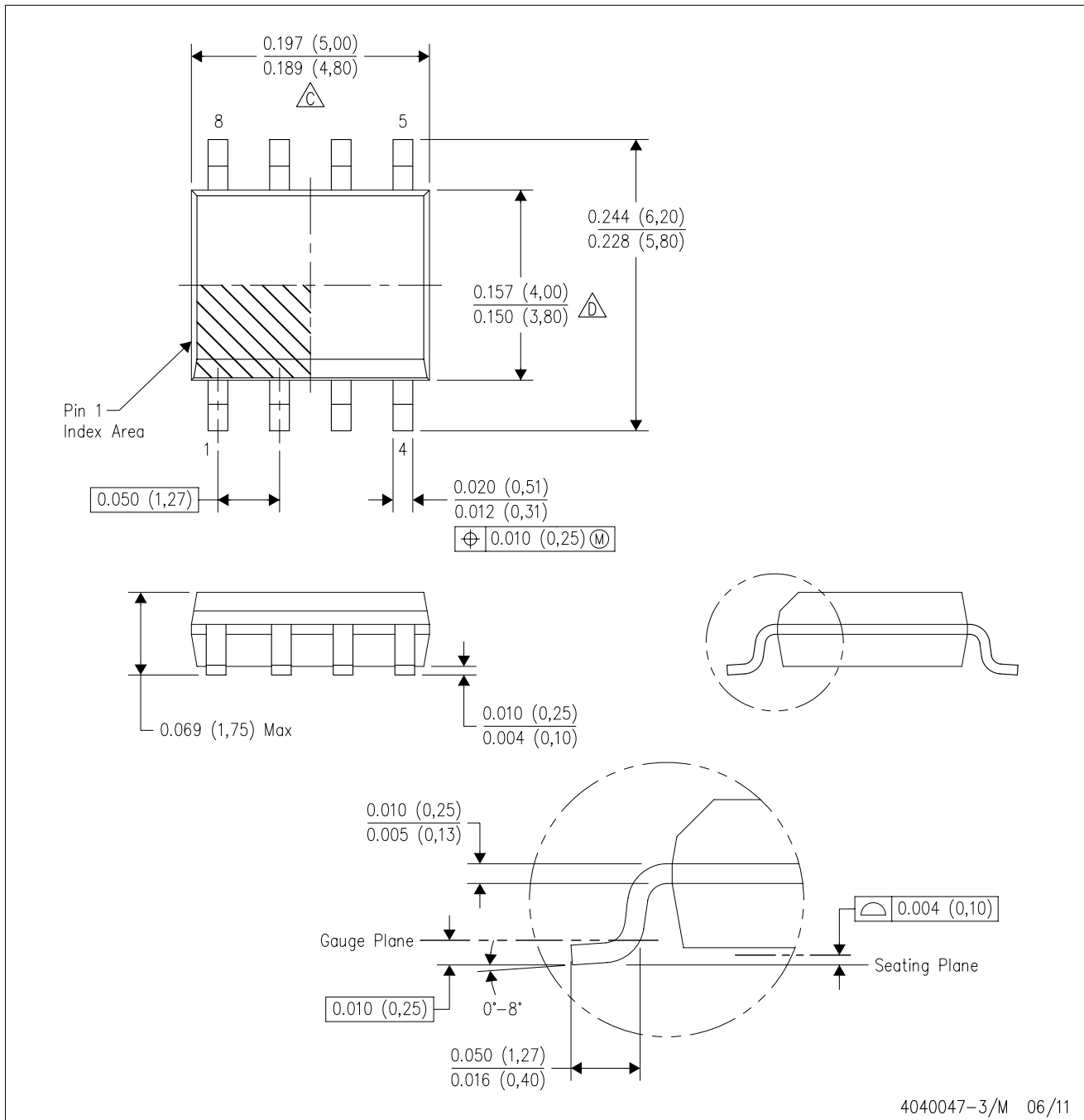
PK (R-PDSO-G3)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

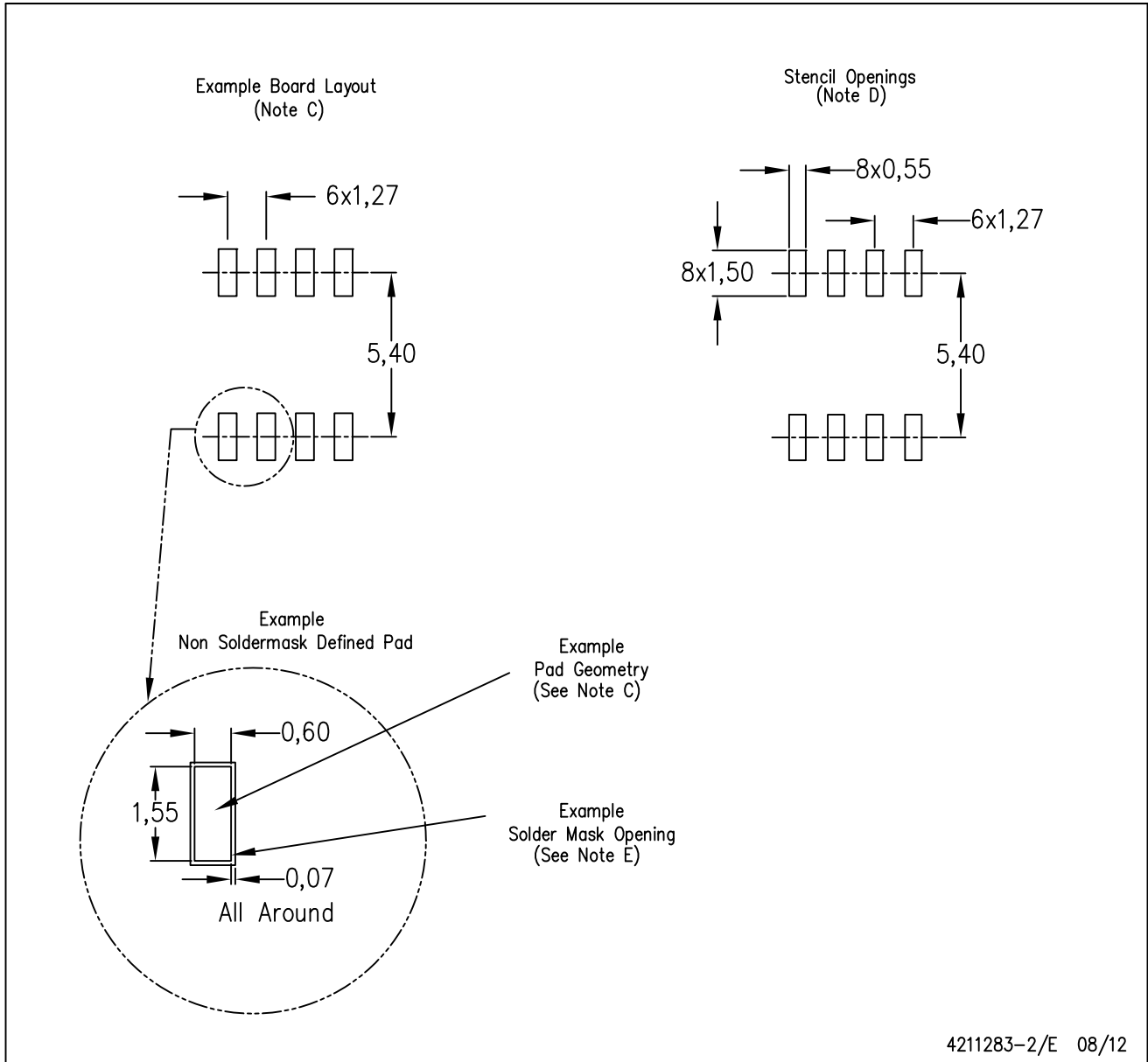
D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



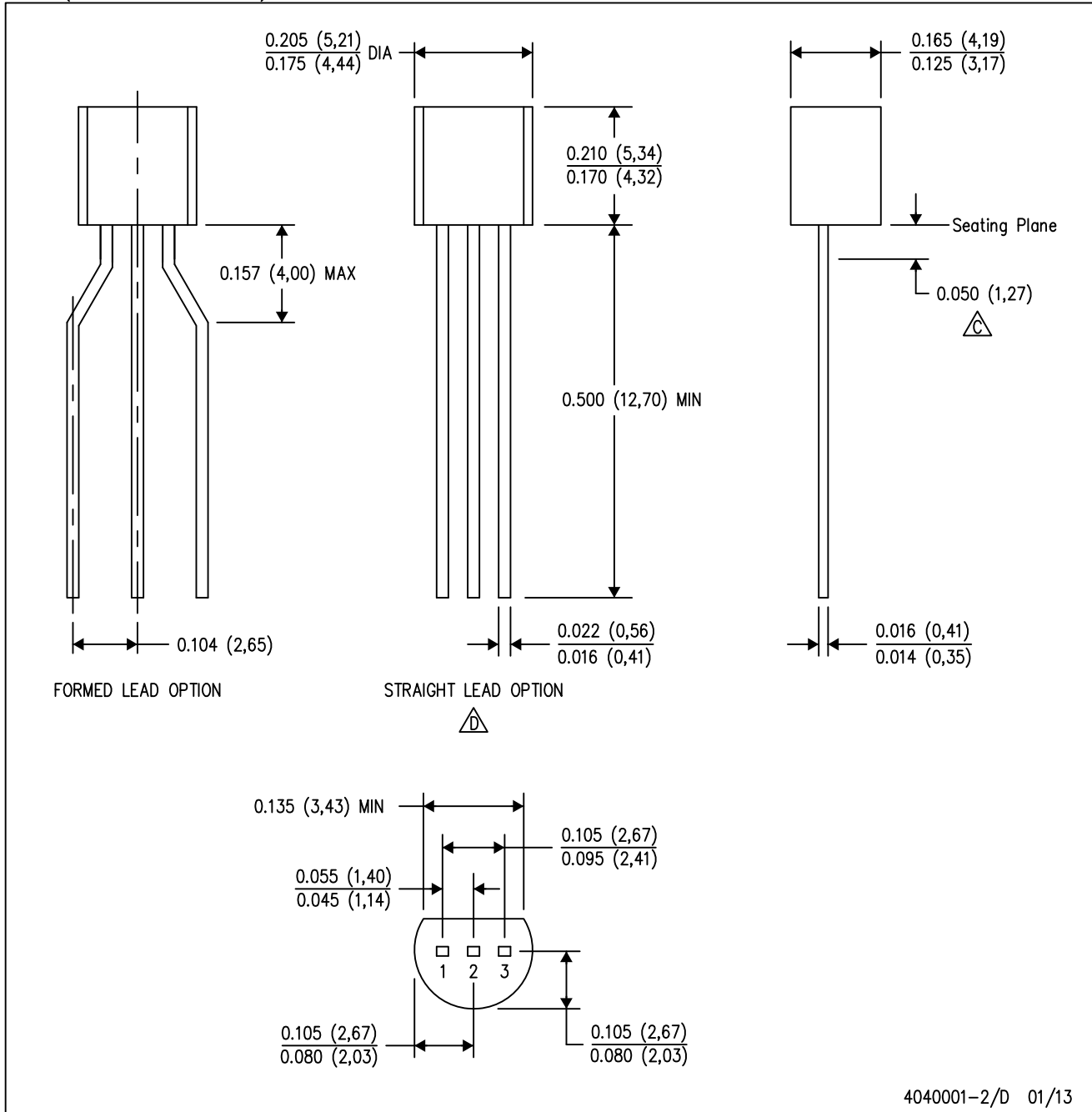
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# MECHANICAL DATA

LP (O-PBCY-W3)

PLASTIC CYLINDRICAL PACKAGE

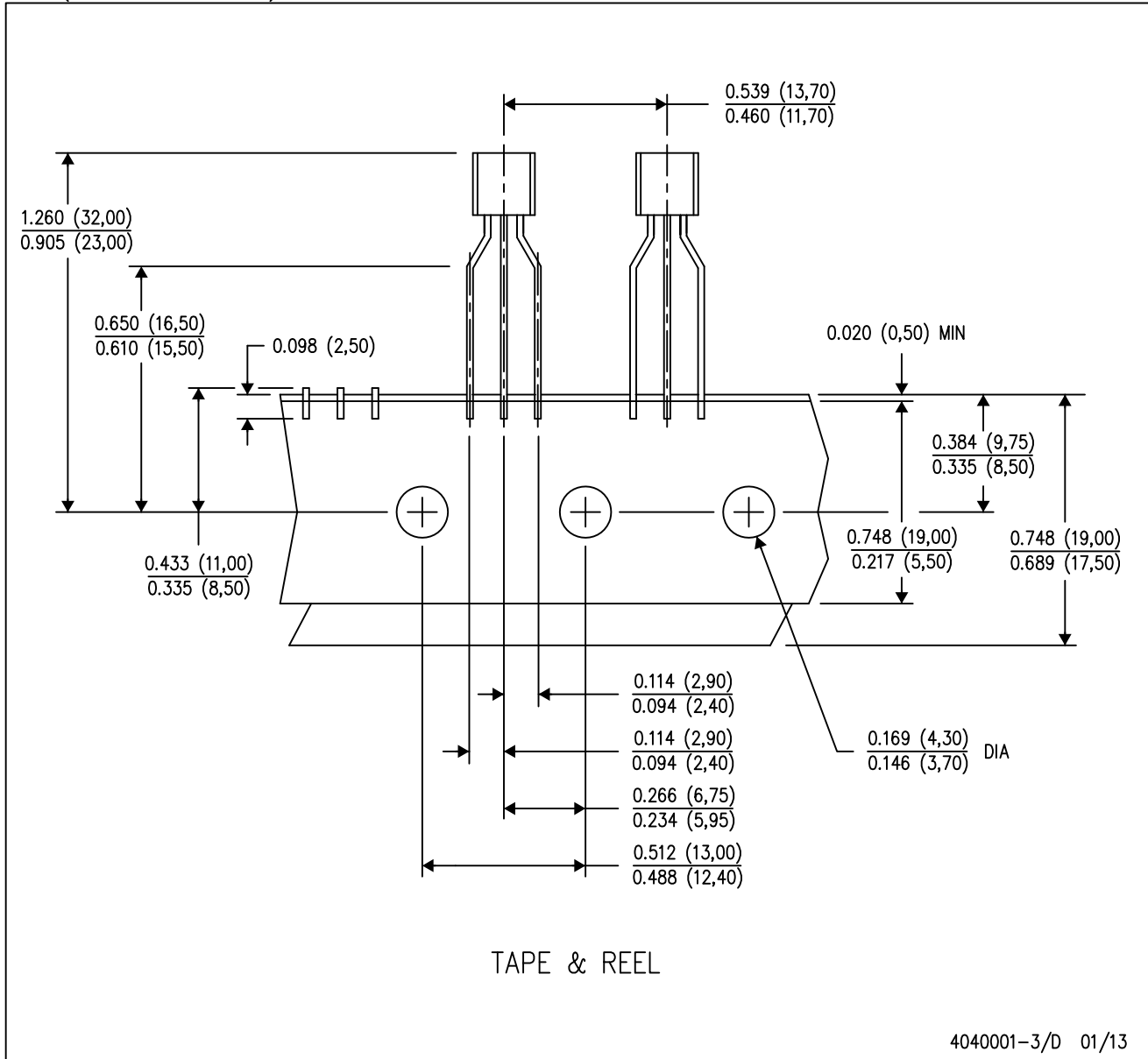


4040001-2/D 01/13

# MECHANICAL DATA

LP (O-PBCY-W3)

PLASTIC CYLINDRICAL PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Tape and Reel information for the Formed Lead Option package.

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