

# DUAL OPERATIONAL AMPLIFIERS WITH INTERNAL REFERENCE

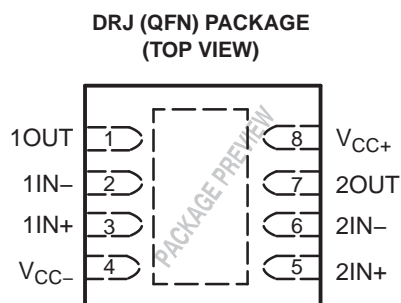
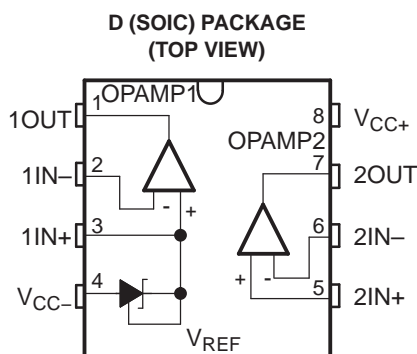
Check for Samples: [TL103W](#), [TL103WA](#)

## FEATURES

- **OPERATIONAL AMPLIFIER**
  - Low Offset Voltage Max of:
    - TL103WA...3 mV (25°C) and 5 mV (Full Temperature)
    - TL103W...4 mV (25°C) and 5 mV (Full Temperature)
  - Low Supply Current...350  $\mu\text{A}/\text{Channel}$  (Typ)
  - Unity Gain Bandwidth...0.9 MHz (Typ)
  - Input Common-Mode Range Includes GND
  - Large Output-Voltage Swing... 0 V to  $V_{CC} - 1.5\text{ V}$
  - Wide Supply-Voltage Range...3 V to 32 V
  - 2-kV ESD Protection (HBM)
- **VOLTAGE REFERENCE**
  - Fixed 2.5-V Reference
  - Tight Tolerance Max of:
    - TL103WA...0.4% (25°C) and 0.8% (Full Temperature)
    - TL103W . . . 0.7% (25°C) and 1.4% (Full Temperature)
  - Low Temperature Drift...7 mV (Typ) Over Operating Temperature Range
  - Wide Sink-Current Range . . . 0.5 mA (Typ) to 100 mA
  - Output Impedance...0.2  $\Omega$  (Typ)

## TYPICAL APPLICATIONS

- Battery Chargers
- Switch-Mode Power Supplies
- Linear Voltage Regulation
- Data-Acquisition Systems



NOTE: Exposed thermal pad is connected internally to  $V_{CC-}$  via die attach.

## DESCRIPTION/ORDERING INFORMATION

The TL103W and TL103WA combine the building blocks of a dual operational amplifier and a fixed voltage reference – both of which often are used in the control circuitry of both switch-mode and linear power supplies. OPAMP1 has its noninverting input internally tied to a fixed 2.5-V reference, while OPAMP2 is independent, with both inputs uncommitted.

For the A grade, especially tight voltage regulation can be achieved through low offset voltages for both operational amplifiers (typically 0.5 mV) and tight tolerances for the voltage reference (0.4% at 25°C and 0.8% over operating temperature range).

The TL103W and TL103WA are characterized for operation from  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ .



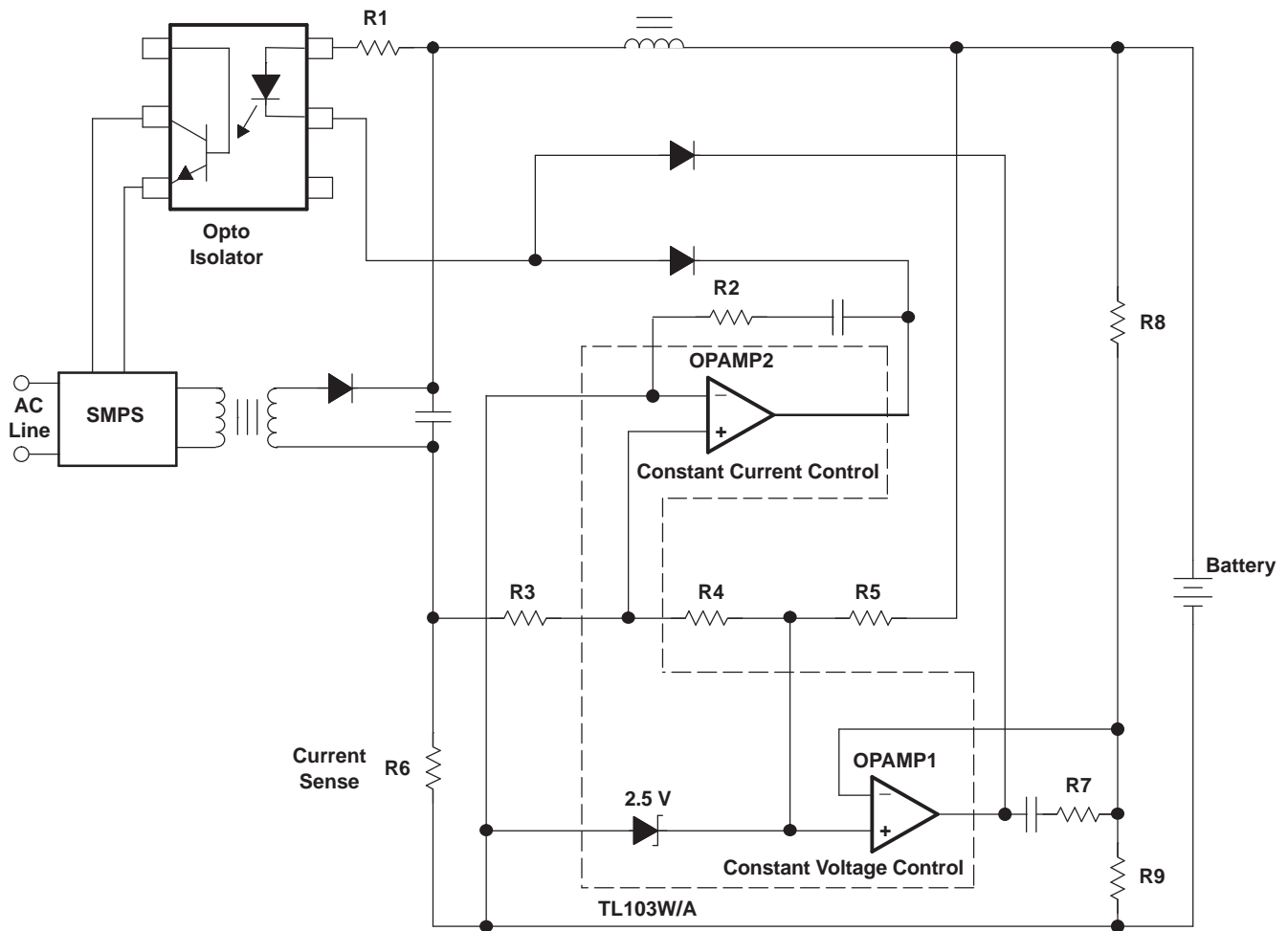
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**ORDERING INFORMATION**

T <sub>A</sub>	MAX V <sub>IO</sub> AND V <sub>REF</sub> TOLERANCE (25°C)	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	A grade 3 mV, 0.4%	QFN (DRJ)	Reel of 1000	TL103WAIDRJR	PREVIEW
		SOIC (D)	Tube of 75	TL103WAID	Z103WA
			Reel of 2500	TL103WAIDR	
	Standard grade 4 mV, 0.7%	QFN (DRJ)	Reel of 1000	TL103WIDRJR	PREVIEW
		SOIC (D)	Tube of 75	TL103WID	Z103W
			Reel of 2500	TL103WIDR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**Typical Application Circuit**



**Figure 1. TL103W/A in a Constant-Current and Constant-Voltage Battery Charger**

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		36	V
V <sub>ID</sub>	Operational amplifier input differential voltage		36	V
V <sub>I</sub>	Operational amplifier input voltage range	–0.3	36	V
I <sub>KA</sub>	Voltage reference cathode current		100	mA
θ <sub>JA</sub>	Package thermal impedance	D package <sup>(2) (3)</sup>	97	°C/W
		DRJ package <sup>(2) (4)</sup>	TBD	
T <sub>J</sub>	Maximum junction temperature		150	°C
T <sub>stg</sub>	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> – T<sub>A</sub>)/θ<sub>JA</sub>. Selecting the maximum of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) The package thermal impedance is calculated in accordance with JESD 51-5.

## Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>IN</sub>	Supply voltage	3	32	V
I <sub>K</sub>	Cathode current	1	100	mA
T <sub>A</sub>	Operating free-air temperature	–40	105	°C

## OPAMP1, Operational Amplifier With Noninverting Input Connected to the Internal $V_{REF}$

### Electrical Characteristics

$V_{CC+} = 5\text{ V}$ ,  $V_{CC} = \text{GND}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	TL103W	$V_{icm} = 0\text{ V}$	25°C	1	4	mV
				Full range	5		
		TL103WA	$V_{icm} = 0\text{ V}$	25°C	0.5	3	
				Full range	5		
$\alpha V_{IO}$	Input offset-voltage drift		25°C	7		$\mu\text{V}/^\circ\text{C}$	
$I_{IB}$	Input bias current (negative input)		25°C	20		nA	
$A_{VD}$	Large-signal voltage gain	$V_{CC+} = 15\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $V_{icm} = 0\text{ V}$	25°C		100		V/mV
$k_{SVR}$	Supply-voltage rejection ratio	$V_{CC+} = 5\text{ V}$ to 30 V, $V_{icm} = 0\text{ V}$	25°C	65	100		dB
$I_{O(\text{source})}$	Output source current	$V_{CC+} = 15\text{ V}$ , $V_O = 2\text{ V}$ , $V_{id} = 1\text{ V}$	25°C	20	40		mA
$I_{SC}$	Short circuit to GND	$V_{CC+} = 15\text{ V}$	25°C		40	60	mA
$I_{O(\text{sink})}$	Output sink current	$V_{CC+} = 15\text{ V}$ , $V_O = 2\text{ V}$ , $V_{id} = -1\text{ V}$	25°C	10	12		mA
		$V_{CC+} = 15\text{ V}$ , $V_O = 0.2\text{ V}$ , $V_{id} = -1\text{ V}$		12	50		$\mu\text{A}$
$V_{OH}$	High-level output voltage	$V_{CC} = 30\text{ V}$ , $R_L = 2\text{ k}\Omega$	25°C	26	27		V
			Full range	26			
		$V_{CC} = 30\text{ V}$ , $R_L = 10\text{ k}\Omega$	25°C	27	28		
			Full range	27			
$V_{OL}$	Low-level output voltage	$R_L = 10\text{ k}\Omega$	25°C		5	20	mV
			Full range		20		
SR	Slew rate at unity gain	$V_{CC+} = 15\text{ V}$ , $C_L = 100\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , $V_I = 0.5\text{ V}$ to 2 V, unity gain	25°C	0.2	0.4		V/ $\mu\text{s}$
GBW	Gain bandwidth product	$V_{CC+} = 30\text{ V}$ , $V_I = 10\text{ mV}$ , $C_L = 100\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , $f = 100\text{ kHz}$	25°C	0.5	0.9		MHz
THD	Total harmonic distortion	$V_{CC+} = 30\text{ V}$ , $V_O = 2\text{ V}_{pp}$ , $C_L = 100\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , $f = 1\text{ kHz}$ , $A_V = 20\text{ dB}$	25°C		0.02		%

**OPAMP2, Independent Operational Amplifier  
Electrical Characteristics**

V<sub>CC+</sub> = 5 V, V<sub>CC</sub> = GND, V<sub>O</sub> = 1.4 V, T<sub>A</sub> = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
V <sub>IO</sub>	Input offset voltage	TL103W	V <sub>icm</sub> = 0 V	25°C	1	4	mV
			Full range		5		
		TL103WA	V <sub>icm</sub> = 0 V	25°C	0.5	3	
			Full range		5		
αV <sub>IO</sub>	Input offset voltage drift		25°C	7		μV/°C	
I <sub>IO</sub>	Input offset current		25°C	2	75	nA	
			Full range		150		
I <sub>IB</sub>	Input bias current		25°C	20	150	nA	
			Full range		200		
A <sub>VD</sub>	Large-signal voltage gain	V <sub>CC+</sub> = 15 V, R <sub>L</sub> = 2 kΩ, V <sub>O</sub> = 1.4 V to 11.4 V	25°C	50	100	V/mV	
			Full range	25			
k <sub>SVR</sub>	Supply-voltage rejection ratio	V <sub>CC+</sub> = 5 V to 30 V	25°C	65	100	dB	
V <sub>ICR</sub>	Input common-mode voltage range	V <sub>CC+</sub> = 30 V <sup>(1)</sup>	25°C	0	V <sub>CC+</sub> – 1.5	V	
			Full range	0	V <sub>CC+</sub> – 2		
CMRR	Common-mode rejection ratio		25°C	70	85	dB	
			Full range	60			
I <sub>O(source)</sub>	Output source current	V <sub>CC+</sub> = 15 V, V <sub>O</sub> = 2 V, V <sub>id</sub> = 1 V	25°C	20	40	mA	
I <sub>SC</sub>	Short circuit to GND	V <sub>CC+</sub> = 15 V	25°C	40	60	mA	
I <sub>O(sink)</sub>	Output sink current	V <sub>CC+</sub> = 15 V, V <sub>O</sub> = 2 V, V <sub>id</sub> = –1 V	25°C	10	12	mA	
		V <sub>CC+</sub> = 15 V, V <sub>O</sub> = 0.2 V, V <sub>id</sub> = –1 V		12	50	μA	
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 30 V, R <sub>L</sub> = 2 kΩ	25°C	26	27	V	
			Full range	26			
		V <sub>CC</sub> = 30 V, R <sub>L</sub> = 10 kΩ	25°C	27	28		
			Full range	27			
V <sub>OL</sub>	Low-level output voltage	R <sub>L</sub> = 10 kΩ	25°C	5	20	mV	
			Full range		20		
SR	Slew rate at unity gain	V <sub>CC+</sub> = 15 V, C <sub>L</sub> = 100 pF, R <sub>L</sub> = 2 kΩ, V <sub>I</sub> = 0.5 V to 3 V, unity gain	25°C	0.2	0.4	V/μs	
GBW	Gain bandwidth product	V <sub>CC+</sub> = 30 V, V <sub>I</sub> = 10 mV, C <sub>L</sub> = 100 pF, R <sub>L</sub> = 2 kΩ, f = 100 kHz	25°C	0.5	0.9	MHz	
THD	Total harmonic distortion	V <sub>CC+</sub> = 30 V, V <sub>O</sub> = 2 V <sub>pp</sub> , C <sub>L</sub> = 100 pF, R <sub>L</sub> = 2 kΩ, f = 1 kHz, A <sub>V</sub> = 20 dB	25°C		0.02	%	
V <sub>n</sub>	Equivalent input noise voltage	V <sub>CC</sub> = 30 V, R <sub>S</sub> = 100 Ω, f = 1 kHz	25°C		50	nV/√Hz	

(1) The input common-mode voltage of either input should not be allowed to go below –0.3 V. The upper end of the common-mode voltage range is V<sub>CC+</sub> – 1.5 V, but either input can go to V<sub>CC+</sub> + 0.3 V (but ≤36 V) without damage.

## Voltage Reference Electrical Characteristics

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
V <sub>REF</sub>	Reference voltage	I <sub>K</sub> = 10 mA	25°C	2.482	2.5	2.518	V
			Full range	2.465		2.535	
	TL103WA	I <sub>K</sub> = 10 mA	25°C	2.49	2.5	2.51	
			Full range	2.48		2.52	
ΔV <sub>REF</sub>	Reference input voltage deviation over temperature range	V <sub>KA</sub> = V <sub>REF</sub> , I <sub>K</sub> = 10 mA	Full range		7	30	mV
I <sub>min</sub>	Minimum cathode current for regulation	V <sub>KA</sub> = V <sub>REF</sub>	25°C		0.5	1	mA
z <sub>ka</sub>	Dynamic impedance <sup>(1)</sup>	V <sub>KA</sub> = V <sub>REF</sub> , ΔI <sub>K</sub> = 1 mA to 100 mA, f < 1 kHz	25°C		0.2	0.5	Ω

(1) The dynamic impedance is defined as  $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$ .

## Total Device Electrical Characteristics

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
I <sub>CC</sub>	Total supply current, excluding cathode-current reference	V <sub>CC+</sub> = 5 V, No load	Full range		0.7	1.2	mA
		V <sub>CC+</sub> = 30 V, No load				2	

## REVISION HISTORY

Changes from Revision J (September 2010) to Revision K	Page
• Changed topside marking to fix typo Z103WQ to Z103WA .....	<a href="#">2</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TL103WAID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	<a href="#">Samples</a>
TL103WAIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	<a href="#">Samples</a>
TL103WAIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	<a href="#">Samples</a>
TL103WAIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	<a href="#">Samples</a>
TL103WAIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	<a href="#">Samples</a>
TL103WAIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	<a href="#">Samples</a>
TL103WID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	<a href="#">Samples</a>
TL103WIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	<a href="#">Samples</a>
TL103WIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	<a href="#">Samples</a>
TL103WIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	<a href="#">Samples</a>
TL103WIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	<a href="#">Samples</a>
TL103WIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.



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**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL103WAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL103WIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

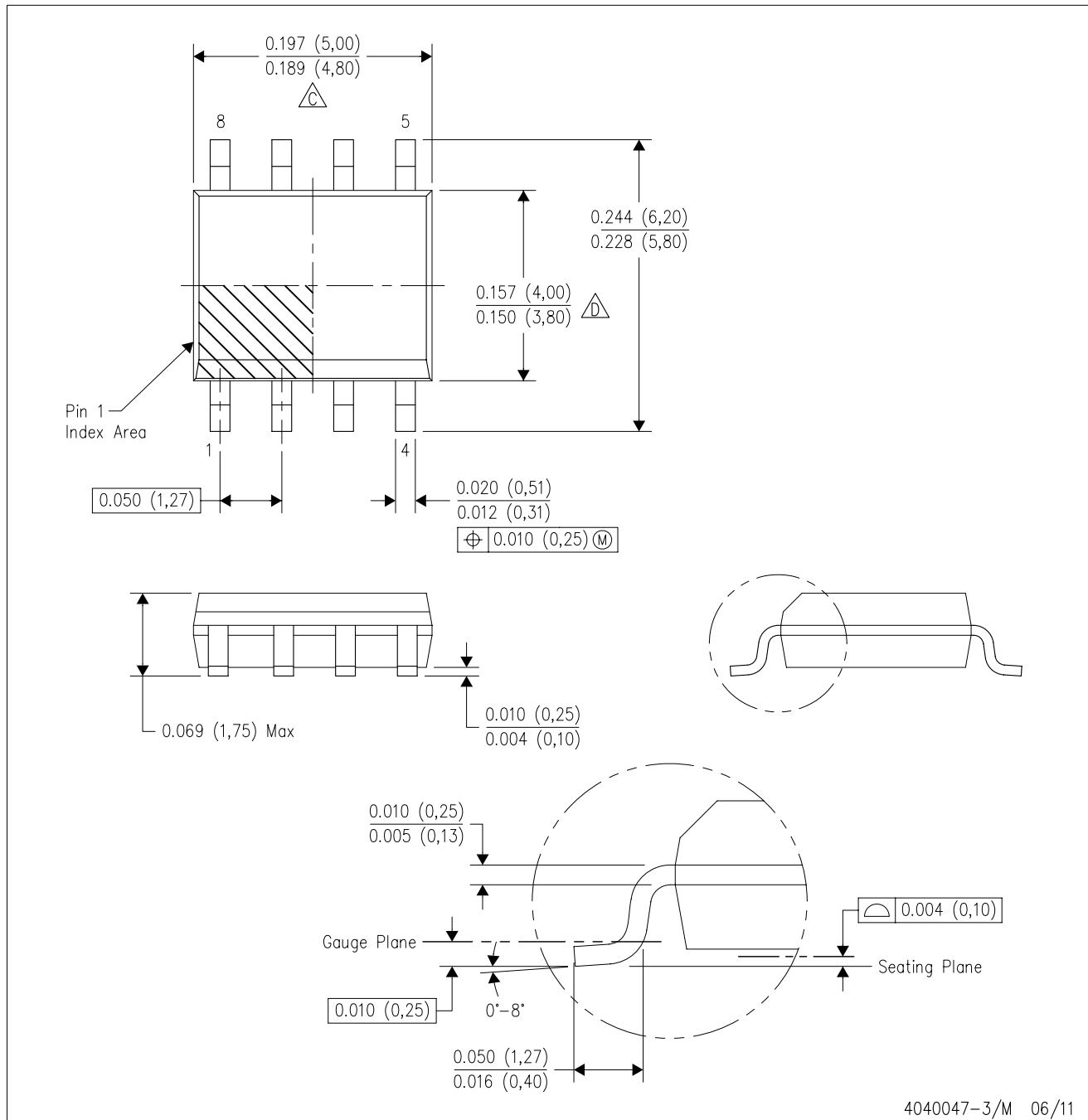
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL103WAIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL103WIDR	SOIC	D	8	2500	340.5	338.1	20.6

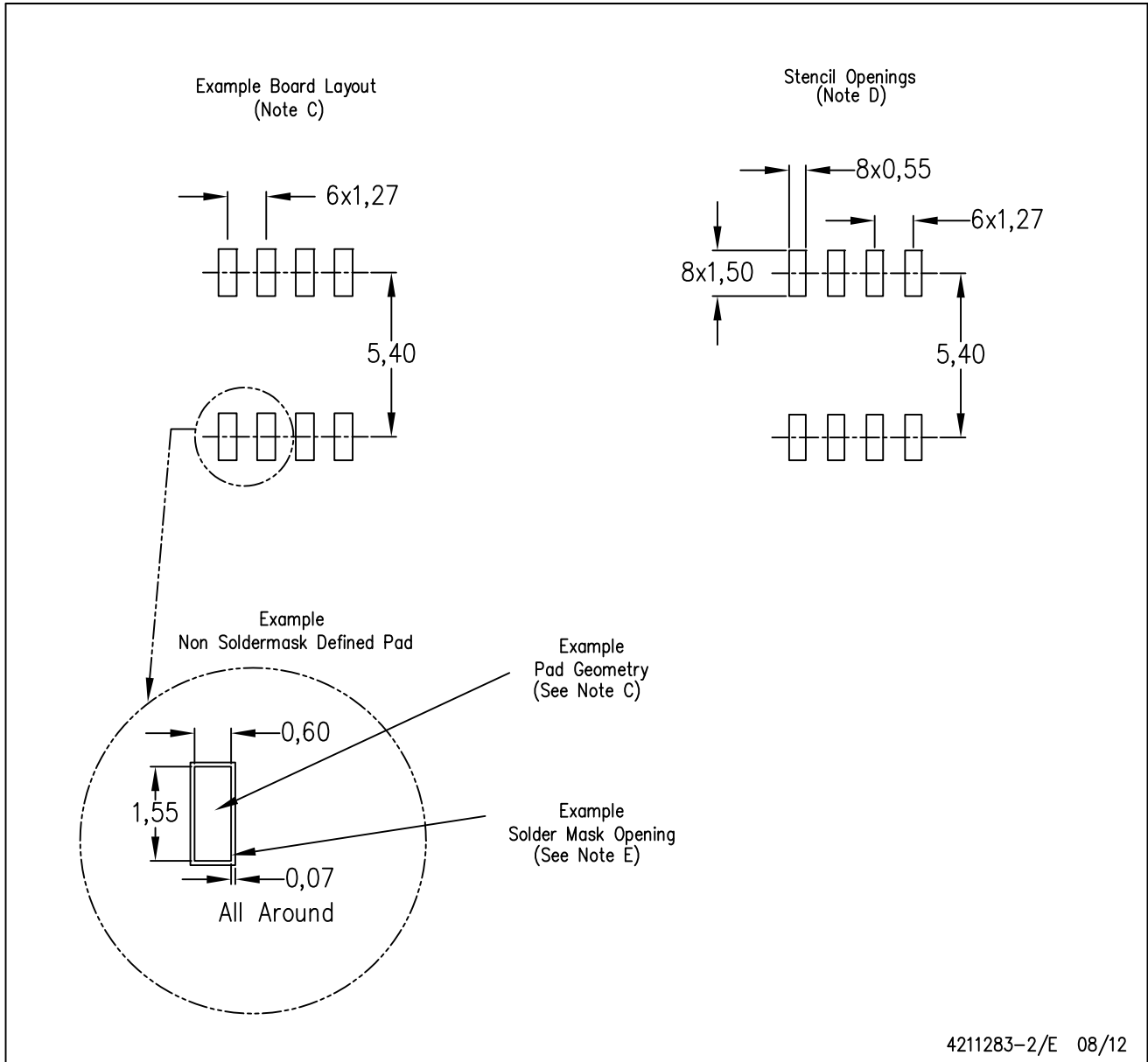
D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

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