50 MHz to 400 MHz CASCADEABLE AMPLIFIER

FEATURES

- **High Dynamic Range**
  - **OIP_3 = 36 dBm**
  - **NF < 4.5 dB**
- **Single-Supply Voltage**
- **High Speed**
  - **V_S = 3 V to 5 V**
  - **I_S = Adjustable**
- **Input/Output Impedance**
  - **50 Ω**

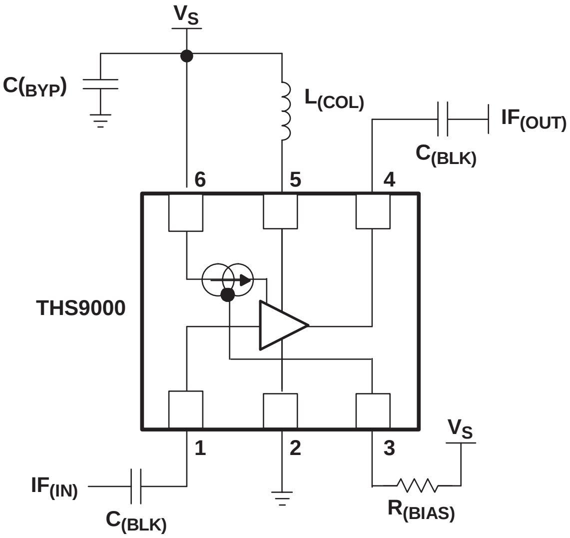
APPLICATIONS

- **IF Amplifiers**
  - **TDMA: GSM, IS-136, EDGE/UWE-136**
  - **CDMA: IS-95, UMTS, CDMA2000**
  - **Wireless Local Loops**
  - **Wireless LAN: IEEE802.11**

DESCRIPTION

The THS9000 is a medium power, cascadeable, gain block optimized for high IF frequencies. The amplifier incorporates internal impedance matching to 50 Ω. The part mounted on the standard EVM achieves greater than 15-dB input and output return loss from 50 MHz to 325 MHz with V_S = 5 V, $R_{(BIAS)}$ = 237 Ω, $L_{(COL)}$ = 470 nH. Design requires only two dc-blocking capacitors, one power-supply bypass capacitor, one RF choke, and one bias resistor.

FUNCTIONAL BLOCK DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

PACKAGED DEVICE[1]	PACKAGE TYPE	TRANSPORT MEDIA, QUANTITY
THS9000DRWT	2 × 2 QFN[2]	Tape and Reel, 250
THS9000DRWR		Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) The PowerPAD™ is electrically isolated from all other pins.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature (unless otherwise noted)[1]

		THS9000	UNIT
Supply voltage, GND to V_S		5.5	V
Input voltage		GND to V_S	
Continuous power dissipation		See Dissipation Rating table	
Maximum junction temperature, T_J		+150	°C
Maximum junction temperature, continuous operation, long term reliability, T_J[2]		+125	°C
Storage temperature, T_{stg}		–65 to +150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		+300	°C
ESD Ratings:	HBM	2000	V
	CDM	1500	V
	MM	100	V

(1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} (°C/W)	POWER RATING[1]	
		T_A ≤ +25°C	T_A = +85°C
DRW[2][3]	91	1.1 W	440 mW

(1) Power rating is determined with a junction temperature of +125°C. Thermal management of the final PCB should strive to keep the junction temperature at or below +125°C for best performance.
(2) This data was taken using the JEDEC standard High-K test PCB.
(3) The THS9000 incorporates a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature, which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD thermally-enhanced package.

RECOMMENDED OPERATING CONDITIONS

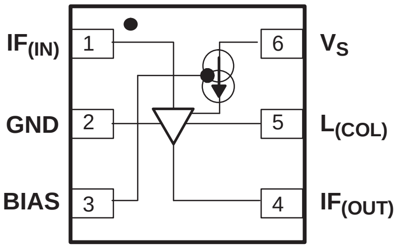
	MIN	NOM	MAX	UNIT
Supply voltage	2.7		5	V
Operating free-air temperature, T_A	–40		+85	°C
Supply current		100		mA

ELECTRICAL CHARACTERISTICS

Typical Performance (V_S = 5 V, $R_{(BIAS)}$ = 237 Ω, $L_{(COL)}$ = 470 nH) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gain	f = 50 MHz		15.9		dB
	f = 350 MHz		15.6		
OIP_3	f = 50 MHz		36		dBm
	f = 350 MHz		35		
1-dB compression	f = 50 MHz		20.8		dBm
	f = 350 MHz		20.6		
Input return loss	f = 50 MHz		15		dB
	f = 350 MHz		19.7		
Output return loss	f = 50 MHz		17.2		dB
	f = 350 MHz		15.1		
Reverse isolation	f = 50 MHz		21		dB
	f = 350 MHz		20		
Noise figure	f = 50 MHz		3.6		dB
	f = 350 MHz		4		

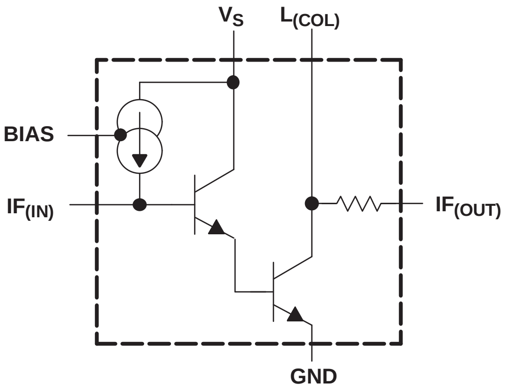
PIN ASSIGNMENT



Terminal Functions

PIN NUMBERS	NAME	DESCRIPTION
1	$IF_{(IN)}$	Signal input
2	GND	Negative power-supply input
3	BIAS	Bias current adjustment input
4	$IF_{(OUT)}$	Signal output
5	$L_{(COL)}$	Output transistor load inductor
6	V_S	Positive power-supply input

SIMPLIFIED SCHEMATIC



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

		FIGURE
	S21 Frequency response	1
	S22 Frequency response	2
	S11 Frequency response	3
	S12 Frequency response	4
	S21 vs $R_{(Bias)}$	5
	Output power vs Input power	6
	OIP_2 vs Frequency	7
	Noise figure vs Frequency	8
	OIP_3 vs Frequency	9
I_S	Supply current vs $R_{(Bias)}$	10
	S21 Frequency response	11
	S22 Frequency response	12
	S11 Frequency response	13
	S12 Frequency response	14
	Noise figure vs Frequency	15
	OIP_2 vs Frequency	16
	Output power vs Input power	17
	OIP_3 vs Frequency	18

S-Parameters of THS9000 as mounted on the EVM with V_S = 5 V, $R_{(BIAS)}$ = 237 Ω, and $L_{(COL)}$ = 68 nH to 470 nH at room temperature.

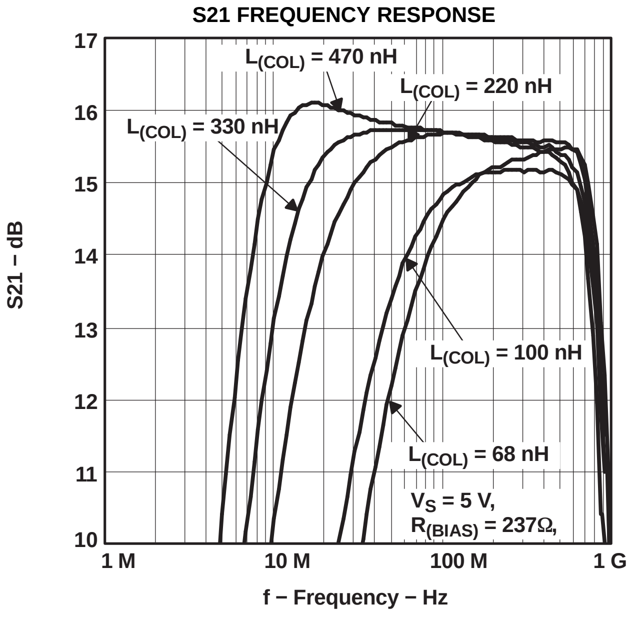


Figure 1.

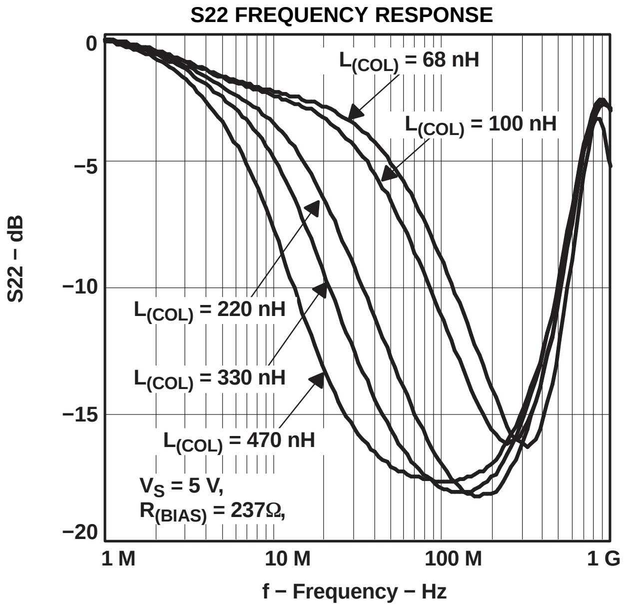


Figure 2.

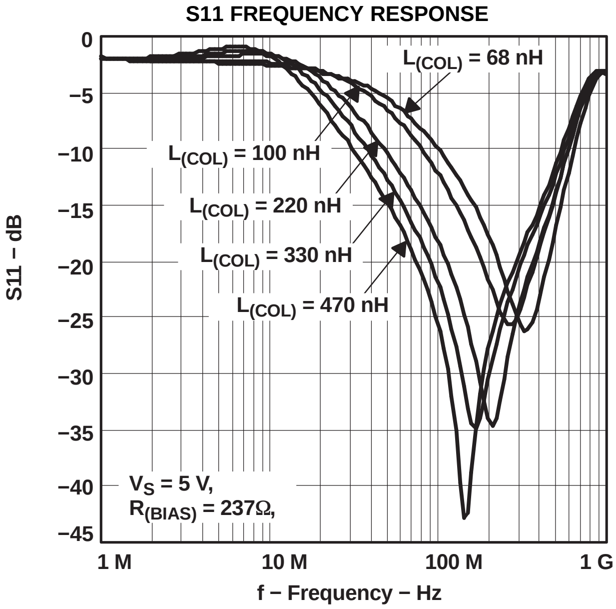

S11 FREQUENCY RESPONSE

Figure 3.

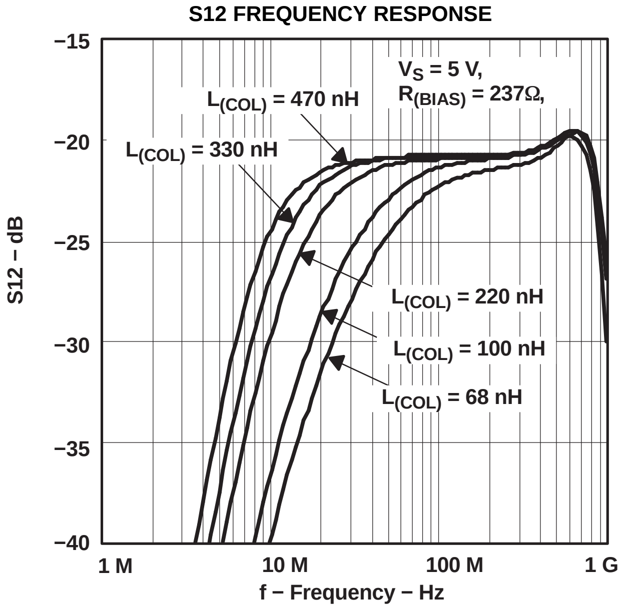

S12 FREQUENCY RESPONSE

Figure 4.

S-Parameters of THS9000 as mounted on the EVM with V_S = 3 V and 5 V, $R_{(BIAS)}$ = various, and $L_{(COL)}$ = 470 nH at room temp.

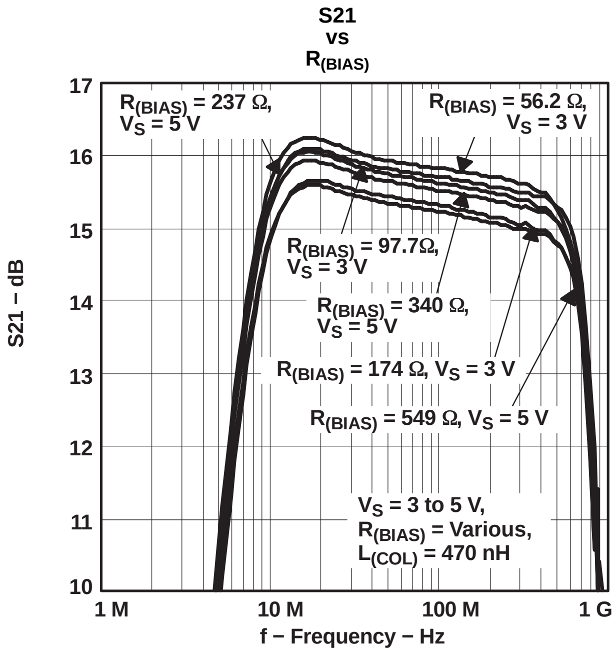

S21
vs
R(BIAS)

Figure 5.

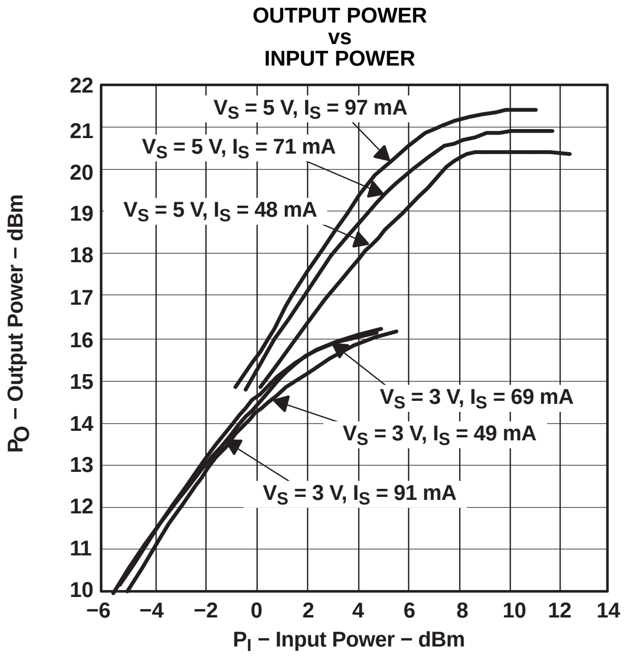

OUTPUT POWER
vs
INPUT POWER

Figure 6.

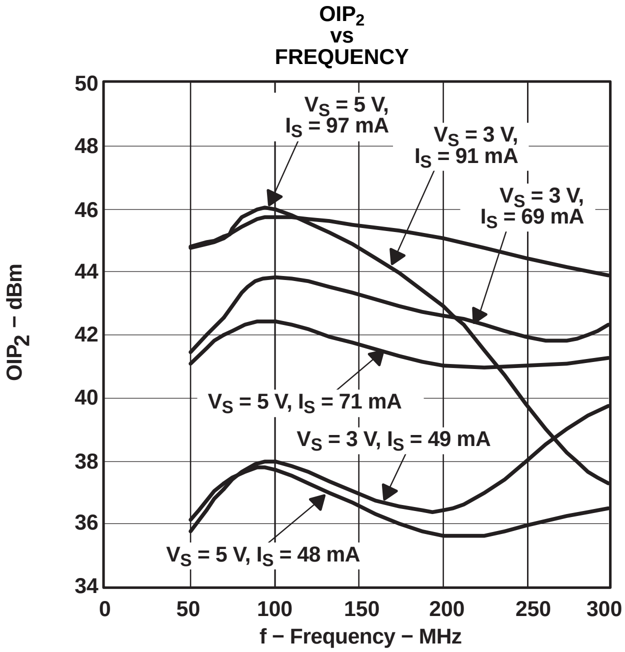

OIP_2 vs FREQUENCY

Figure 7.

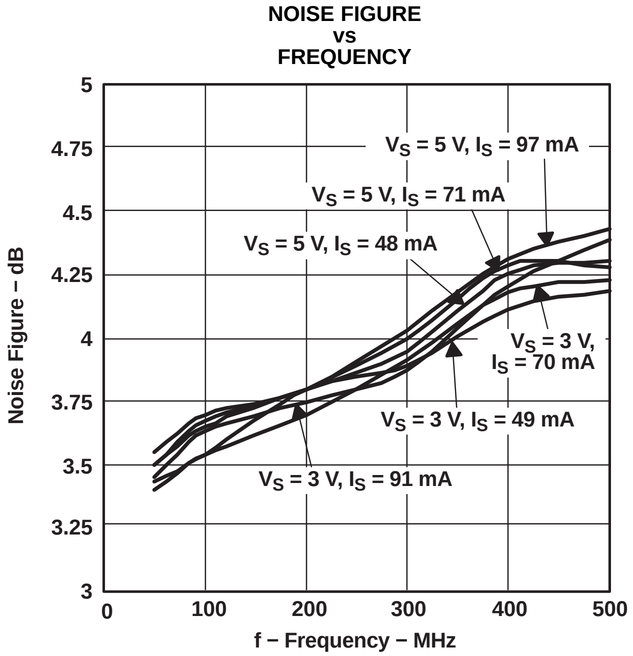

NOISE FIGURE vs FREQUENCY

Figure 8.

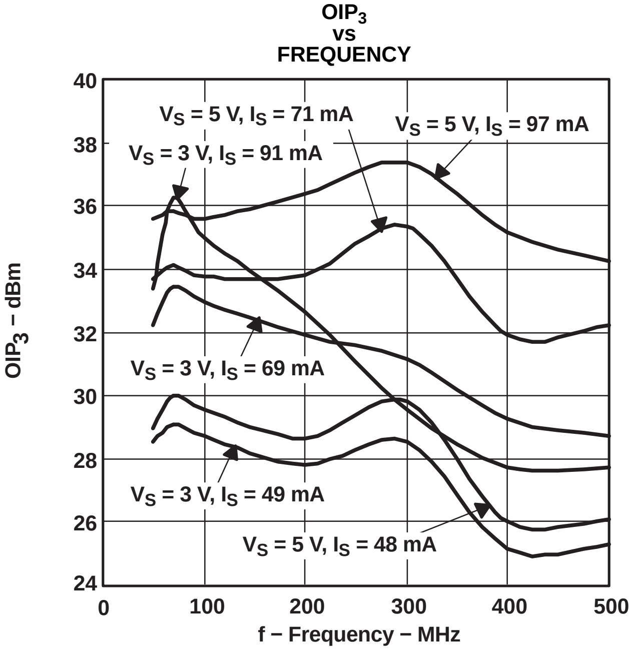

OIP_3 vs FREQUENCY

Figure 9.

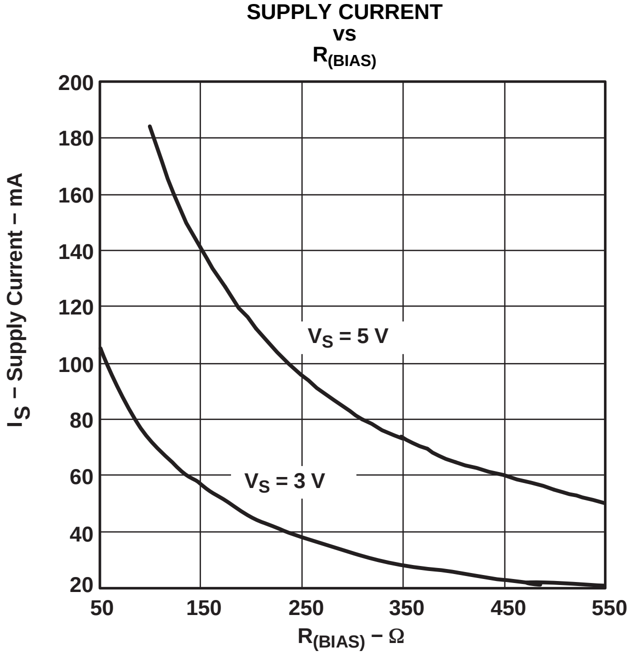

SUPPLY CURRENT vs $R_{(BIAS)}$

Figure 10.

THS9000 as mounted on the EVM with V_S = 5 V, $R_{(BIAS)}$ = 237 Ω, and $L_{(COL)}$ = 470 nH at +40°C, +25°C, and +85°C.

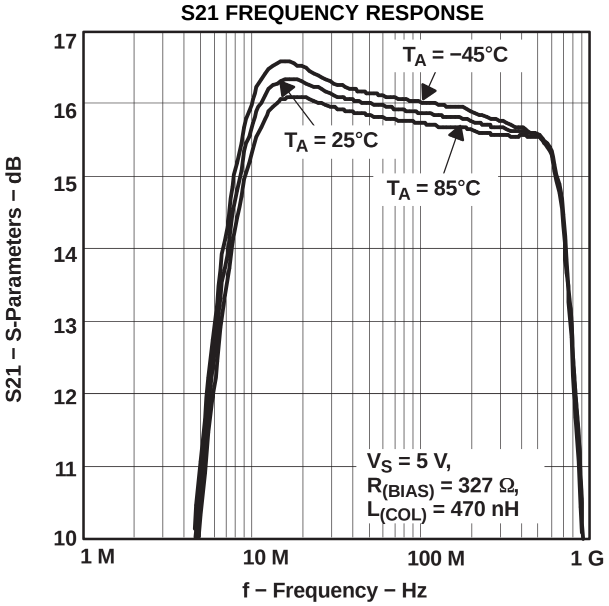


Figure 11.

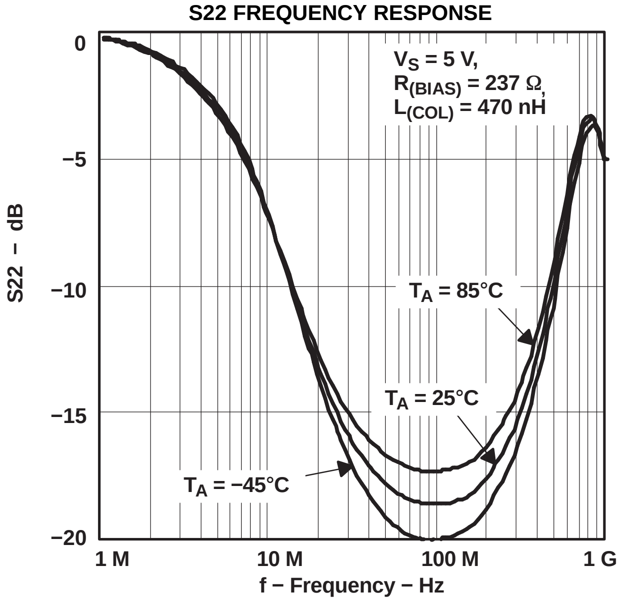


Figure 12.

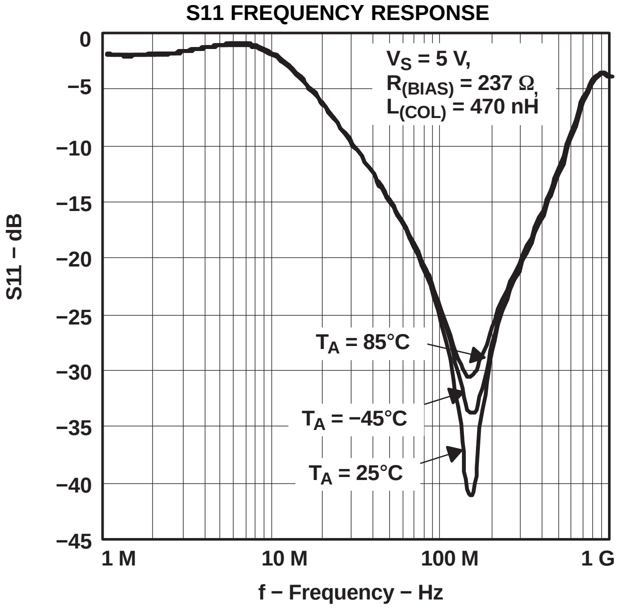


Figure 13.

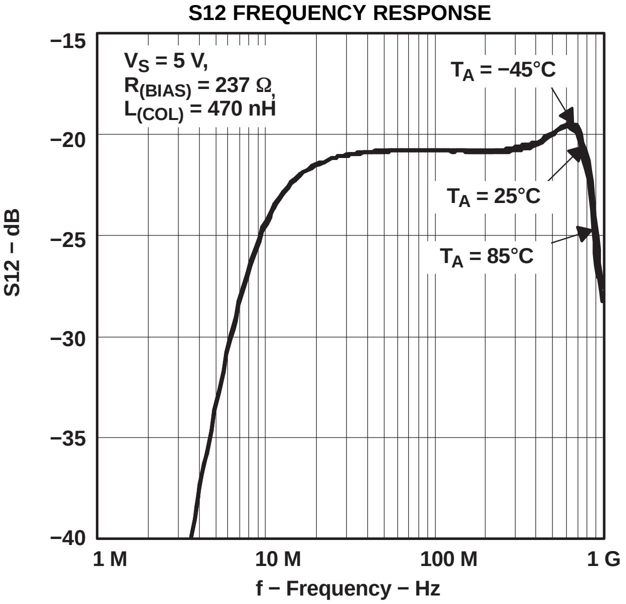


Figure 14.

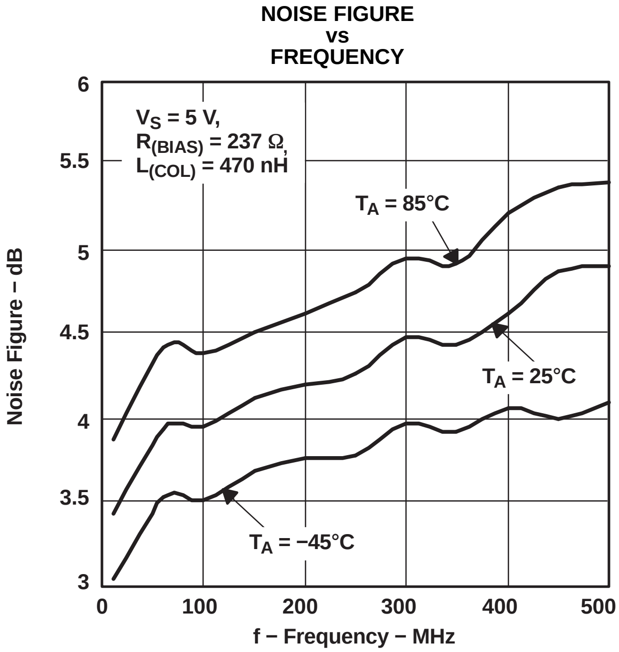


Figure 15.

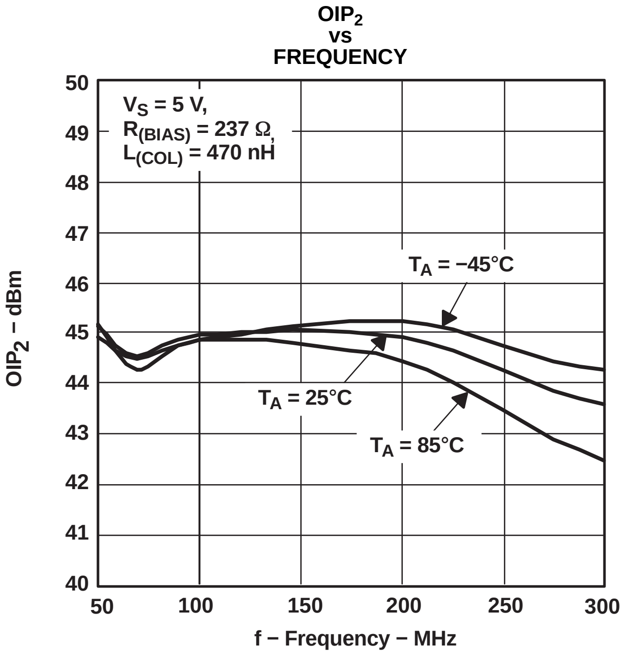


Figure 16.

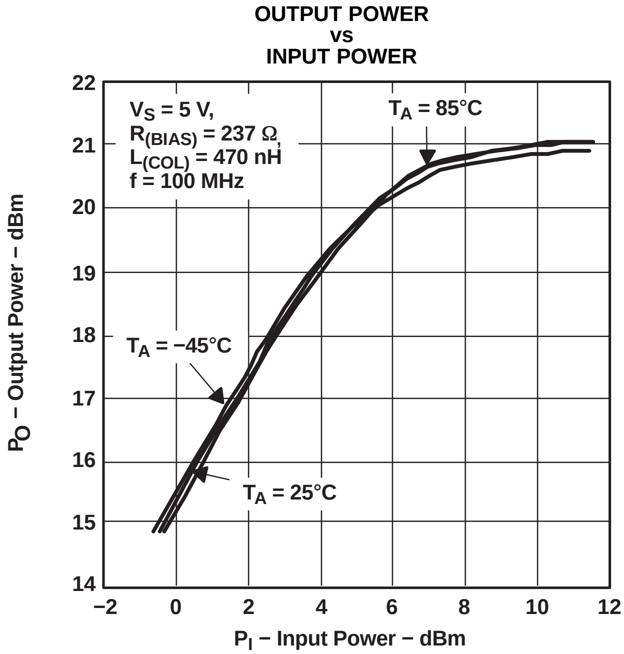


Figure 17.

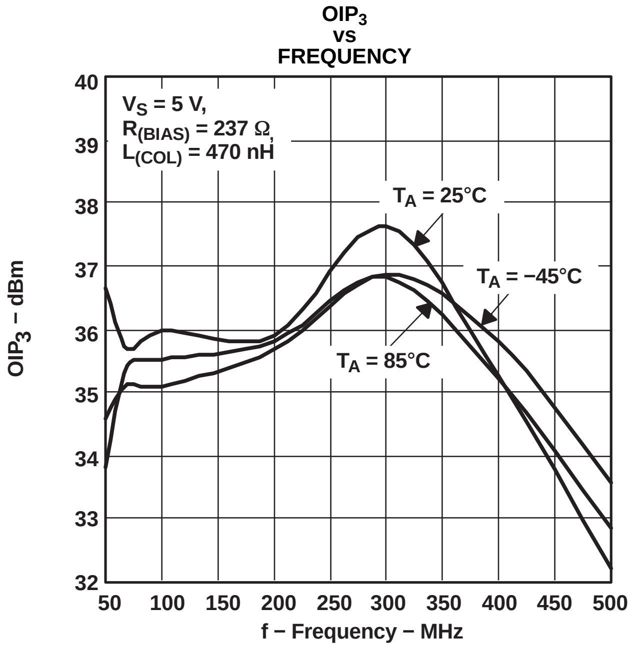


Figure 18.

TYPICAL CHARACTERISTICS

S-Parameters Tables of THS9000 with EVM De-Embedded

V_S = 5 V, $R_{(BIAS)}$ = 237 Ω, $L_{(COL)}$ = 470 nH								
	S21		S11		S22		S12	
FREQUENCY (MHz)	GAIN (dB)	PHASE (°)	GAIN (dB)	PHASE (°)	GAIN (dB)	PHASE (°)	GAIN (dB)	PHASE (°)
1.0	–4.2	–169.5	–2.4	–0.9	–1.9	158.1	–63.1	167.0
5.0	11.3	–124.5	–1.5	–14.5	–2.6	138.0	–32.9	122.4
10.2	15.8	–147.8	–2.2	–42.3	–5.0	101.0	–24.0	80.4
19.7	16.4	–169.4	–6.5	–69.7	–10.5	66.6	–21.3	41.6
50.1	16.0	177.2	–15.6	–91.4	–16.7	30.1	–20.7	14.4
69.7	15.9	173.5	–19.8	–97.7	–17.8	17.7	–20.7	9.1
102.4	15.9	168.4	–26.9	–102.6	–18.2	4.3	–20.7	4.4
150.5	15.8	162.0	–39.0	14.1	–18.1	–8.6	–20.7	–0.7
198.1	15.7	155.8	–27.6	50.8	–17.4	–19.6	–20.7	–1.7
246.9	15.7	149.6	–23.7	40.6	–16.4	–26.7	–20.7	–3.5
307.6	15.6	141.9	–19.8	33.1	–14.9	–37.2	–20.6	–5.7
362.8	15.6	134.7	–17.3	24.7	–13.3	–44.3	–20.4	–7.7
405.0	15.6	129.2	–15.5	20.3	–12.1	–51.0	–20.2	–10.0
452.2	15.6	122.3	–13.8	14.7	–10.6	–58.1	–19.9	–12.5
504.7	15.5	114.9	–11.8	6.3	–9.0	–66.5	–19.7	–16.2
563.4	15.4	105.8	–9.7	–2.9	–7.2	–77.5	–19.4	–22.4
595.3	15.3	100.5	–8.6	–9.1	–6.3	–83.6	–19.3	–26.2
664.5	14.9	88.7	–6.3	–24.2	–4.4	–99.7	–19.3	–36.7
702.1	14.6	81.0	–5.3	–33.2	–3.7	–109.2	–19.6	–43.4
741.8	14.1	76.3	–4.4	–42.9	–3.0	–118.8	–19.9	–50.2
828.1	12.7	60.2	–2.9	–65.5	–2.3	–142.8	–21.7	–69.2
874.9	11.2	51.0	–2.5	–77.9	–2.5	–155.0	–23.6	–75.0
924.4	10.1	50.2	–2.4	–90.4	–3.1	–166.0	–25.8	–85.2
976.7	8.8	51.8	–2.5	—100.7	–4.3	–173.7	–28.4	–78.9
1031.9	9.2	58.2	–2.6	–108.7	–4.7	–175.2	–29.7	–68.7
1090.3	8.9	48.0	–2.5	–115.2	–4.4	–164.7	–31.4	–69.1
1151.9	8.8	39.9	–2.3	–123.3	–3.5	–175.4	–33.6	–83.4
1217.1	8.0	27.7	–2.1	–132.0	–3.0	175.3	–38.2	–81.4
1285.9	7.0	30.5	–2.0	–140.7	–2.8	168.7	–42.3	–25.5
1358.6	5.6	20.6	–1.9	–149.4	–2.9	159.1	–42.2	41.6
1435.5	4.3	19.5	–1.8	–159.4	–3.0	151.3	–38.7	63.3
1516.6	3.4	17.7	–1.9	–168.3	–3.2	144.7	–33.6	62.4
1602.4	2.8	16.5	–2.0	–177.2	–3.5	138.2	–30.5	59.6
1693.0	2.2	8.6	–2.1	174.0	–3.8	131.4	–28.1	56.2
1788.8	1.4	–0.7	–2.2	165.4	–4.1	124.6	–26.2	50.4
1889.9	0.5	–4.1	–2.3	157.0	–4.5	118.2	–24.7	42.4
1996.8	–0.6	–4.5	–2.6	150.0	–4.9	111.2	–24.2	39.5

APPLICATION INFORMATION

The THS9000 is a medium power, cascadeable, amplifier optimized for high intermediate frequencies in radios. The amplifier is unconditionally stable and the design requires only two dc-blocking capacitors, one power-supply bypass capacitor, one RF choke, and one bias resistor. Refer to Figure 25 for the circuit diagram.

The THS9000 operates with a power-supply voltage ranging from 2.5 V to 5.5 V.

The value of $R_{(BIAS)}$ sets the bias current to the amplifier. Refer to Figure 10. This allows the designer to trade-off linearity versus power consumption. $R_{(BIAS)}$ can be removed without damage to the device.

Component selection of $C_{(BYP)}$, C_{IN}, and C_{OUT} is not critical. The values shown in Figure 25 were used for all the data shown in this data sheet.

The amplifier incorporates internal impedance matching to 50 Ω that can be adjusted for various frequencies of operation by proper selection of $L_{(COL)}$.

Figure 19 shows the s-parameters of the part mounted on the standard EVM with V_S = 5 V, $R_{(BIAS)}$ = 237 Ω, and $L_{(COL)}$ = 470 nH. With this configuration, the part is very broadband, and achieves greater than 15-dB input and output return loss from 50 MHz to 325 MHz.

Figure 20 shows the S-parameters of the part mounted on the standard EVM with V_S = 5 V, $R_{(BIAS)}$ = 237 Ω, and $L_{(COL)}$ = 68 nH. With this configuration, the part achieves greater than 15-dB input and output return loss from 250 MHz to 400 MHz.

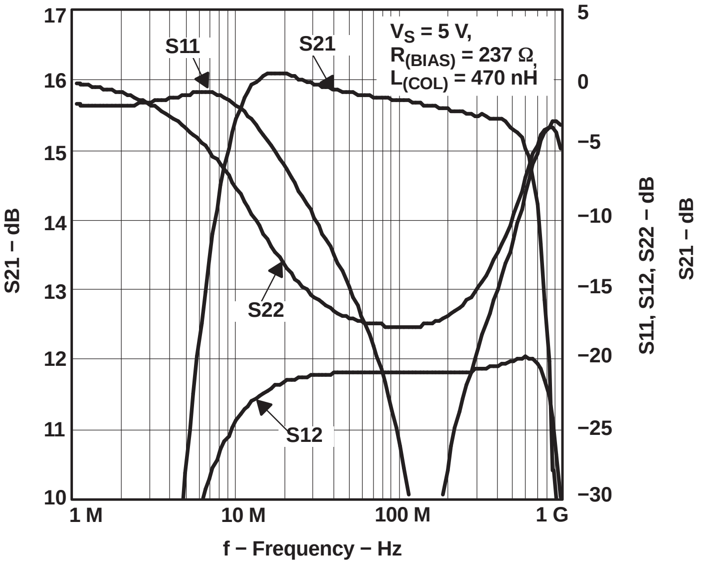


Figure 19. S-Parameters of THS9000 mounted on the standard EVM with V_S = 5 V, $R_{(BIAS)}$ = 237 Ω, and $L_{(COL)}$ = 470 nH

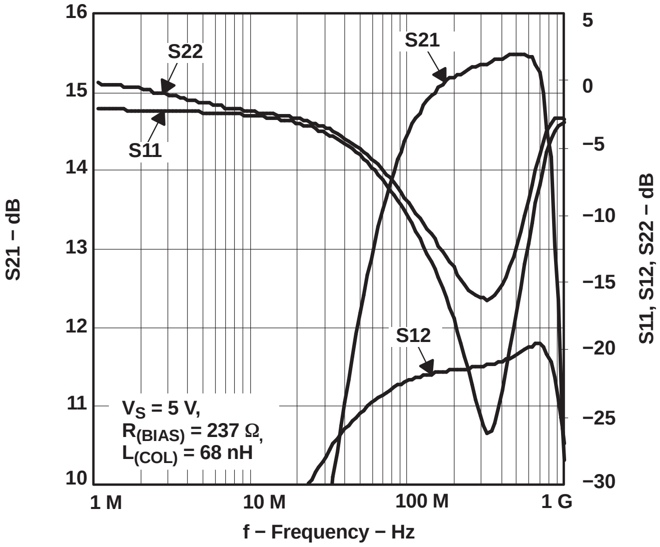


Figure 20. S-Parameters of THS9000 mounted on the standard EVM with V_S = 5 V, $R_{(BIAS)}$ = 237 Ω, and $L_{(COL)}$ = 68 nH

Figure 21 shows an example of a single conversion receiver architecture and where the THS9000 would typically be used.

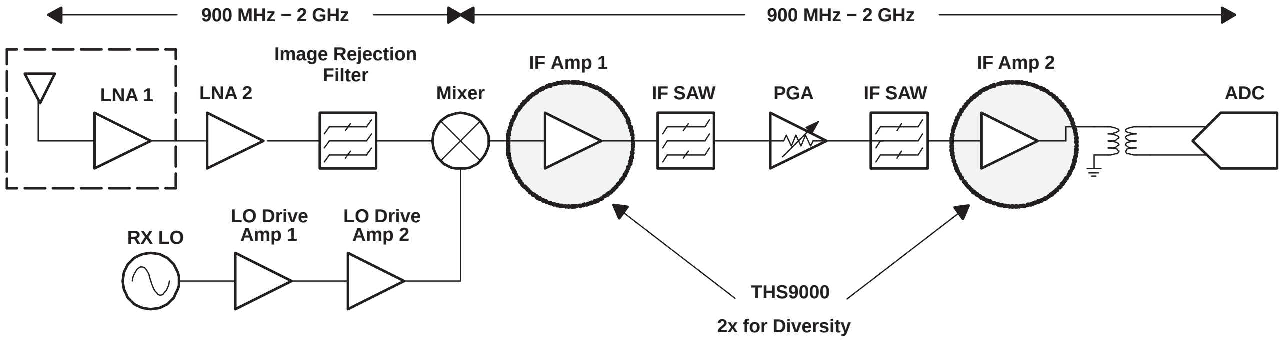


Figure 21. Example Single Conversion Receiver Architecture

Figure 22 shows an example of a dual conversion receiver architecture and where the THS9000 would typically be used.

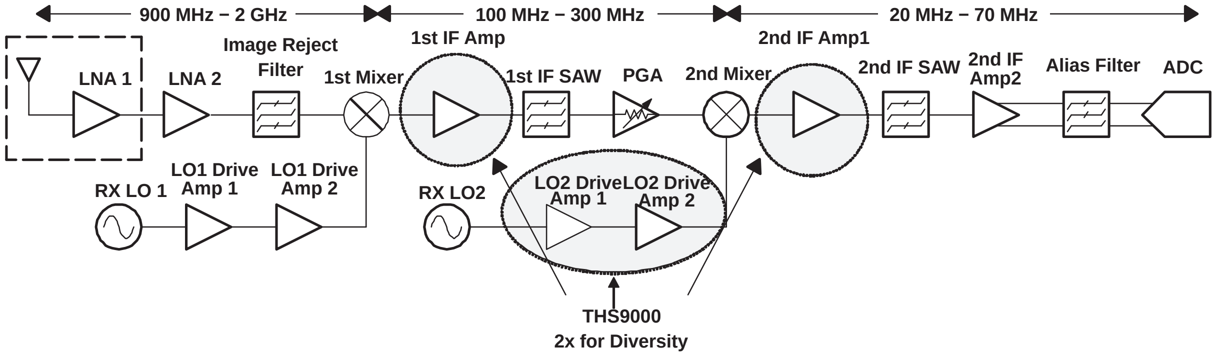


Figure 22. Example Dual Conversion Receiver Architecture

Figure 23 shows an example of a dual conversion transmitter architecture and where the THS9000 would typically be used.

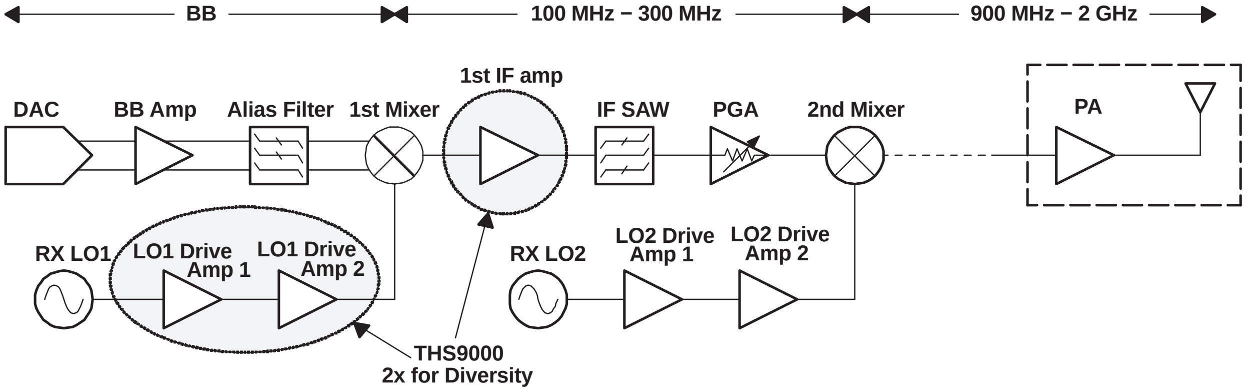
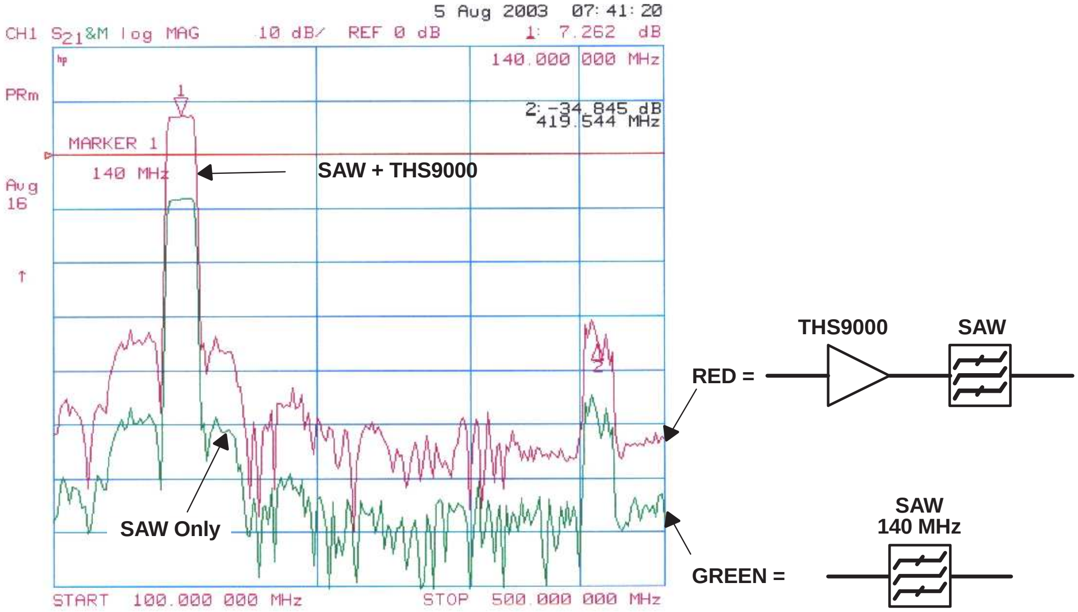


Figure 23. Example Dual Conversion Transmitter Architecture

Figure 24 shows the THS9000 and Sawtek #854916 SAW filter frequency response along with the frequency response of the SAW filter alone. The SAW filter has a center frequency of 140 MHz with 10-MHz bandwidth and 8-dB insertion loss. It can be seen that the frequency response with the THS9000 is the same as with the SAW except for a 15-dB gain. The THS9000 is mounted on the standard EVM with V_S = 5 V, $R_{(BIAS)}$ = 237 Ω, and $L_{(COL)}$ = 470 nH. Note the amplifier does not add artifacts to the signal.



140 MHz SAW: Sawtek #854916

Figure 24. Frequency Response of the THS9000 and SAW Filter, and SAW Filter Only

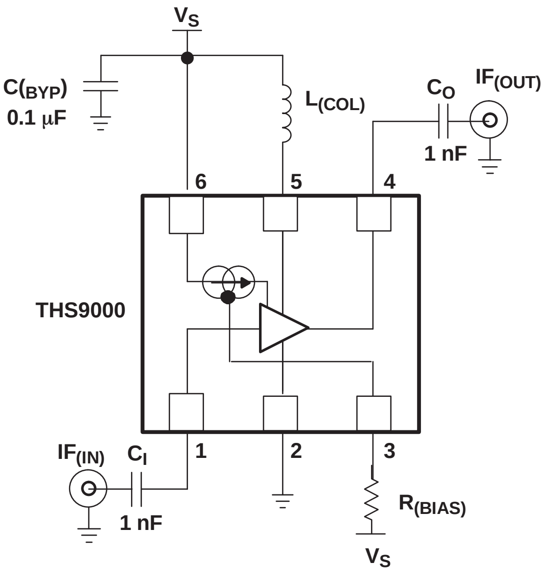


Figure 25. THS9000 Recommended Circuit (used for all tests)

Evaluation Module

Table 1 is the bill of materials, and Figure 26 and Figure 27 show the EVM layout.

Bill Of Materials

ITEM	DESCRIPTION	REF DES	QTY	PART NUMBER(1)
1	Cap, 0.1 μF, ceramic, X7R, 50 V	C1	1	(AVX) 08055C104KAT2A
2	Cap, 1000 pF, ceramic, NPO, 100 V	C2, C3	2	(AVX) 08051A102JAT2A
3	Inductor, 470 nH, 5%	L1	1	(Coilcraft) 0805CS-471XJBC
4	Resistor, 237 Ω, 1/8 W, 1%	R1	1	(Phycomp) 9C08052A2370FKHFT
5	Open	TR1	1	
6	Jack, banana receptance, 0.25" dia.	J3, J4	2	(SPC) 813
7	Connector, edge, SMA PCB jack	J1, J2	2	(Johnson) 142-0701-801
8	Standoff, 4-40 Hex, 0.625" Length		4	(KEYSTONE) 1808
9	Screw, Phillips, 4-40, .250"		4	SHR-0440-016-SN
10	IC, THS9000	U1	1	(TI) THS9000DRD
11	Board, printed-circuit		1	(TI) EDGE # 6453521 Rev.A

(1) The manufacturer's part numbers are used for test purposes only.

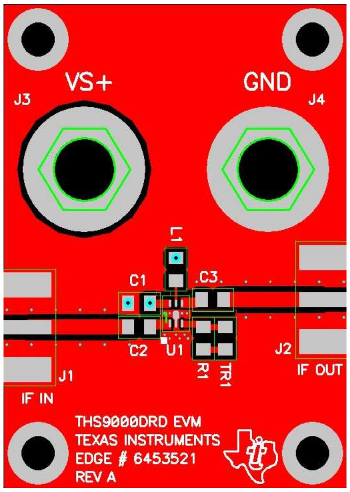


Figure 26. EVM Top Layout

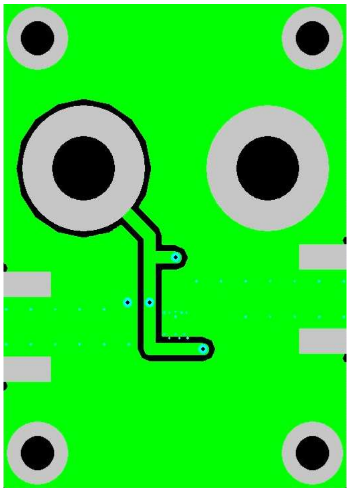


Figure 27. EVM Bottom Layout

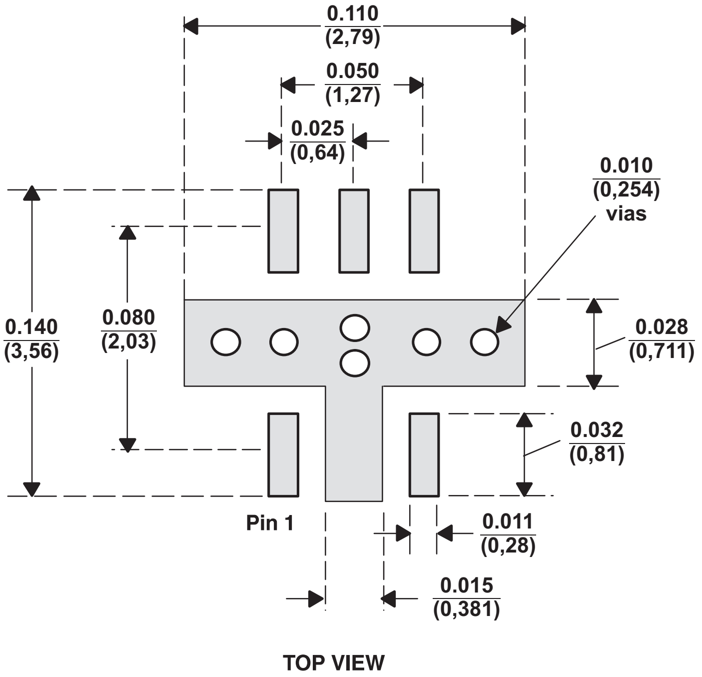


Figure 28. THS9000 Recommended Footprint dimensions are in inches (millimeters)

Revision History

Changes from Revision C (February 2007) to Revision D	Page
• Removed the DRD ordering options from the *Available Options* table	2
• Formatted the Absolute Maximum Ratings table to current standards	2
• Deleted DRD row from the *Dissipation Rating* table	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
THS9000DRDR	OBSOLETE	SON	DRD	6		TBD	Call TI	Call TI	-40 to 85		
THS9000DRDT	OBSOLETE	SON	DRD	6		TBD	Call TI	Call TI	-40 to 85		
THS9000DRWR	ACTIVE	VSON	DRW	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQX	Samples
THS9000DRWRG4	ACTIVE	VSON	DRW	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQX	Samples
THS9000DRWT	ACTIVE	VSON	DRW	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQX	Samples
THS9000DRWTG4	ACTIVE	VSON	DRW	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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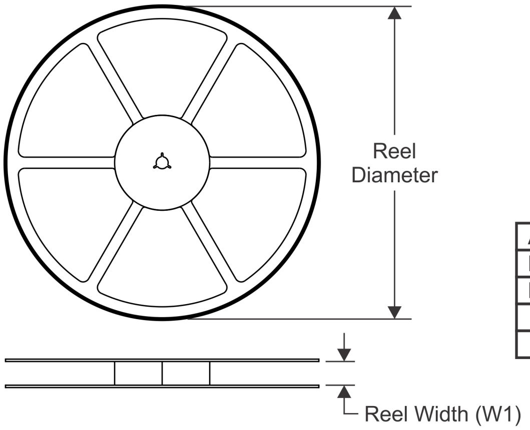
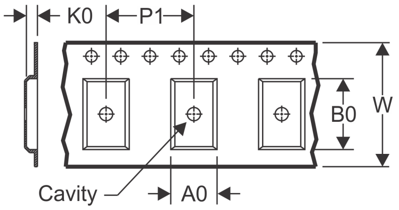
TAPE AND REEL INFORMATION

REEL DIMENSIONS

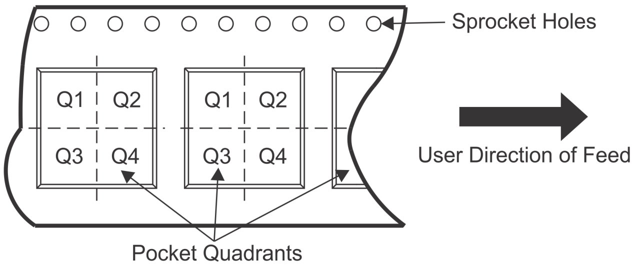


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

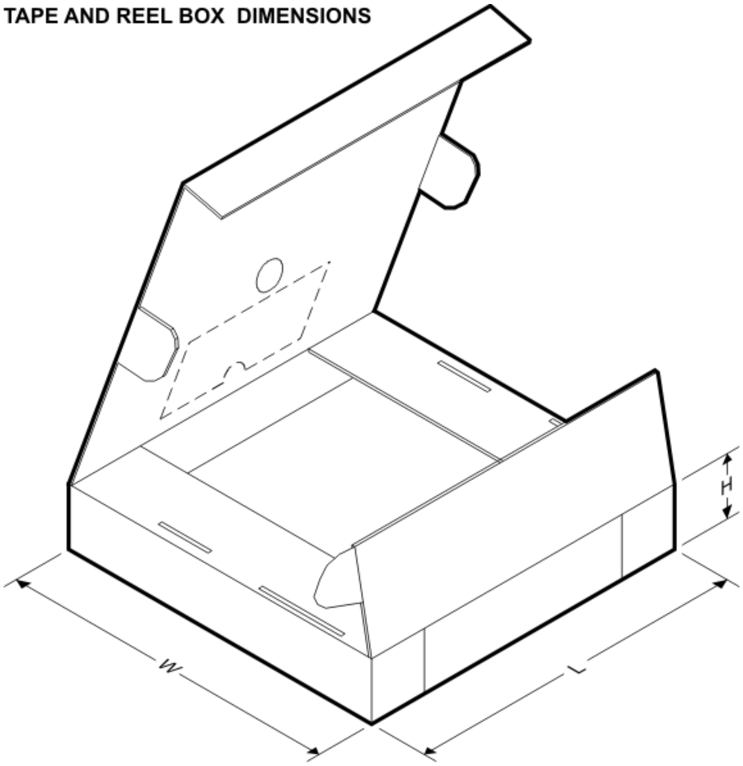
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS9000DRWR	VSON	DRW	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
THS9000DRWT	VSON	DRW	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

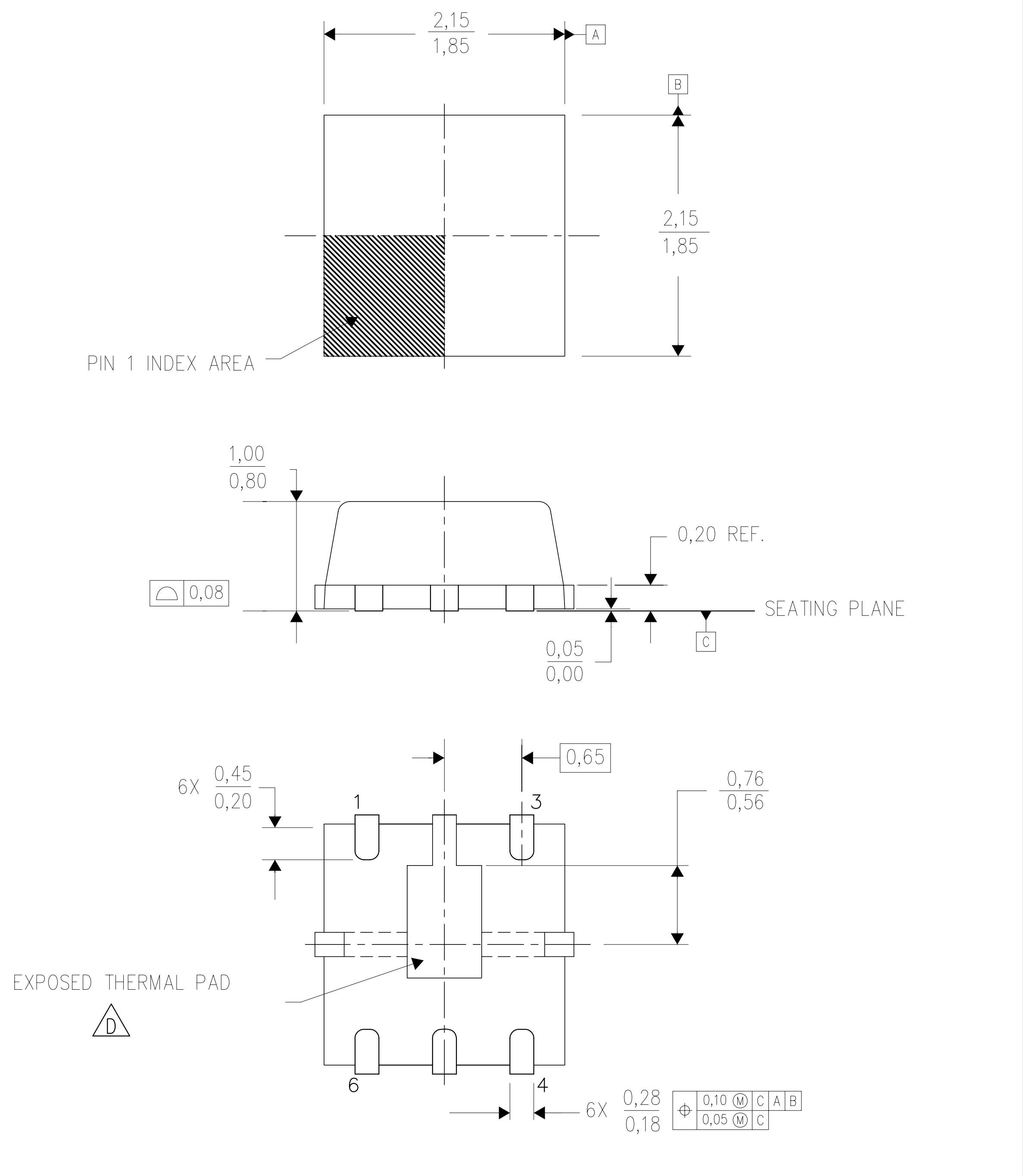
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

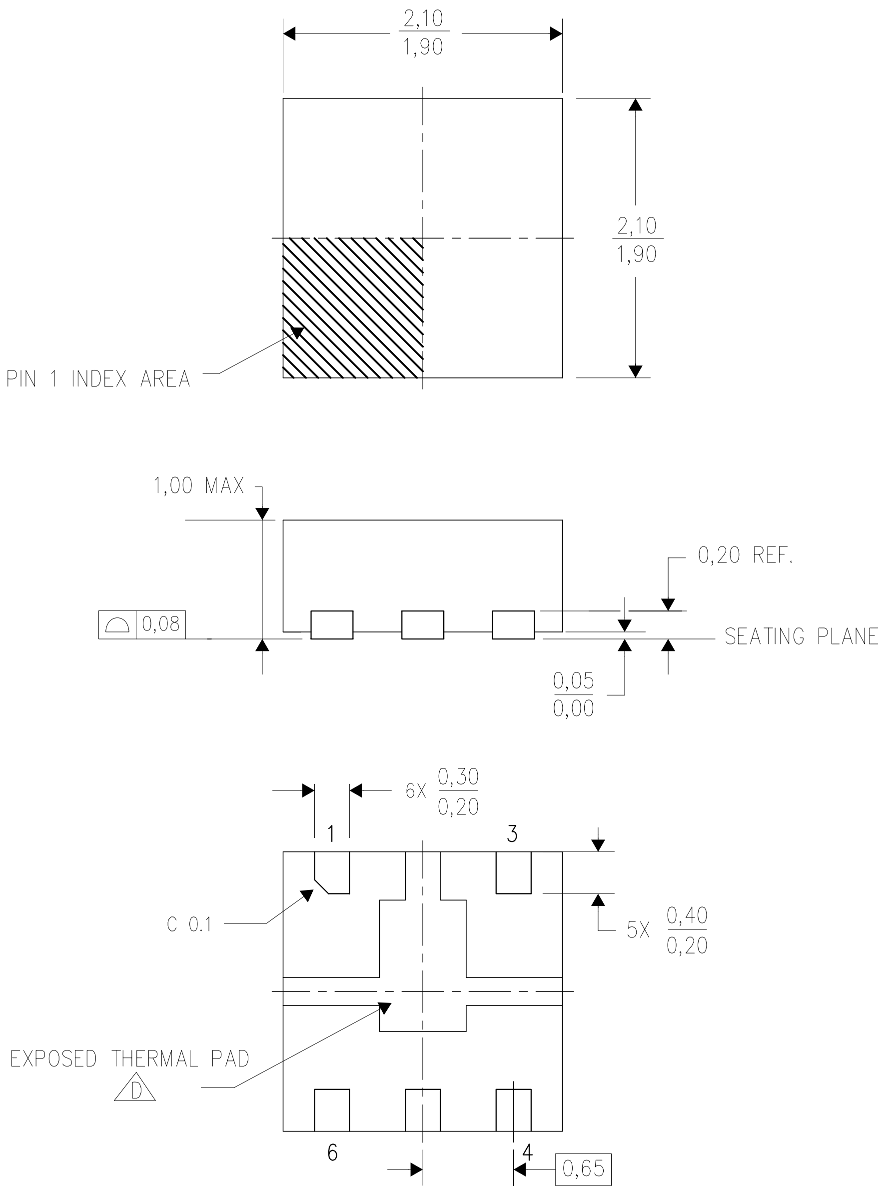
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS9000DRWR	VSON	DRW	6	3000	195.0	200.0	45.0
THS9000DRWT	VSON	DRW	6	250	195.0	200.0	45.0

DRD (S-PVSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

DRW (S-PVSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

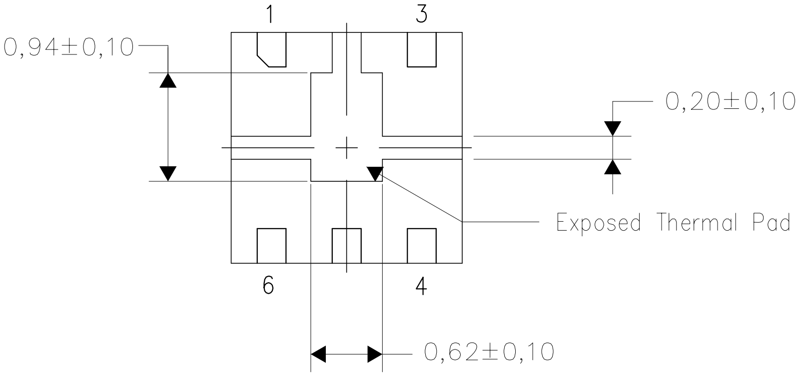
DRW (S-PVSON-N6) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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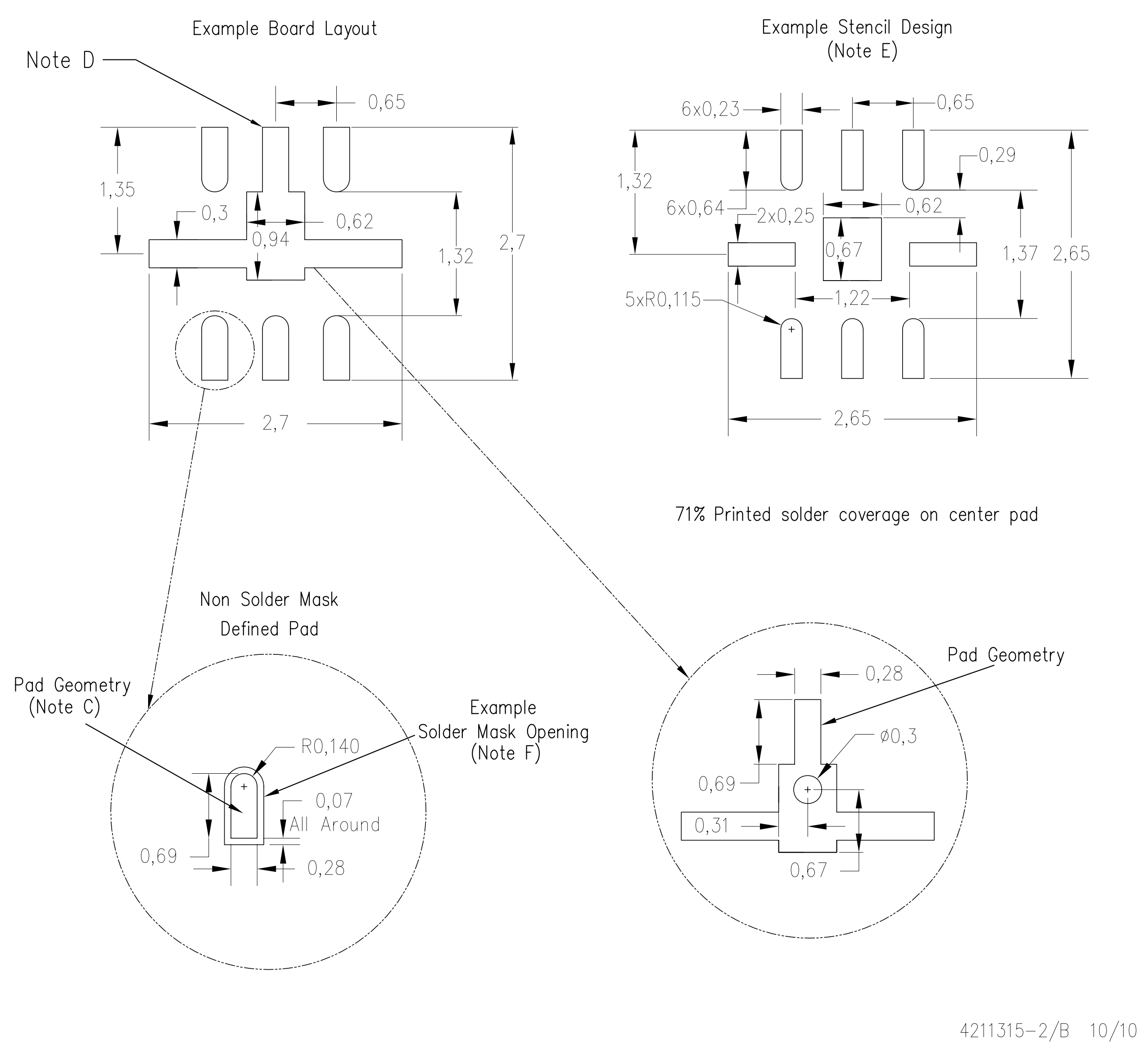
NOTE: A. All linear dimensions are in millimeters

DRW (S-PVSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-SM-782 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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