

TENTATIVE TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

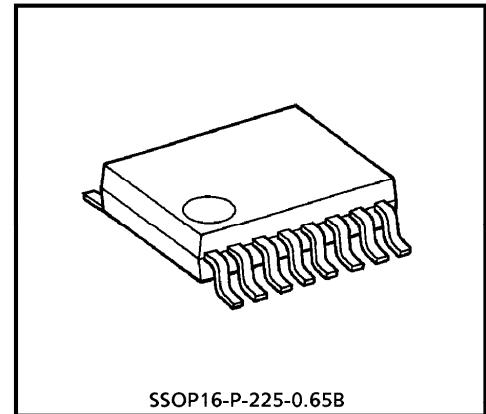
**TD7628FN****3-WIRE AND I<sup>2</sup>C BUS SYSTEM, 1.3GHz DIRECT TWO MODULUS-TYPE  
FREQUENCY SYNTHESIZER FOR TV AND CATV**

The TD7628FN can be combined with a micro CPU to create a highly functional frequency synthesizer. The control data conforms to 3-wire bus and standard I<sup>2</sup>C bus formats. BUS-SW can be used to easily switch for easy tuner system set-up.

**FEATURES**

- Direct two modulus-type frequency synthesizer
- Standard I<sup>2</sup>C bus format control with built-in read mode
- 3-wire bus format control
- 18-bit and 19-bit automatic discrimination circuit (when 3-wire bus selected)
- High voltage tuning amplifier built-in (Not built-in available)
- 4-bit bandswitch drive transistor
- 5-level A/D converter (when I<sup>2</sup>C bus selected)
- Frequency Step : 31.25kHz, 50kHz and 62.5kHz (at 4MHz X'tal used)
- Phase lock detector
- Various function settings via program data
- Four address settings via address selector (when I<sup>2</sup>C bus selected)
- Power on reset circuit
- Flat, compact package : SSOP16 (0.65mm pitch)
- Power on reset operation condition
  - Bandswitch register 1 to 4 : OFF
  - Tuning amplifier : ON
  - Charge-pump output current :  $\pm 60\mu\text{A}$
  - Phase comparator reference frequency divider ratio : 1/80
  - Counter data : All [ 0 ]

(Note) These devices are easy to be damaged by high static voltage or electric fields.  
In regards to this, please handle with care.



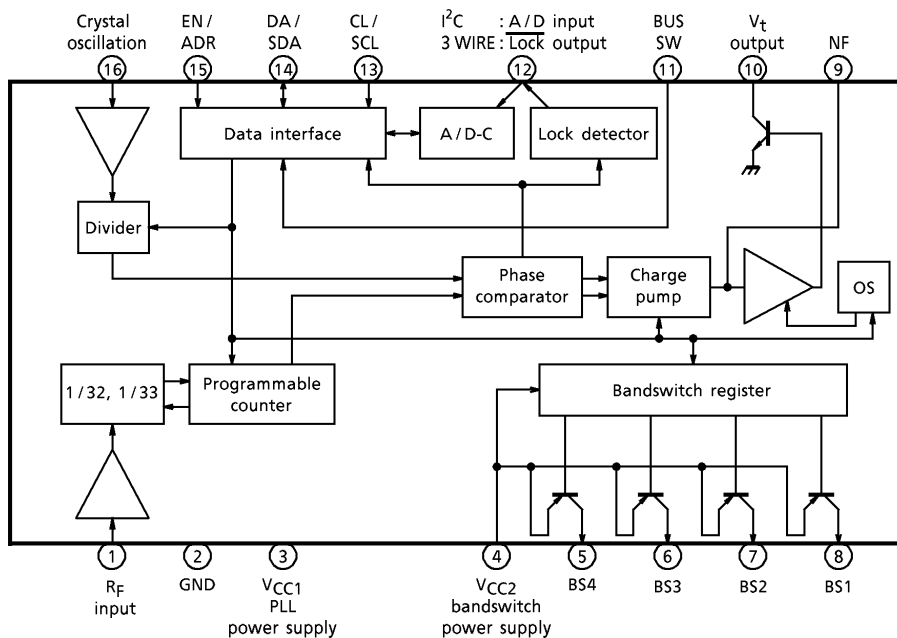
SSOP16-P-225-0.65B

Weight : 0.07g (Typ.)

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BLOCK DIAGRAM



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage 1	V <sub>CC1</sub>	6.0	V
Supply Voltage 2	V <sub>CC2</sub>	12	V
VT Amplifier Maximum Applied Voltage	V <sub>tMAX</sub>	38	V
Power Dissipation	P <sub>D</sub>	560	mW
Operating Temperature	T <sub>opr</sub>	- 20~85	°C
Storage Temperature	T <sub>stg</sub>	- 55~150	°C

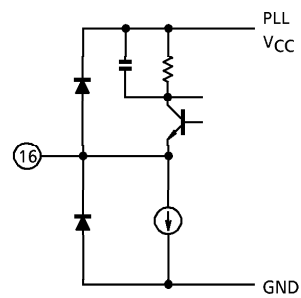
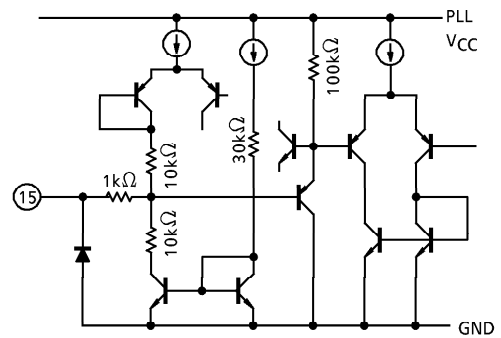
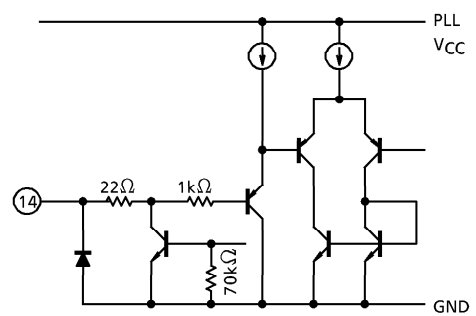
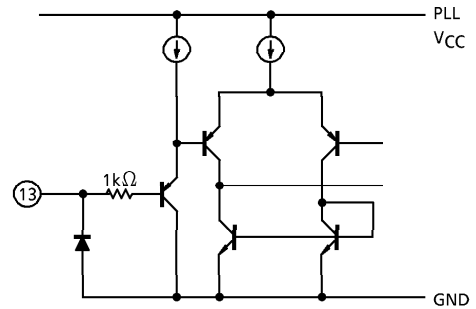
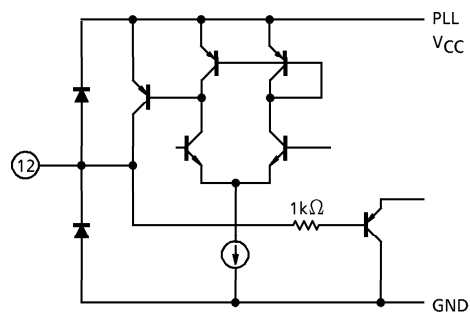
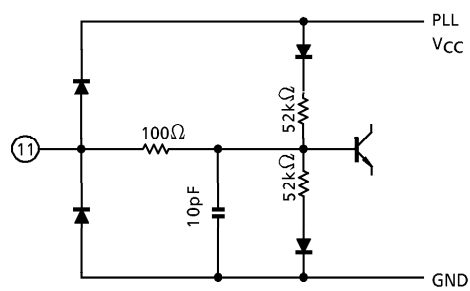
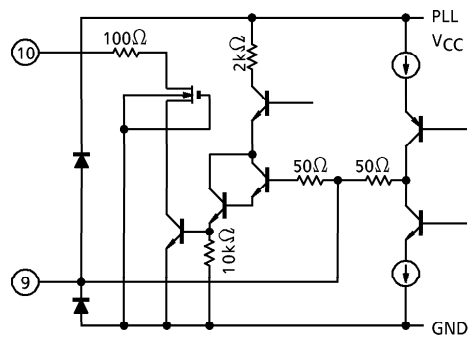
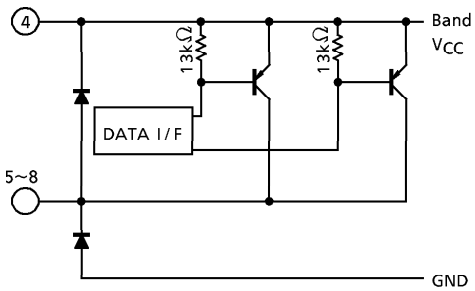
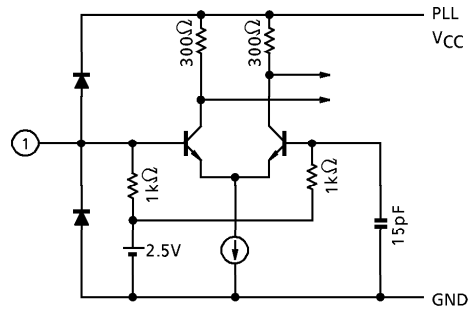
(Note 1) When using the device at above Ta = 25°C, decrease the power dissipation by 4.5mW for each increase of 1°C.

(Note 2) These devices are easy to be damaged by high static voltage or electric fields. In regards to this, please handle with care.

RECOMMENDED SUPPLY VOLTAGE

PIN No.	PIN NAME	MIN	TYP.	MAX	UNIT
3	V <sub>CC1</sub> : PLL Power Supply	4.5	5.0	5.5	V
4	V <sub>CC2</sub> : Band Switch Power Supply	V <sub>CC1</sub>	—	9.9	V

**PIN INTERFACE**



ELECTRICAL CHARACTERISTICS (Unless otherwise specified,  $V_{CC1} = 5V$ ,  $V_{CC2} = 9V$ ,  $V_{CC3} = 33V$ ,  $T_a = 25^\circ C$ )

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage 1	$V_{CC1}$	—	—	4.5	5.0	5.5	V
Supply Current 1	$I_{CC1}$	1	Bandswitch : OFF $V_t$ : OFF	13	16	21	mA
Supply Voltage 2	$V_{CC2}$	—	—	$V_{CC1}$	—	9.9	V
Supply Current 2	$I_{CC2-1}$	1	Bandswitch : 1 Band ON $I_{BD} = 30mA$ (LOAD)	—	35	39	mA
	$I_{CC2-2}$		Bandswitch : 2 Band ON $I_{BD} = 40mA$ (TOTAL LOAD)	—	50	58	
Bandswitch Drive Current	$I_{BD}$	3	Maximum Drive Current / 1 port	—	—	30	mA
Bandswitch Drive Voltage Drop	$V_{BD}$ Sat	3	$I_{BD} = 30mA$	—	0.2	0.4	V
Tuning Amplifier Output Voltage (closed loop)	$V_t$ OUT	1	$V_{CC3}$ (BT) = 33 [V], $R_L = 33$ [k $\Omega$ ]	0.3	—	33	V
Tuning Amplifier Max Input Current	$I_{Vt}$	1	$V_{CC3}$ (BT) = 33 [V]	—	—	3	mA
X'tal Operating Range	$OSC_{in}$	—	—	3.2	—	4.5	MHz
X'tal Negative Resistance	$OSCR$	1	—	—	1.5	—	k $\Omega$
X'tal External Input Level	$OSC_{in}$	—	—	250	—	1000	mVp-p
Ratio Setting Range	N14	—	15-bit counter	1024	—	32767	Ratio
	N13		14-bit counter	1024	—	16384	
Prescaler Input Sensitivity	$V_{in1}$	2	$f = 80 \sim 150MHz$	-25	—	+5	dBmW
	$V_{in2}$		$f = 150 \sim 1300MHz$	-30	—	+5	
Lock Output Low Voltage	$V_{LKL}$	1	(lock mode, 3-wire bus mode)	—	—	0.4	V
Lock Output High Voltage	$V_{LkH}$	1	(unlock mode, 3-wire bus mode)	4.6	—	—	V
Logic Input Low Voltage	$V_{BsL}$	1	Pins 13 to 15	-0.3	—	0.8	V
Logic Input High Voltage	$V_{BsH}$	1	Pins 13 to 15	3.0	—	$V_{CC1} + 0.3$	V
Logic Input Current (low)	$I_{BsL}$	1	Pins 13 to 15	-20	—	10	$\mu A$
Logic Input Current (high)	$I_{BsH}$	1	Pins 13 to 15	-10	—	20	
BUS-SW Low Input Voltage	$V_{BIL}$	1	—	0.0	—	0.8	V
BUS-SW High Input Voltage	$V_{BIH}$	1	—	3.0	—	$V_{CC1}$	

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
BUS-SW Low Current (low)	I <sub>BIL</sub>	1	—	- 200	—	—	μA
BUS-SW Low Current (high)	I <sub>BIH</sub>	1	—	—	—	200	
Charge Pump Output Current	I <sub>chg</sub>	2	CP = 『 0 』	± 50	± 60	± 90	μA
			CP = 『 1 』	± 230	± 280	± 420	
ACK Output Voltage	V <sub>ACK</sub>	1	I <sub>SINK</sub> = 3mA (I <sup>2</sup> C-bus mode)	—	—	0.4	V
A/D Converter Input Voltage	V <sub>ADC</sub>	—	—	0.0	—	V <sub>CC1</sub>	V
Set-up Time	T <sub>S</sub>	—	(3-wire bus mode) Refer to data timing chart	2	—	—	μs
Enable Hold Time	T <sub>S</sub> L			2	—	—	
Next Enable Stop Time	T <sub>NE</sub>			6	—	—	
Next Clock Stop Time	T <sub>NC</sub>			6	—	—	
Clock Width	T <sub>C</sub>			2	—	—	
Enable Set-up Time	T <sub>L</sub>			10	—	—	
Data Hold Time	T <sub>H</sub>			2	—	—	

## OPERATION INSTRUCTIONS

TD7628FN can be controlled with either the 3-wire bus or standard I<sup>2</sup>C bus.

The 3-wire bus mode is equipped with an 18-bit/19-bit automatic selection circuit.

Frequency steps can be switched, depending on the voltage applied to the BUS-SW pin.

The I<sup>2</sup>C bus conforms to the standard I<sup>2</sup>C bus format. The bus supports two-way bus communications control, consisting of WRITE mode where data are received and READ mode where data are transmitted. In READ mode, the voltage applied on the A/D converter input pin can be transmitted and output with 5-level resolution.

(This function is only valid when the I<sup>2</sup>C bus is selected. When the 3-wire bus is selected, the A/D converter input pin function as the  $\overline{\text{LOCK}}$  output pin.)

Addresses can be set using the hardware bits. Three programmable addresses are supported. 3-wire bus and standard I<sup>2</sup>C bus are switches by the voltage applied on the BUS-SW pin.

When the supply voltage ( $V_{CC1}$ ) is applied, the power-on reset circuit operates. Before data are input, counter data are all initialized to 『 0 』 : band switches are all initialized to off.

### FUNCTION CHART

NAME	3-WIRE BUS MODE	I <sup>2</sup> C BUS MODE
BUS-SW	『 OPEN 』 or 『 $V_{CC}$ 』	『 GND 』
CL/SCL	CLOCK INPUT	SCL INPUT
DA/SDA	DATA INPUT	SDA IN/OUTPUT
EN/ADR	ENABLE INPUT	ADDRESS
$\overline{\text{LOCK}}$ /ADC	$\overline{\text{LOCK}}$	ADC

### — 3-WIRE BUS COMMUNICATIONS CONTROL —

The 3-wire bus used normal 18-bit and 19-bit data (bandswitch information and programmable counter information) and 27-bit test data (charge pump current setting, reference frequency divider ratio setting, and testing item functions) are available.

The program frequency can be calculated together with normal data and test data.

$$f_{osc} = f_r \times N$$

$f_{osc}$  : Program frequency

$f_r$  : Phase comparator reference frequency (Step frequency)

N : Counter total ratio

(1) Normal data

Depending on the voltage (OPEN, V<sub>CC</sub>) applied on the BUS-SW pin and the transfer DATA bit length, the X'tal divider ratio setting, phase comparator reference frequency, and step frequency of the normal data are as shown in the table below.

NORMAL DATA FUNCTION TABLE

BUS-SW INPUT	TRANSFER DATA	X'TAL RATIO	REFERENCE FREQUENCY	STEP FREQUENCY
「V <sub>CC</sub> 」	18-bit	Cannot be set	←	←
「V <sub>CC</sub> 」	19-bit	1 / 80	50kHz	50kHz
「OPEN」	18-bit	1 / 64	62.5kHz	62.5kHz
「OPEN」	19-bit	1 / 128	31.25kHz	31.25kHz

(Note 1) The step frequency at 4MHz X'tal used

(Note 2) During "OPEN", automatically set with transmitted bit length (18↔19 possible)

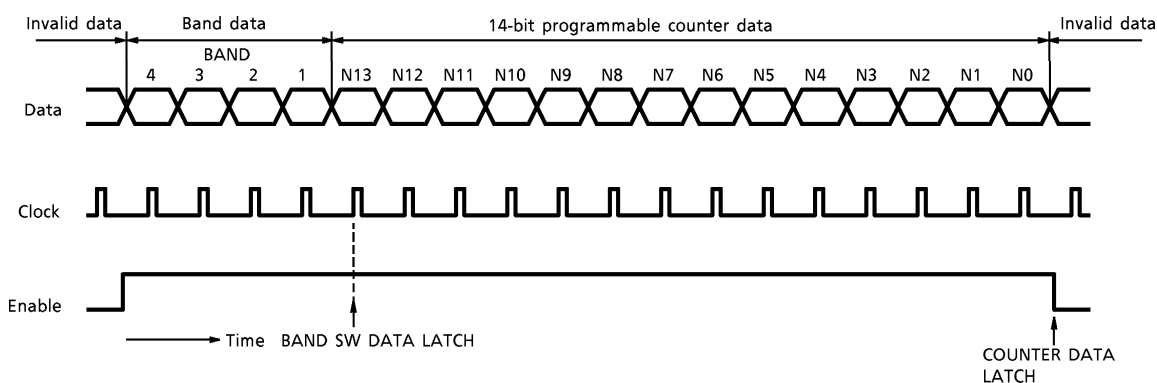


Fig.1 Normal data format (18-bit transmission)

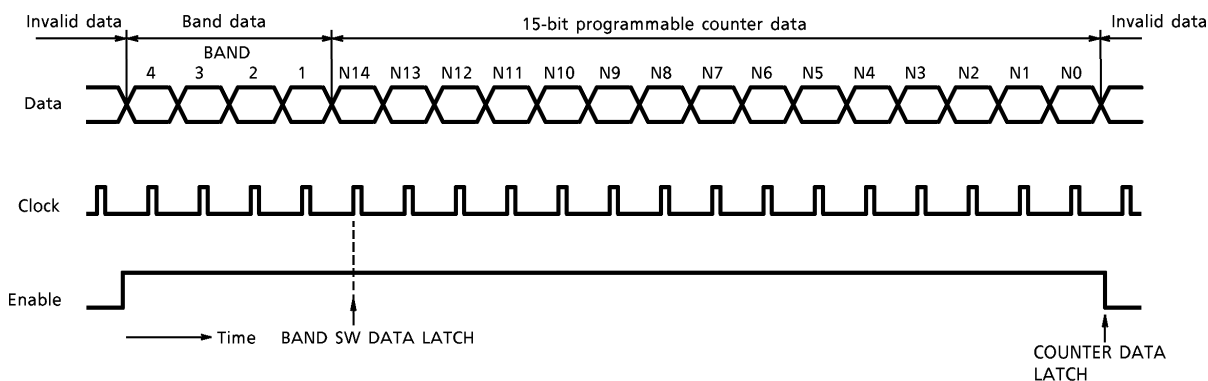


Fig.2 Normal data format (19-bit transmission)

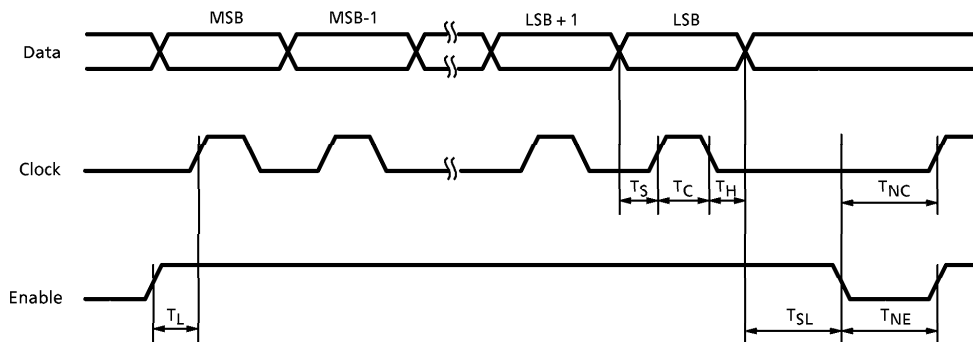


Fig.3 Data timing chart (Falling edge timing)

- 18-bit DATA TRANSMISSION :

During a high level of the enable signal, the data is clocked into the register on the falling edge of the clock.

The clock number during a high level of the enable signal must be set to 18-bit for the latch condition. (The number of clock rising edges is 18).

For latch timing, the first four bits, which control the bandswitch buffers, are loaded at the fifth rising edge of the clock, and the data is updated.

The programmed counter data transmits the 18-bit data, latched on the falling edge of the enable signal.

During 18-bit data transmission, "N14" programmable counter data is constantly set to [ 0 ], and the phase comparator reference frequency divider ratio is automatically set to "1/64".

Details of the data timing, see the data timing chart (Figure 1)

- 19-bit DATA TRANSMISSION :

During a high level of the enable signal, the data is clocked into the register on the falling edge of the clock.

The clock number during a high level of the enable signal must be set to 19-bit for the latch condition. (The number of clock rising edge is 19).

For latch timing, the first four bits, which control the bandswitch buffers, are loaded at the fifth rising edge of the clock, and the data is updated.

The programmed counter data transmits the 19-bit data, latched on the falling edge of the enable signal.

During 19-bit data transmission, the phase comparator reference frequency divider ratio is automatically set to "1/80" or "1/128" in BUS-SW mode.

Details of the data timing, see the data timing chart (Figure 1)



**(2) TEST MODE**

In the test mode, the settings can be changed and the functions can be checked. Change from the normal mode to the test mode with a 27-bit or more of clock and data transmission during a high level of the enable signal.

The data are latched at the 27th falling edge of the clock signal, validating the previous 27-bit data. The latch timing is the same as normal data.

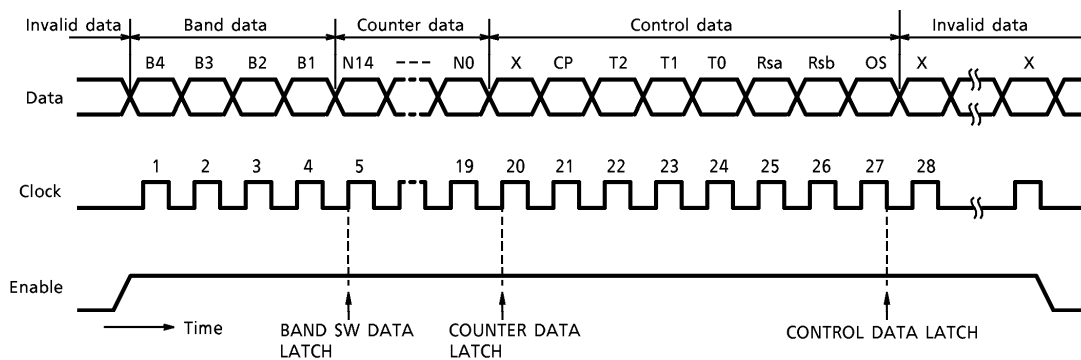
The 4-bit bandswitch data are latched at the 5th bit rising edge of the clock signal, and the data is updated.

The programmable counter data are latched at the 20th bit rising edge of the clock signal, and the data is updated.

The test data are latched at the 27th bit falling edge of the clock signal, and the data is updated.

When the mode is changed from test to normal, RSa changes depending on the data bit length (18 or 19 bits, automatic discrimination). The data set in RSb in test mode are retained (see the table below).

REFERENCE FREQUENCY DIVIDER RATIO SETTING VIA TEST MODE	DATA TRANSMISSION LENGTH	SET REFERENCE FREQUENCY DIVIDER RATIO
1 / 64	18-bit	1 / 64
	19-bit	1 / 128
1 / 80	18-bit	1 / 80
	19-bit	1 / 80
1 / 128	18-bit	1 / 64
	19-bit	1 / 128



**Fig.4 Test data format**

(Note) The data timing is the same as normal data.

**TEST DATA SPECIFICATIONS**

- B4~B1 : Band drive data  
     『 0 』 : OFF  
     『 1 』 : ON
- N14~N0 : Programmable divider data
- CP : Charge pump output current  
     『 0 』 : ±60μA (Typ.)  
     『 1 』 : ±280μA (Typ.)
- T2, T1, T0 : Test mode setting bits

CHARACTERISTIC	T2	T1	T0	NOTE
Normal operation	0	0	1	—
Reference signal output	1	0	0	Reference signal output : B4, Counter output : B2
1/2 counter divider output	1	0	1	Reference signal output : B4, 1/2 counter output : B2
Phase comparator test	0	0	0	Comparative signal input : DA Reference signal input : CL (check output : NF)

X : Don't care

(Note) When testing the counter divider output, programmable counter data input is necessary.

- Rsa, Rsb : X'tal Reference frequency divider ratio select bits

RSa	RSb	DIVIDER RATIO	STEP FREQUENCY
1	1	1 / 64	62.5k
0	1	1 / 128	31.25k
X	0	1 / 80	50.0k

X : Don't care

(Note) When the mode is changed from test to normal, RSa changes depending on the data bit length (18 or 19 bits, automatic discrimination). The data set in RSb in test mode are retained.

- OS : Tuning amplifier control bit  
     『 0 』 : Tuning amp ON (Normal operation)  
     『 1 』 : Tuning amp OFF (V<sub>t</sub> Output is High impedance)
- X : Don't care

— I<sup>2</sup>C BUS COMMUNICATIONS CONTROL—

TD7628FN conform to standard I<sup>2</sup>C bus format.

The I<sup>2</sup>C bus mode enables two-way bus communications with the WRITE mode, which receives data, and READ mode, which status data.

WRITE and READ mode are set using the last bit (R/W bit) of the address byte.

If the last address bit is set to [ 0 ], WRITE mode is set ; if set to [ 1 ] READ mode is set.

Address can be set using the hardware bits. Three programmable address can be programmed.

With this setting, multiple frequency synthesizers can be used in the same I<sup>2</sup>C bus line.

The address for the hardware bit setting can be selected by applying voltage to the address setting pin (ADR : Pin 15). An address is selected according to the set bits.

When the correct address byte is received, during acknowledgment, serial data (SDA) line is "Low".

If WRITE mode is set at this time, when the data byte is programmed, the serial data (SDA) line is "Low" during the next acknowledgment.

## a) WRITE mode (setting command)

When WRITE mode is set, byte 1 segment the address data ; bytes 2 and 3 segment the frequency data ; byte 4 segment the divider ratio setting and function setting data ; and byte 5 segment the output port data.

Data are latched and transferred at the end of byte 3, byte 4 and byte 5.

Byte 2 and byte 3 are latched and transferred is done with a two byte set (byte 2 + byte 3).

Once a correct address is received and acknowledged, the data type is determined according to [ 0 ] or [ 1 ] set in the first bit of the next byte. That is, if the first bit is [ 0 ], the data are frequency data ; if [ 1 ], function setting or output port data.

Until the I<sup>2</sup>C bus STOP CONDITION is detected, the additional data can be input without transmitting the address again. (Ex : Frequency sweep is possible with additional frequency data.)

If data transmission is aborted, data programmed before the abort are valid.

Byte 1 can set the hardware bit with address data.

The hardware bit is set with voltage applied to the address setting pin (ADR : Pin 15).

Bytes 2 and 3 are stored in the 15-bit shift register with counter data for the frequency setting, and control the 15-bit programmable counter ratio.

The program frequency can be calculated in the following formula :

$$f_{osc} = f_r \times N$$

$f_{osc}$  : Program frequency

$f_r$  : Phase comparator reference frequency (Step frequency)

N : Counter total ratio

$f_r$  is calculated using the crystal oscillator frequency and the reference frequency divider ratio set in byte 4 (control byte). ( $f_r = X'tal \text{ oscillator frequency} / \text{reference frequency divider ratio}$ )

The reference frequency divider ratio can be set to 1/64, 1/128 and 1/80.

When using a 4MHz crystal oscillator,  $f_r = 62.5\text{kHz}$ , 31.25kHz and 50kHz.

The step frequency are 62.5kHz, 31.25kHz, and 50kHz.

Byte 4 is a control byte used to set function. Bit 2 (CP) controls the output current of the charge-pump circuit. When bit 2 is set to '0' : the output current is set to  $\pm 60\mu\text{A}$  ; when set to '1' ,  $\pm 280\mu\text{A}$ .

Bit 3 ( $T_2$ ), bit 4 ( $T_1$ ) and bit 5 ( $T_0$ ) are used to set test mode. They are used to set the phase comparator reference signal output, and counter divider output.

For details of test mode, see the test mode setting table.

Bit 6 (RSa) and bit 7 (RSb) are used to set the X'tal reference frequency divider ratio.

For details of the X'tal reference frequency divider ratios, see the table for X'tal reference frequency divider ratios.

Bit 8 (OS) is used to set the charge-pump drive amplifier output setting. When bit 8 is set to '0' the output is ON (Normal Use) ; when set to '1' the output is OFF ( $V_t$  Output is High impedance).

Byte 5 is used to set and control the output port (Bands 1~4).

When an output port set to '0' is OFF ; when set to '1' is ON.

Two output ports can be operation turned on, but be sure to keep the total output current under 50mA.

#### b) READ mode (status request)

When READ mode is set, power-on reset operation status, phase comparator lock detector output status, and 5-level A/D converter pin input voltage status are output to the master device.

Bit 1 (POR) indicates the power-on reset operation status. When the power supply of  $V_{CC1}$  stops, bit 1 is set to '1' . The condition for reset to '0' , voltage supplied to  $V_{CC1}$  is 3V or higher, transmission is requested in READ mode, and the status is output. (when  $V_{CC1}$  is turned on, bit 1 is also set to '1' .)

Bit 2 (FL) indicates the phase comparator lock status. When locked, '1' is output ; when unlocked, '0' is output.

Bits 6, 7 and 8 ( $A_2$ ,  $A_1$ ,  $A_0$ ) indicate the 5-level A/D converter status. The voltage applied to the A/D converter input pin (pin 12) is output through a 5-level resolution.

For the voltage applied on the A/D converter input pin, 5-level resolution, and the output bits, see the table.

(Ex : The AFT output voltage data can be given to the master device.)

**DATA FORMAT**

a) WRITE MODE

BYTE		MSB							LSB	
1	Address Byte	1	1	0	0	0	MA1	MA0	R/W = 0	ACK
2	Divider Byte①	0	N14	N13	N12	N11	N10	N9	N8	ACK
3	Divider Byte②	N7	N6	N5	N4	N3	N2	N1	N0	ACKⓁ
4	Control Byte	1	CP	T2	T1	T0	RSa	RSb	OS	ACKⓁ
5	Band SW Byte	x	x	x	x	B4	B3	B2	B1	ACKⓁ

x : DON'T Care

ACK : Acknowledged

Ⓛ : Latch and transfer timing

b) READ MODE

BYTE		MSB							LSB	
1	Address Byte	1	1	0	0	0	MA1	MA0	R/W = 1	ACK
2	Status Byte	POR	FL	1	1	1	A2	A1	A0	—

ACK : Acknowledged

**DATA SPECIFICATIONS**

- MA1, MA0 : Programmable hardware address bits

ADDRESS PIN APPLIED VOLTAGE	MA1	MA0
0~0.1V <sub>CC1</sub>	0	0
0.4V <sub>CC1</sub> ~0.6V <sub>CC1</sub>	1	0
0~V <sub>CC1</sub>	0	1
0.9V <sub>CC1</sub> ~V <sub>CC1</sub>	1	1

- CP : Charge-pump output current setting

〔 0 〕 : ±60μA (Typ.)

〔 1 〕 : ±280μA (Typ.)

- T2, T1, T0 : Test mode setting

CHARACTERISTIC	T2	T1	T0	NOTE
Normal operation	0	0	1	—
Reference signal output	1	0	0	Reference signal output : B4, Counter output : B2
1/2 counter divider output	1	0	1	Reference signal output : B4, 1/2 counter output : B2
Phase comparator test	0	0	0	Comparative signal input : SDA Reference signal input : SCL (check output : NF)

X : Don't care

(Note) When testing the counter divider output, programmable counter data input is necessary.

- RSa, RSb : X'tal reference frequency divider ratio select bits

RSa	RSb	DIVIDER RATIO	STEP FREQUENCY
1	1	1 / 64	62.5k
0	1	1 / 128	31.25k
X	0	1 / 80	50.0k

X : Don't care

- OS : Tuning amplifier control setting
  - 〔 0 〕 : Tuning amp ON (Normal operation)
  - 〔 1 〕 : Tuning amp OFF ( $V_t$  Output is High impedance)

- POR : Power-on reset flag
  - 〔 0 〕 : Normal operation
  - 〔 1 〕 : Reset operation

- FL : Lock detect flag
  - 〔 0 〕 : Unlocked
  - 〔 1 〕 : Locked

- A2, A1, A0 : 5-level A/D converter status.

ADC PIN APPLIED VOLTAGE	A2	A1	A0
0.60V <sub>CC1</sub> ~V <sub>CC1</sub>	1	0	0
0.45V <sub>CC1</sub> ~0.60V <sub>CC1</sub>	0	1	1
0.30V <sub>CC1</sub> ~0.45V <sub>CC1</sub>	0	1	0
0.15V <sub>CC1</sub> ~0.30V <sub>CC1</sub>	0	0	1
0~0.15V <sub>CC1</sub>	0	0	0

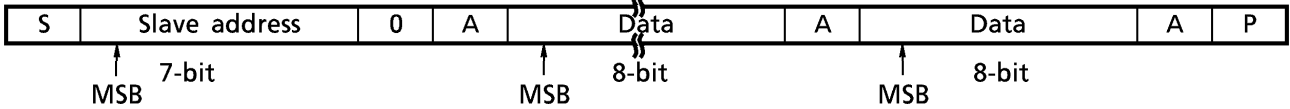
(\*) Accuracy is  $\pm 0.03 \times V_{CC1}$

- X : DON'T Care

**I<sup>2</sup>C BUS CONTROL SUMMARY**

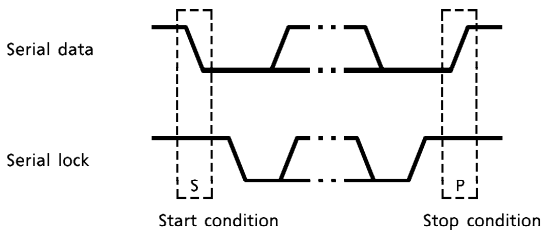
The bus control format of TD7628FN conforms to the Philips I<sup>2</sup>C bus control format.

**Data transmission format**

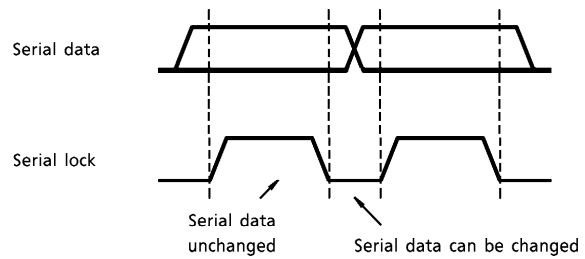


S : Start condition  
 P : Stop condition  
 A : Acknowledge

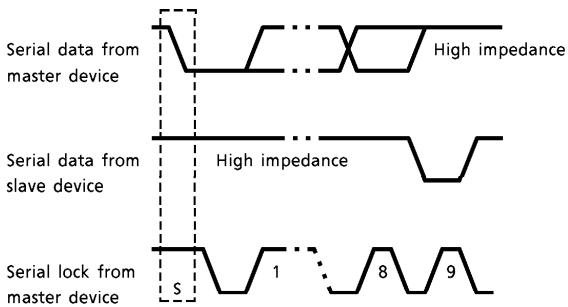
**(1) Start/Stop condition**



**(2) Bit transfer**



**(3) Acknowledge**

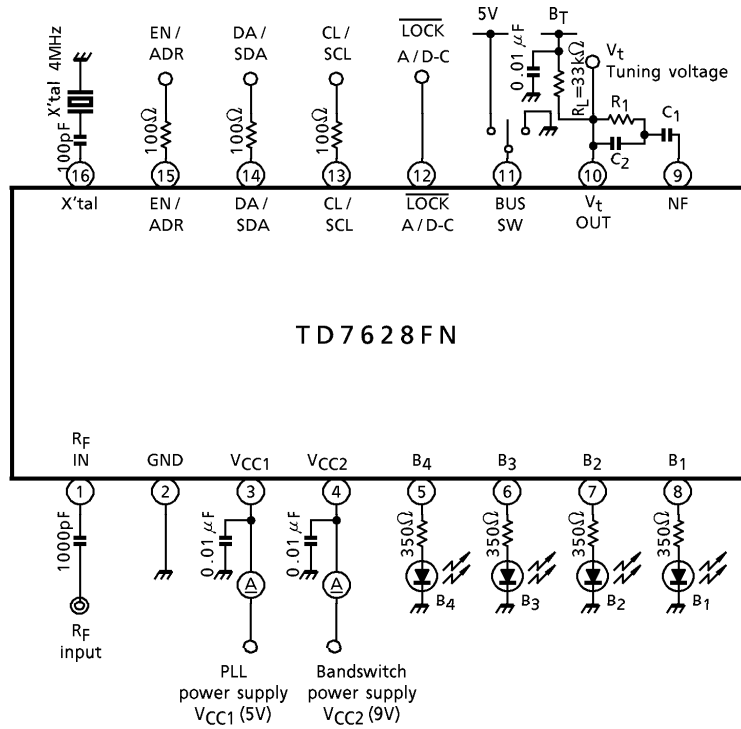


**(4) Slave address**

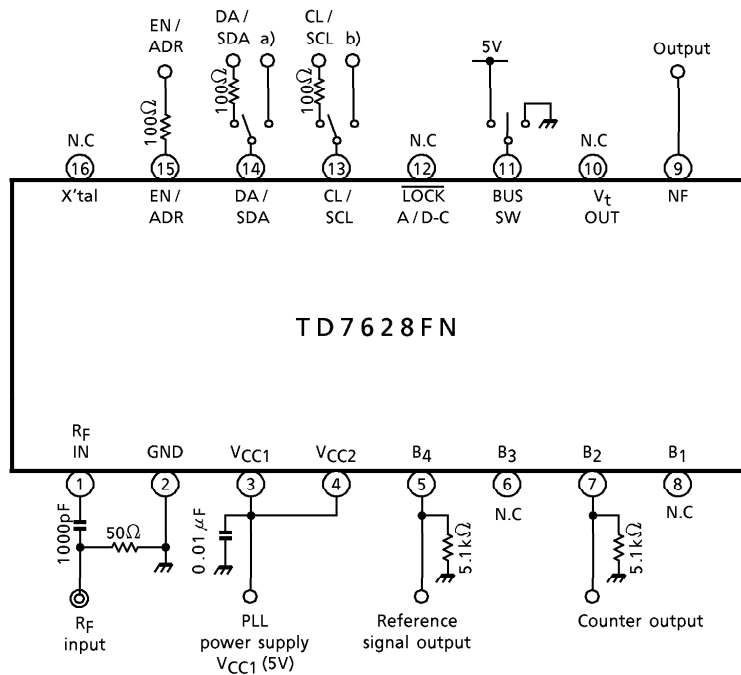
A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	R/W
1	1	0	0	0	*	*	0

Purchase of TOSHIBA I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Tights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

**TEST CIRCUIT 1**  
Evaluation circuit board



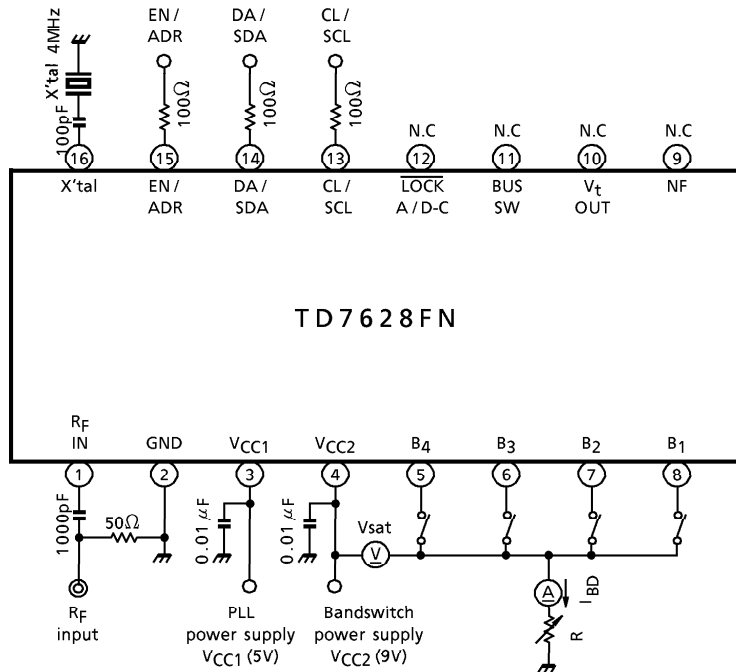
**TEST CIRCUIT 2**  
Input sensitivity test circuit  
Test mode circuit



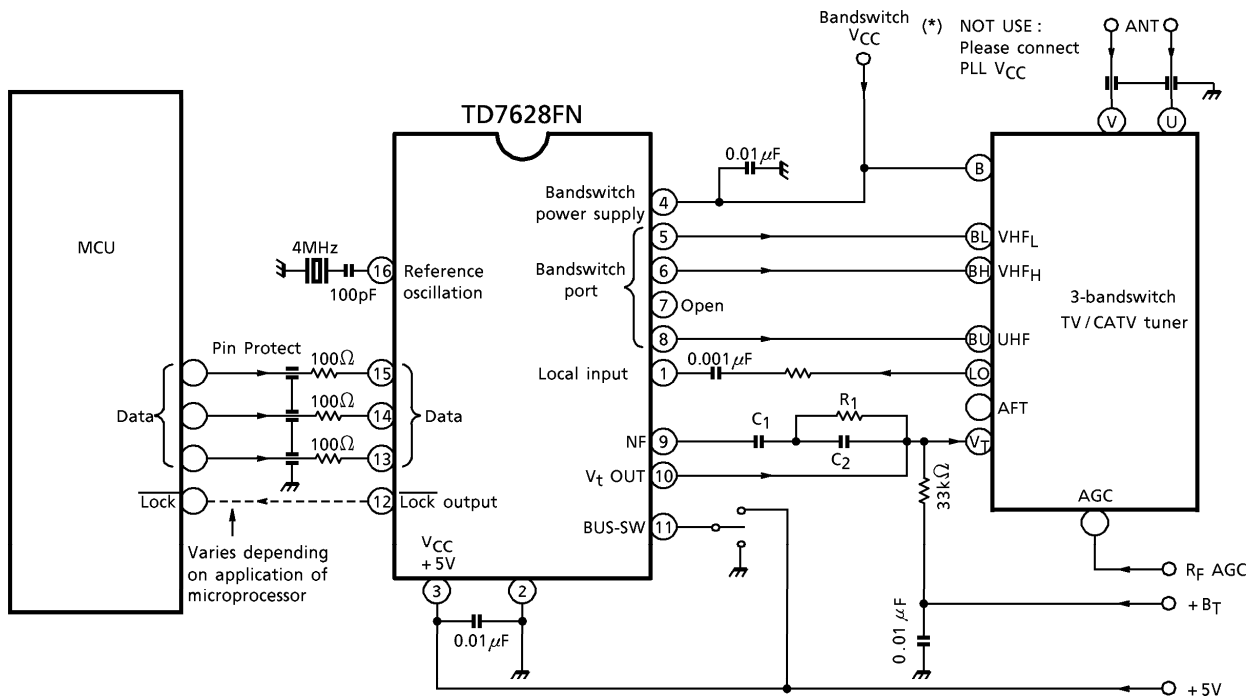
(Notes)  
a) : Comparative signal input  
b) : Reference signal input



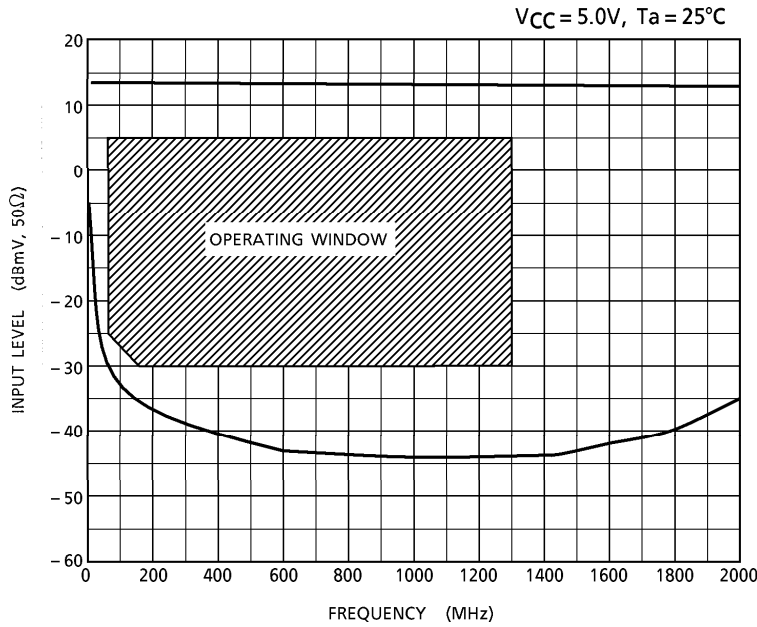
**TEST CIRCUIT 3**  
Bandswitch drive test circuit



**SYSTEM APPLICATION DIAGRAM**



**TYPICAL INPUT SENSITIVITY CURVE**



**FILTER COMPONENT EXPRESSION**

$$C1 = [Kv * I_{comp} / (2\pi)] / (\omega_n^2 * N)$$

$$R1 = [2 * \epsilon] / (\omega_n * C1)$$

$$C2 = 1 / (2\pi * f_c * R1)$$

with :

K<sub>v</sub> = Oscillator control sensitivity (radian / Second / Volts)

I<sub>comp</sub> = Charge-pump current (A)

ω<sub>n</sub> = Natural radian frequency (radian / Second)

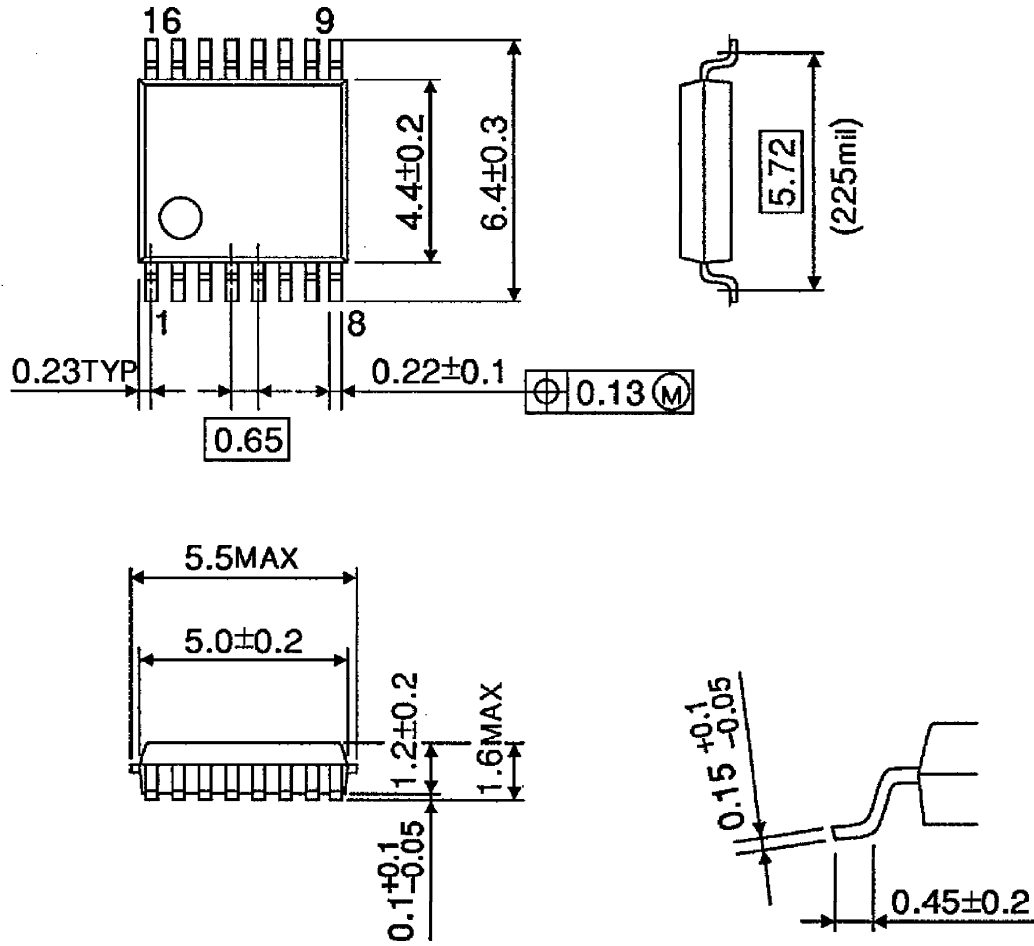
N = Total counter ratio

ε = Damping-factor (generally : damping-factor is about 0.5~1.0)

f<sub>c</sub> = filter cut-off frequency with combination resistor R1.  
(generally : f<sub>c</sub> is about f<sub>r</sub> (reference frequency) / 20)

**OUTLINE DRAWING**  
SSOP16-P-225-0.65B

Unit : mm



Weight : 0.07g (Typ.)