INTEGRATED CIRCUIT TOSHIBA

TECHNICAL DATA

TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT TD6358P, TD6358N

SILICON MONOLITHIC

FREQUENCY SYNTHESIZER FOR TV/CATV

The TD6358P and TD6358N are single-chip frequency synthesizer ICs, which can organization high-performance frequency synthesizer systems in combination with a 4bit μ CPU controller.

The TD6358P integrates high input sensitivity ECL prescaler, I²L programmable counter, PLL logic and bandswitch drive decoder in a DIP20-pin small package. The TD6358N is packaged in a shrink 20-pin package even smaller than TD6358P.

FEATURES

• High input sensitivity

 $f_{in} = 80 \sim 100 MHz$: -24dBmW (50 Ω) (Min.) $f_{in} = 0.1 \sim 1 GHz$: $-27dBmW (50\Omega) (Min.)$

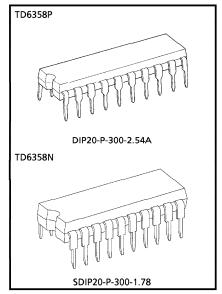
• Wide operating frequency: 1GHz (Max.)

 Simple control bus : 19bit serial input

5V single power supply operation

3.2MHz basic oscillator and 50kHz frequency step

Bandswitch driver : 4 channels



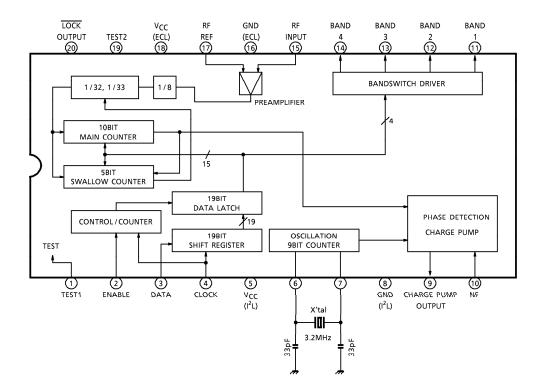
Weight DIP20-P-300-2.54A : 2.25g (Typ.) SDIP20-P-300-1.78 : 1.02g (Typ.)

(Note) Handle with care as this product is weak at surge voltage.

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BLOCK DIAGRAM



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TERMINAL FUNCTION

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
1	Test Pin 1	Low level: this will be in normal use operation mode when connected to GND or open. In order to prevent a static breakdown, it will be more effective to connect to GND. High level: this will be in test mode when connected to VCC.	1 20κΩ
2	Enable Input	This is an enable pulse input terminal at normal use operation. This will be a test mode select terminal of test mode by means of the pin 1 mode select pin. In order to prevent a static breakdown, it will be effective to connect in series a resistor of about $1k\Omega$. The pins 3 and 4 below are the same as this pin.	2 18kΩ
3	Data Input	This is a data input terminal in normal mode. In test mode 1 or 2, this will be a main counter output terminal. In test mode 3, this can be an external input terminal of comparison signal of phase comparator (a counter output terminal in normal mode).	3 18kΩ C 005
4	Clock Input	This is a clock pulse input terminal in normal mode. In test mode 1 or 2, this will be an output terminal of reference signal whose crystal oscillator is divided by 29. In test mode 3, this can be an input terminal of external reference signal.	4 18kΩ C C 0005
5	Logic V _{CC}	This is logic circuit power supply. Connect a bypass condenser between this pin and pin 8.	_

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PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
6 7	Crystal Oscillation	This is a crystal oscillation terminal to make the reference signal. Make sure to use the logic GND of pin 8 as this oscillates in a big amplitude (about 800mV _{p-p}).	G 10KΩ 75.
8	Logic GND	This is used for crystal oscillator GND as is logic GND. Never wire this pin close to the high frequency GND of pin 16.	l
9 10	Frequency Phase Comparator Output	In normal use, this compares a high frequency wave input with frequency data and feeds back its difference by means of the supply pump.	10kΩ 3 150Ω
11 ~ 14	Bandswitch	This can make the 4 band switching operate independently. The external driver can freely be operated anywhere between 1~4 pins. Connect an unused pin to the bandswitch power supply.	11-14 1kΩ 5V
15 17	Reference Bias By RF Input	This is an input terminal of local oscillation of tuner. In order to prevent disturbance or unwanted resonance, use the pattern of short distance or lead wire for pin 15. Also, connect a bypass condenser to pin 16 for pin 17 as well.	(a) (b) (c) (c) (c) (c) (c) (c) (c) (c) (c) (c
16	High Frequency GND	This is mainly used for a bypass condenser of pins 17 and 18 as is high frequency GND. Also the pattern should be lay out so as to be separated from the logic GND of pin 8.	_

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PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
18	High Frequency VCC	This is high frequency circuit power supply. Connect a bypass condenser between this pin and pin 8.	_
19	Test Pin 2	This is used only when in test mode 2. This terminal is possible to be input to the main counter without passing through a 1/8 prescaler. Leave this pin open in normal use.	(10, 10, 10, 10, 10, 10, 10, 10, 10, 10,
20	Lock Output	In normal use, a pull up resistor is connected to VCC. It will be low level only when PLL is locked. In test mode, this will be the test 1 or 2 select terminal and in mode 3, this will be a 256 divided output terminal of high frequency input. This is used for measuring the input sensitivity of a prescaler.	20 1κΩ

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OPERATION WHEN IN TEST MODE

If the test 1pin (pin 1) is set to high level, this will be test mode. There are three kinds of test modes as follows:

(1) Mode 1, Mode 2

In mode 1 and 2, a test to inspect the PLL lock condition is executed. After inputting data to the main counter and swallow counter by means of the method indicated in the diagram 2, the test 1 terminal (pin 1) will be set to high level while the enable terminal (pin 2) is held to low level. In this condition, a comparating frequency signal is output to the clock terminal (pin 4) and main counter division signal to the data terminal (pin 3).

The method of inputting to a divider has two kinds: mode 1 and mode 2.

- Mode 1. This is the method of inputting from the RF input terminal (pin 15) by setting the lock terminal (pin 20) to high level.

 The lock condition in normal use operation can be inspected using this method.
- Mode 2. This is the method of directly inputting to a 1/32 and 1/33 divider from the test 2 terminal (pin 19) without passing through a 1/8 prescaler by setting the lock

The input level should be indicated in the diagram 3.

(2) Mode 3

In mode 3, a prescaler, phase comparator, and charge pump will be tested. If both test 1 terminal (pin 1) and enable terminal (pin 2) are set to high level, these will be mode 3. The clock terminal (pin 4) is a comparison reference frequency signal input of phase comparator, the data terminal (pin 3) is a compared frequency signal input, and the lock terminal (pin 20) is a prescaler output (the fixed dividing ratio of 1/256).

The output polarity of phase comparator is as follows:

terminal (pin 20) to low level.

INPUT FREQUENCY	CHARGE PUMP OUTPUT PIN (PIN 9)
Input frequency>Programmed frequency	High level
Input frequency < Programmed frequency	Low level

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TEST MODE

PIN NAME	NORMAL	MODE 1	MODE 2	MODE 3
Test 1 (Pin 1)	L	Н	Н	Н
Enable (Pin 2)	Enable	L	L	Н
Lock (Pin 20)	Lock	H (Pin 15 input)	L (Pin 19 input)	1 / 256 output (Pin 15 input)
Clock (Pin 4)	Clock input	Comparison reference signal output (6.25kHz)	Comparison reference signal output (6.25kHz)	P.D. Reference signal input
Data (Pin 3)	Data input	Main counter output	Main counter output	P.D. Comparison signal input
Test 2 (Pin 19)	Inhibit	Inhibit	Divider input	Inhibit
RF Input (Pin 15)	RF input	RF input	Inhibit	RF input

THE METHOD OF INPUTTING DATA

The method of inputting data will be indicated in the diagram 1.

LOCK FREQUENCY CALCULATION METHOD

The lock frequency can be calculated in the following formula :

 $f_{OSC} = f_r \times 8 \times (32M + S)$

 f_{OSC} : The oscillation frequency of V_{CO} (the input frequency of prescaler); $51.2MHz \le f_{OSC}$ X'tal = 3.2MHz

 f_r : Reference frequency; it will be 1/512 of oscillation frequency of a crystal oscillator. When a 3.2MHz crystal oscillator is used, this will be f_r =6.25kHz and the lock frequency step will be 50kHz.

M : Preset value of Main counter ; The 10 bits between MSB to MSB-9. Input $32 \le M \le 1023$ value in binary.

S : Preset value of Swallow counter ; The 5 bits between MSB-10 to LSB. Input $0 \le S \le 31$ value in binary.

For example, when $f_{OSC} = 801MHz$ is received at the reference frequency of 6.25kHz,

 $801 \times 10^3 = 6.25 \times 8 \times (32M + S)$

32M + S = 16020

 $M = 500_{(10)} = 0111110100_{(2)}$

 $S = 20_{(10)} = 10100_{(2)}$

Further, if the band "4" is used, the received data will be as follows :

$\underline{1000}0111110100\underline{10100}$

BAND MAIN COUNTER SWALLOW COUNTER

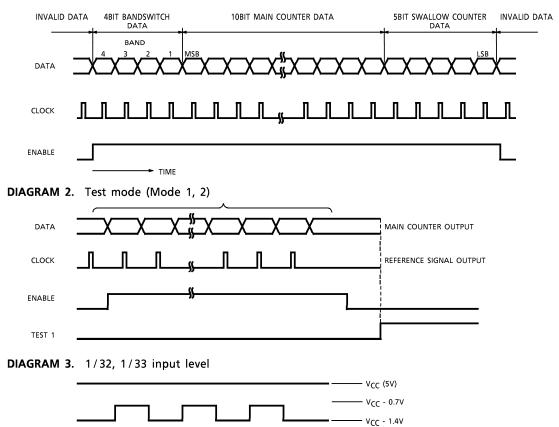
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DIAGRAM 1. Normal use



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	Vcc	6.5	V
ECL Input Voltage	V _{in1}	2.0	V _{p-p}
Logic Input Voltage	V _{in2}	-0.3~V _{CC}	V
Power Dissipation	PD	(Note 1)	W
Operating Temperature	T _{opr}	<i>–</i> 20∼75	°C
Storage Temperature	T _{stg}	- 55∼150	°C

(Note 1) P-type: 1.4W, N-type: 1.7W

(Note 2) When using the device at above $Ta = 25^{\circ}C$, decrease the power dissipation by 11.2mW for P-type and 9.5mW for N-type for each increase of 1°C.

(Note 3) Handle with care as this product is weak at surge voltage.

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RECOMMENDED SUPPLY VOLTAGE

PIN No.	PIN NAME	MIN.	TYP.	MAX.	UNIT
5	ECL V _C C	4.5	5	5.5	٧
18	I ² L V _{CC}	4.5	5	5.5	٧

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C)

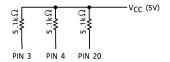
			-					
CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply	(ECL)	l _{CC1}	2		40	60	80	- A
Current	(I ² L)	^I CC2	2		15	25	35	mA
Bandswitch Max. Voltage		V _B MAX.	_	Band 1~4	12	_	15	V
Bandswitch Inflow Current		I _B MAX.	_	V _{CC} = 5V	0.7	_	2.2	mA
DC Voltage		V ₁₅	_	_	1.7	2.0	2.3	V
		V ₁₇	_	_	1.7	2.0	2.3	1 '
DC Current High Level		lΗ	_	V _{in} = 5V (Note 1)	_	180	300	μΑ
Input	"H" Level	V _{IH}	_	(Note 1)	3.0	_	_	V
Voltage	"L" Level	v_{IL}	_	(Note 1)	_	_	0.8	
Output	"H" Level	Voн	1	(Note 2)	3.8	_	_	\ \
Voltage	"L" Level	v_{OL}	1	(Note 2)	_	_	0.5	
N/F Leak Current		IL	_	(Note 3)	- 0.2	_	0.2	μΑ
RF Input Sensitivity		V_{in1}	3	f _{in} = 80-100MHz	- 24	-	3	dBmW
		V_{in2}	3	f _{in} = 100-1000MHz	- 27	_	3	(50 Ω)
Setup Time		T_{S}	_		2	_	_	
Enable Hold Time		T_{SL}	_		2	_	<u> </u>	
Enable Inhibit Time		T _{NE}	_		6	_	_	
Clock Inhibit Time		T _{NC}	_	Data timing chart	6	_	-	μ s
Clock Width		T _C	_		2	_	_] [
Enable Setup Time		ΤL	_		10	_	_	
Data Hold Time		Τ _Η	_		2	_	_	

(Note 1) TEST 1, Enable, Clock, Lock : applied to input mode.

(Note 2) Data, Clock, Lock : applied to output mode.

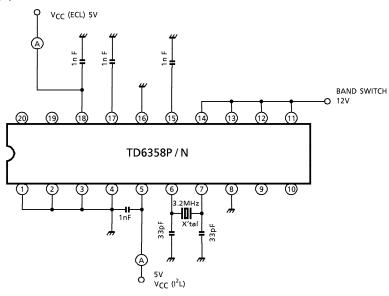
(Note 3) Pin 10: 2.1V, Pin 9: Open

TEST CIRCUIT 1. Test mode



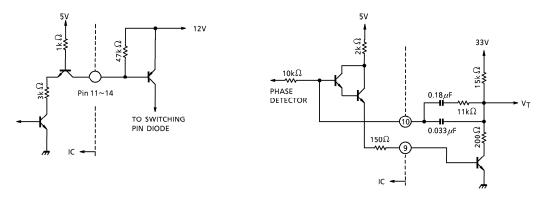
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TEST CIRCUIT 2. Supply test circuit



Bandswitch output circuit

Phase detection output circuit

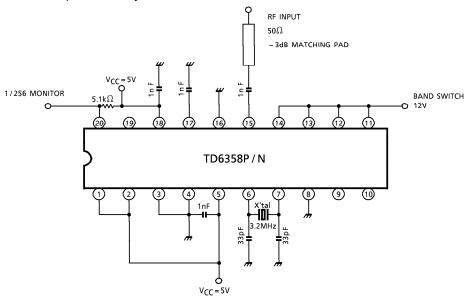


The output polarity of phase detector is as follows:

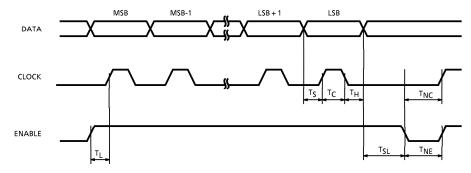
INPUT FREQUENCY	P.D. OUTPUT (PIN 9)
Input frequency>Programmed frequency	High level
Input frequency <programmed frequency<="" td=""><td>Low level</td></programmed>	Low level

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TEST CIRCUIT 3. Input sensitivity test circuit

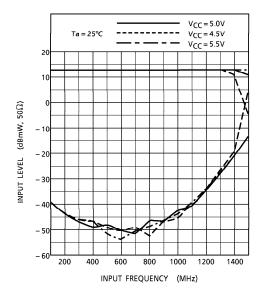


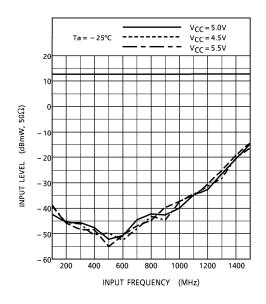
DATA TIMING CHART (Rising timing)

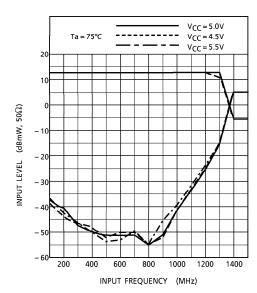


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RF AGC 4-BAND TV / CATV TUNER AFT 12KV Ω002 5 0 GND 0.001 µF 16 0.001 F TEST 1 TEST 2 BANDSWITCH LOCAL INPUT TD6358P/N REFERENCE --- 20 LOCK OUTPUT VCC VCC I²L ECL 10 µF > DATA 5.1kΩ z HMS. ε PIN PROTECTION DEPENDS ON THE MICROCOMPUTER APPLICATION NO K νCPU

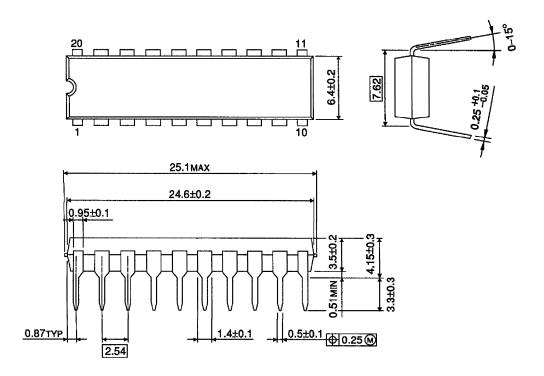
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OUTLINE DRAWING DIP20-P-300-2.54A

Unit: mm



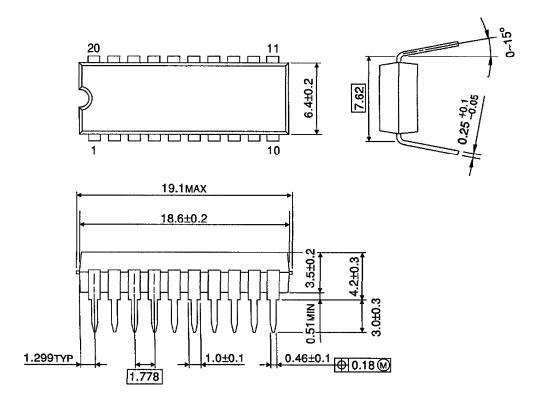
Weight: 2.25g (Typ.)

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OUTLINE DRAWING SDIP20-P-300-1.78

Unit: mm



Weight: 1.02g (Typ.)

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