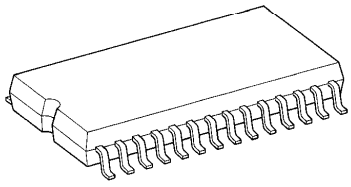
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9245F, TC9245N

RECEIVING DEMODULATION IC FOR DIGITAL AUDIO INTERFACE

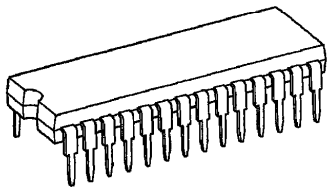
TC9245F, TC9245N are a receiving demodulation IC for digital audio interface developed in accordance with EIAJ "CP-340 Standard".

TC9245F



SOP28-P-450-1.27

TC9245N



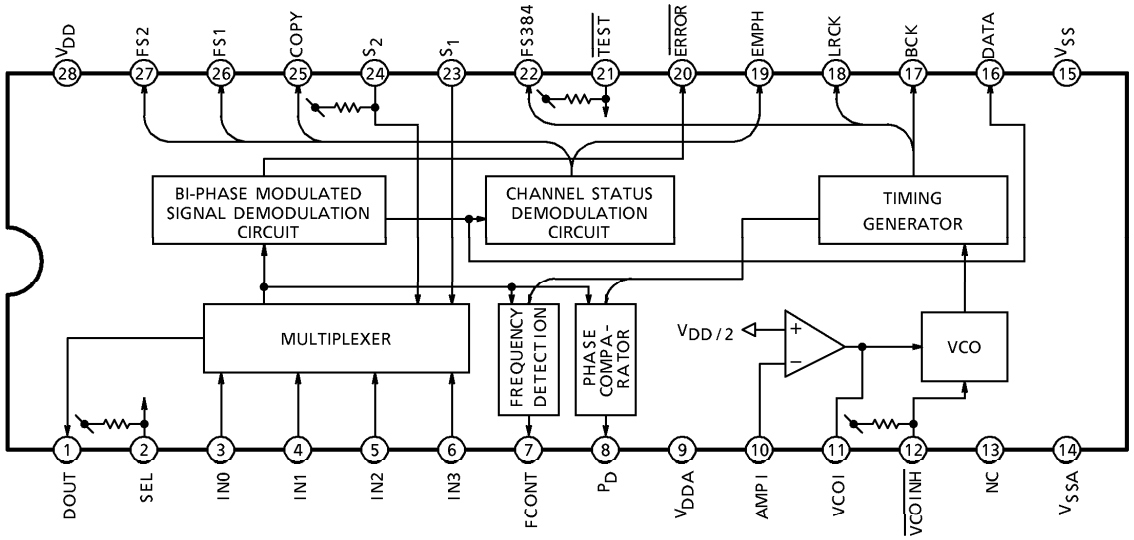
SDIP28-P-400-1.78

Weight
SOP28-P-450-1.27 : 0.8g (Typ.)
SDIP28-P-400-1.78 : 2.2g (Typ.)

FEATURES

- Compatible with SCMS (Serial Copy Management System).
- Compatible with 4 inputs including both coaxial and optical inputs.
- Performs 2 kinds of error detection, i.e., synchronizing signal detection and parity check.
  If an error is detected, output data is muted for a fixed time.
- PLL circuit can be easily constructed by built-in VCO.
- Built-in pseudo-locking preventive function assures positive locking.
- With VCO oscillation stop function.
- CMOS silicon gate construction with low power dissipation.
- 2 kinds of package, 28pin flat package and 28pin DIP shrunk package.

BLOCK DIAGRAM



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PIN FUNCTION

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION				REMARKS
		I/O	PARALLEL MODE	I/O	SERIAL MODE	
1	DOUT	O	IN0~IN2 selecting output terminal. When selecting IN3, output is fixed at "L".			With a pull-down resistor + switch.
2	SEL	I	Microcomputer interface mode selecting input terminal. Compatible with the parallel mode when this terminal is at "H" level or open and the serial mode at "L" level.			With a pull-up resistor.
3	IN0	I	Digital audio data input terminal.			With a pull-down resistor + switch.
4	IN1					
5	IN2					
6	IN3					
7	FCONT	O	PLL mis-lock detection signal output terminal.			3-state output.
8	P_D	O	Phase comparator phase error signal output terminal.			3-state output.
9	V_{DDA}	—	Analog supply voltage terminal.			—
10	AMPI	I	LPF operational amplifier input terminal.			—
11	VCOI	O	Operation amplifier output terminal. (VCO oscillation control voltage output)			—
12	$\overline{\text{VCOINH}}$	I	VCO oscillation stop control input terminal.			—
13	NC	—	Non connection terminal.			—
14	V_{SSA}	—	Analog ground terminal.			—
15	V_{SS}	—	Digital ground terminal.			—
16	DATA	O	Digital audio data output terminal.			—
17	BCK	O	Bit clock output terminal. (32fs)			—
18	LRCK	O	LR clock output terminal. L/R-ch polarity fixed.	O	LR clock output terminal. L/R-ch polarity variable.	—
19	EMPH	O	Emphasis output terminal. Emphasis is available at "H".			—
20	$\overline{\text{ERROR}}$	O	Error detection flag output terminal. Error is detected at "L".			—
21	$\overline{\text{TEST}}$	I	Test terminal.			With a pull-up resistor.
22	FS384	O	384fs clock output terminal.			
23	S_1	I	Input selecting terminal.	O	192fs or 128fs clock output terminal.	—
24	S_2	I	Input selecting terminal.	I	Microcomputer data input/output mode selecting terminal.	With a pull-up resistor.
25	COPY	O	Copy inhibit flag output terminal. Copy is inhibited at "L".	I/O	Microcomputer data input/output terminal.	With a pull-up resistor. Open drain output.
26	FS1	O	Sampling frequency bit decoding output terminal.	I	Microcomputer data latch pulse input terminal.	
27	FS2	O		I	Microcomputer data transfer clock input terminal.	
28	V_{DD}	—	Digital power supply voltage terminal.			—

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DESCRIPTION OF OUTLINE

1. Mode setting

The communication modes are set by setting the SEL terminal at "L" or "H" level.
The parallel communication mode is set statically and the serial communication mode is set by inputting 3 signals of serial data, transfer clock and latch pulse as shown in Fig.1.

Table.1 Terminal name change table

PIN NAME		I/O	FUNCTION IN SERIAL COMMUNICATION MODE
PARALLEL	SERIAL		
S_1	CKOUT	O	192fs or 128fs clock is output.
S_2	$\overline{I/O}$	I	The output mode when the microcomputer I/O mode selecting terminal is at "H" level and the input mode at "L" level.
FS1	$\overline{LP}$	I	$\overline{I/O}$ = H : Data output trigger signal input. $\overline{I/O}$ = L : Data latch pulse input.
FS2	$\overline{SCK}$	I	Data transfer clock input.
COPY	μDATA	I/O	$\overline{I/O}$ = H : Channel status output. $\overline{I/O}$ = L : Internally set serial data input.

(a) Parallel communication mode : (SEL = H)

In this mode, sampling frequency is decoded and output by 2 bits of FS1 and FS2 and input data (internally taken in) and DOUT output data by S_1 and S_2 as shown in the following table :

Table.2 Sampling frequency encode table

FS2	FS1	SAMPLING FREQUENCY
L	L	44.1kHz
L	H	—
H	L	48kHz
H	H	32kHz

Table.3 Input/Output setting table

S_2	S_1	INTERNAL PROCESS	DOUT PIN
L	L	IN0	IN0
L	H	IN1	IN1
H	L	IN2	IN2
H	H	IN3	"L" fix

(b) Serial communication mode : (SEL = L)

In this mode, S_1 and S_2 are input in the data input mode and channel status signals shown in Table 5 are output to the outside in the data output mode.
The data input and output modes are briefly explained hereinafter.

- Data input mode : ($\overline{I/O}$ = L)

  In this mode, 4 bits of S_1, S_2, LRS and 192s can be input.
  Each of these bits is taken in the IC at the trailing edge of $\overline{SCK}$ and the internal mode is updated at the trailing edge of $\overline{LP}$.

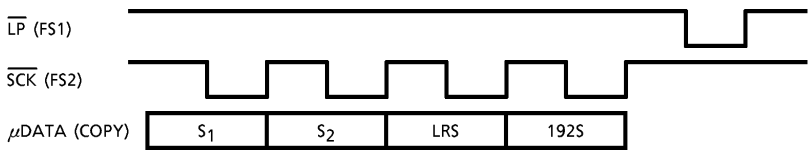


Fig.1 Serial data input timing

Table.4 Internal setting by serial data

SERIAL DATA	FUNCTION DESCRIPTION
S_1, S_2	The same operation as S_1 and S_2 terminal in the parallel setting mode.
LRS	Changes phase of LRCK. L : The same as the parallel mode. H : Inverse output.
192S	"H" : 192fs clock is output through the CKOUT terminal. "L" : 128fs clock is output.

- Data output mode : ($\overline{I/O}$ = H)

  In this mode, the channel status bits shown in Table.5 can be monitored.
  Each channel status bit is output as serial data.
  The serial data output timing is shown in Fig.2.

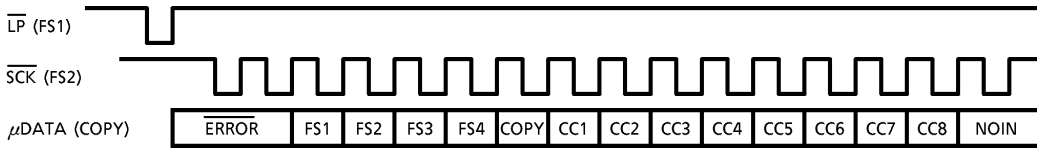


Fig.2 Serial data output timing

Table.5 Contents of serial data output

SYMBOL	CONTENTS
$\overline{ERROR}$	Error detection result
COPY	Copy flag
CC1~8	Category bit
FS1~4	Sampling frequency bit
NOIN	No signal detected at selected input terminal

(Note 1) In order to cope with SCMS, sampling frequency bits are not decoded.

Further, in the actual serial data output, parity (even parity from the top bit $\overline{ERROR}$) is output for every data bit as shown in Fig.3.

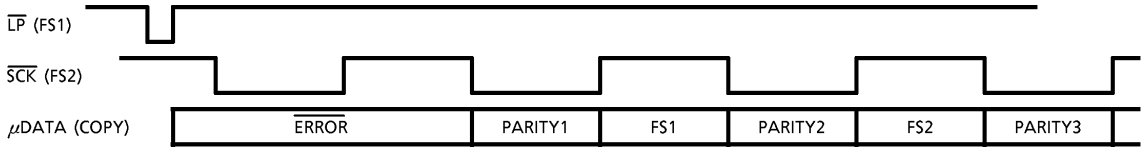


Fig.3 Parity output timing of serial data output mode

2. Detection of error

If an error is detected, the $\overline{\text{ERROR}}$ terminal is set at "L" level and output data is muted. In addition, the channel status latch operation is inhibited and a preceding value is held. If the no error status continues for times shown in the following table, the $\overline{\text{ERROR}}$ terminal is set at "H" level, returning to the normal operation.

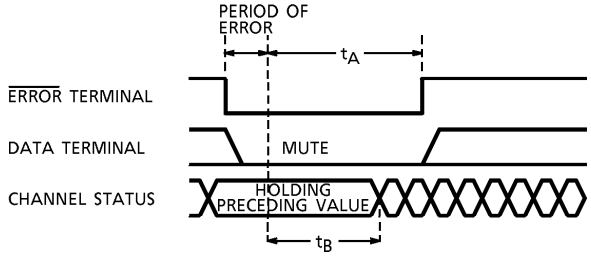


Fig.4 Internal operation timing at error

Table.6 Error detecting operation releasing time

SAMPLING FREQUENCY (kHz)	$\overline{\text{ERROR}}$, DATA TERMINAL t_A (ms)	CHANNEL STATUS t_B (ms)
32	384.0	288.0
44.1	278.6	209.0
48	256.0	192.0

3. Detection of no input

Detecting existence of IN0~3 input signals, oscillation of VCO is automatically suppressed to low if no edge is detected for a fixed time.

Table.7 No input judging time of input data

SAMPLING FREQUENCY (kHz)	TIME FROM LAST EDGE (ms)
32	approx. 1000
44.1	approx. 750
48	approx. 700

4. Detection of mis-lock

Detecting mis-lock by comparing input signal with oscillation frequency, outputs a signal to escape from the mis-lock through the FCONT terminal.

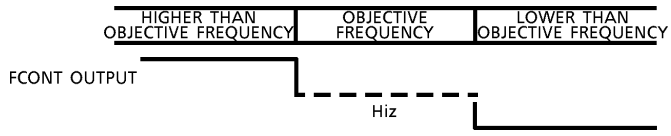


Fig.5 Mis-lock detection timing

5. Digital data input terminal

The configuration of IN0~3 input multiplexer is shown in Fig.6.
Considering crosstalk to other terminals, an unused terminal can be pulled down by resistors through ON / OFF of the internal switch.

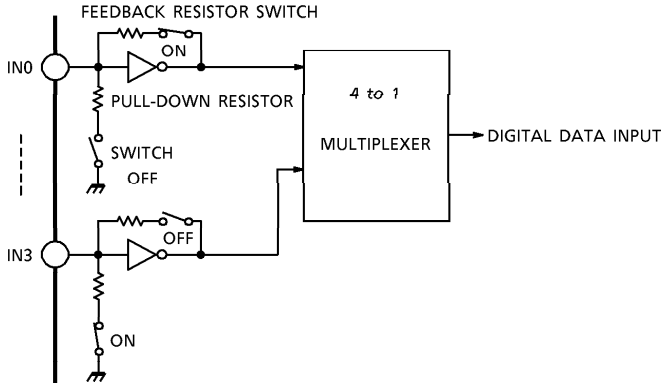


Fig.6 Configuration of input multiplexer

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	−0.3~6.0	V
Input Voltage		V_{IN}	−0.3~V_{DD} + 0.3	V
Power Dissipation	TC9245F	P_D	600	mW
	TC9245N		800	
Operating Temperature		T_{opr}	−25~75	°C
Storage Temperature		T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{DD} = 5V)

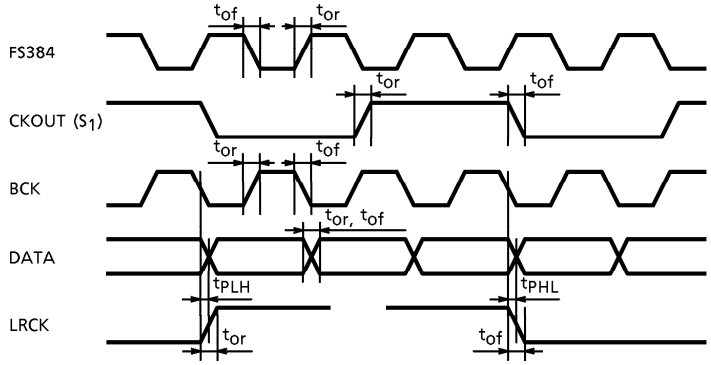
DC characteristics

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		V_{DD}	—	Ta = – 25~75°C		4.75	5.00	5.25	V
Operating Supply Current		I_{DD}	—	—		—	15.0	25.0	mA
Input Voltage	"H" Level	V_{IH}	—	$\overline{VCOINH}$, $\overline{TEST}$, S_1, S_2, SEL, COPY, FS1, FS2, IN0~3		4.0	—	V_{DD}	V
	"L" Level	V_{IL}	—			0.0	—	1.0	
Input Amplitude		V_{IN}	—	IN0~3		0.4	—	5.0	V_{p-p}
Input Current (1)	"H" Level	I_{IH} (1)	—	S_1, AMPI	V_{IH} = 5.0V	—	—	1.0	μA
	"L" Level	I_{IL} (1)	—		V_{IL} = 0.0V	– 1.0	—	—	
Input Current (2)	"H" Level	I_{IH} (2)	—	IN0~3	V_{IH} = 5.0V	—	10	—	
	"L" Level	I_{IL} (2)	—		V_{IL} = 0.0V	—	– 10	—	
Trystate Leak Current	"H" Level	I_{TLH}	—	FCONT, P_D	V_{IH} = 5.0V	—	—	1.0	
	"L" Level	I_{TLL}	—		V_{IL} = 0.0V	– 1.0	—	—	
Output Current (1)	"H" Level	I_{OH} (1)	—	EMPH, $\overline{ERROR}$	V_{OH} = 4.5V	—	—	– 1.0	mA
	"L" Level	I_{OL} (1)	—		V_{OL} = 0.5V	2.0	—	—	
Output Current (2)	"H" Level	I_{OH} (2)	—	DATA, BCK, LRCK, FS384, DOUT	V_{OH} = 4.5V	—	—	– 2.0	
	"L" Level	I_{OL} (2)	—		V_{OL} = 0.5V	4.0	—	—	
Output Current (3)	"H" Level	I_{OH} (3)	—	S_1, FCONT, P_D	V_{OH} = 4.5V	—	—	– 4.0	
	"L" Level	I_{OL} (3)	—	S_1, FCONT, P_D, COPY, FS1, FS2	V_{OL} = 0.5V	8.0	—	—	
Pull-up Resistor		R_{UP}	—	$\overline{VCOINH}$, $\overline{TEST}$, S_2, SEL, COPY, FS1, FS2		—	20	—	kΩ
Pull-down Resistor		R_{DOWN}	—	IN0~3, DOUT		—	1	—	

AC characteristics

(1) Clock system and data output system timing

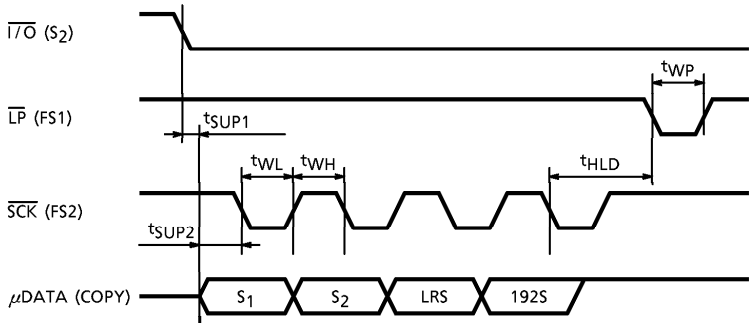
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	—	FS384, BCK, LRCK, DATA CKOUT (S_1)	—	—	15	ns
Output Fall Time		t_{of}	—		—	—	15	
Delay Time	"H" Level	t_{PHL}	—	BCK→DATA, LRCK	—	—	25	ns
	"L" Level	t_{PLH}	—		—	—	25	



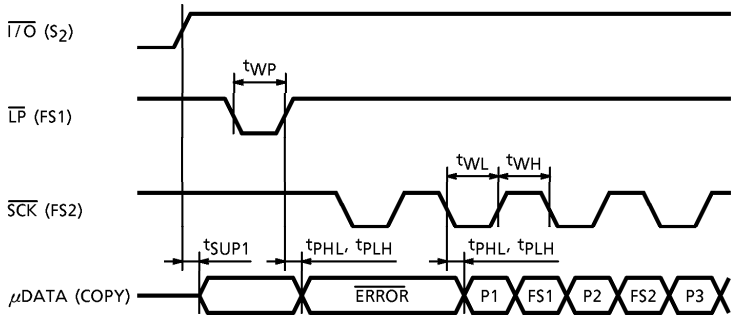
(2) Microcomputer interface system timing (SEL = L : Serial communication mode)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer Time	"H" Level	t_{PHL}	—	$\overline{SCK}\rightarrow\mu DATA$	—	—	1	μs
	"L" Level	t_{PLH}	—	$\overline{LP}\rightarrow\mu DATA$	—	—	0.2	
Strobe Pulse Width		t_{WP}	—	$\overline{LP}$	0.5	—	—	μs
Clock Pulse Width	"H" Level	t_{WH}	—	$\overline{SCK}$	1	—	—	μs
	"L" Level	t_{WL}	—		1	—	—	
Setup Time		t_{SUP1}	—	$\overline{I/O}\rightarrow\mu DATA$	0.2	—	—	μs
		t_{SUP2}		$\mu DATA\rightarrow\overline{SCK}$	0.5	—	—	
Hold Time		t_{HLD}	—	$\overline{SCK}\rightarrow\overline{LP}$	0.5	—	—	μs

- Data input mode ($\overline{I/O}$ = L) :

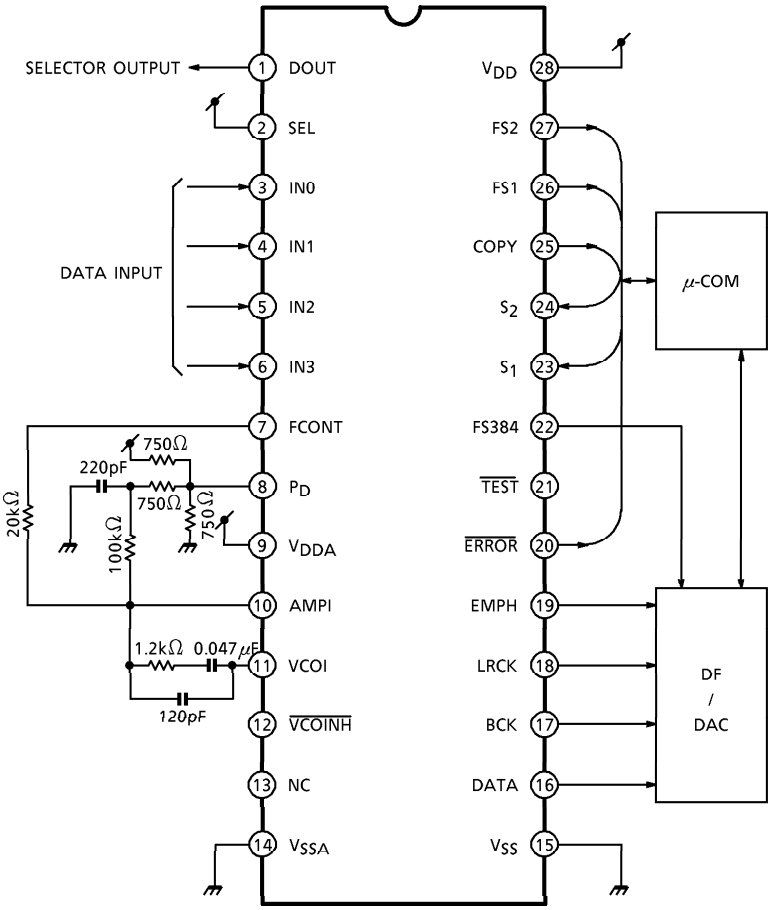


- Data output mode ($\overline{I/O}$ = H) :

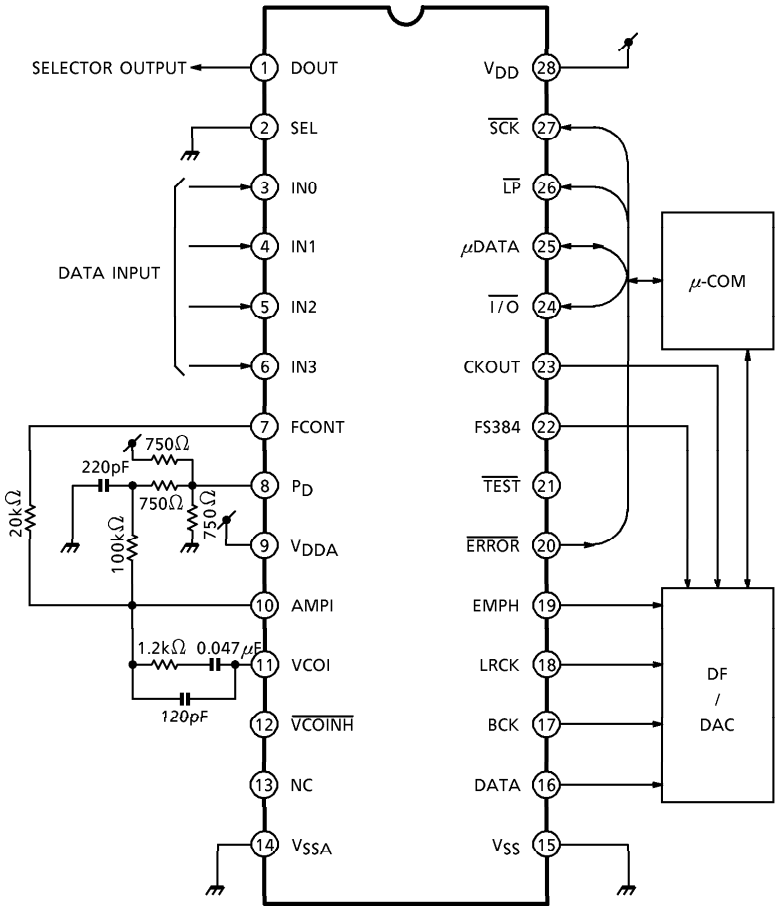


APPLICATION CIRCUIT

1. Parallel setting mode



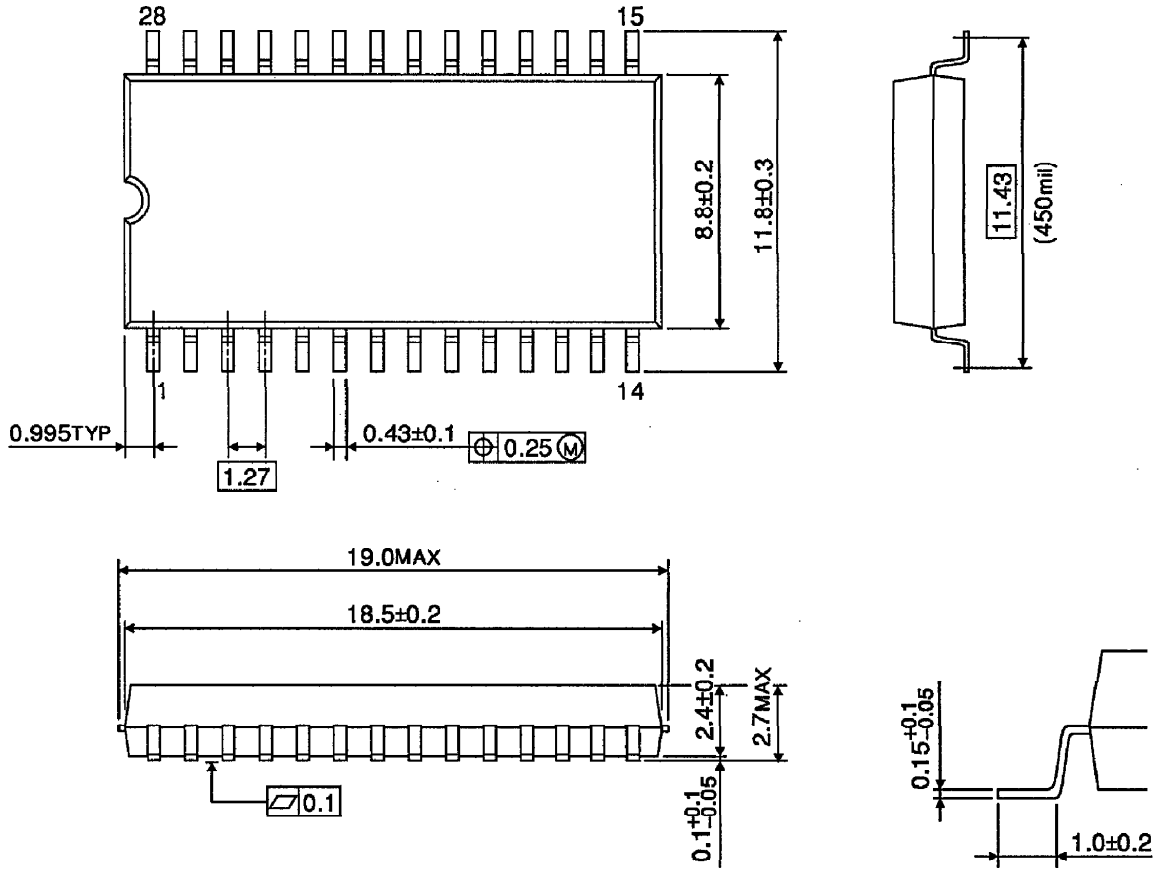
2. Serial communication mode



OUTLINE DRAWING

SOP28-P-450-1.27

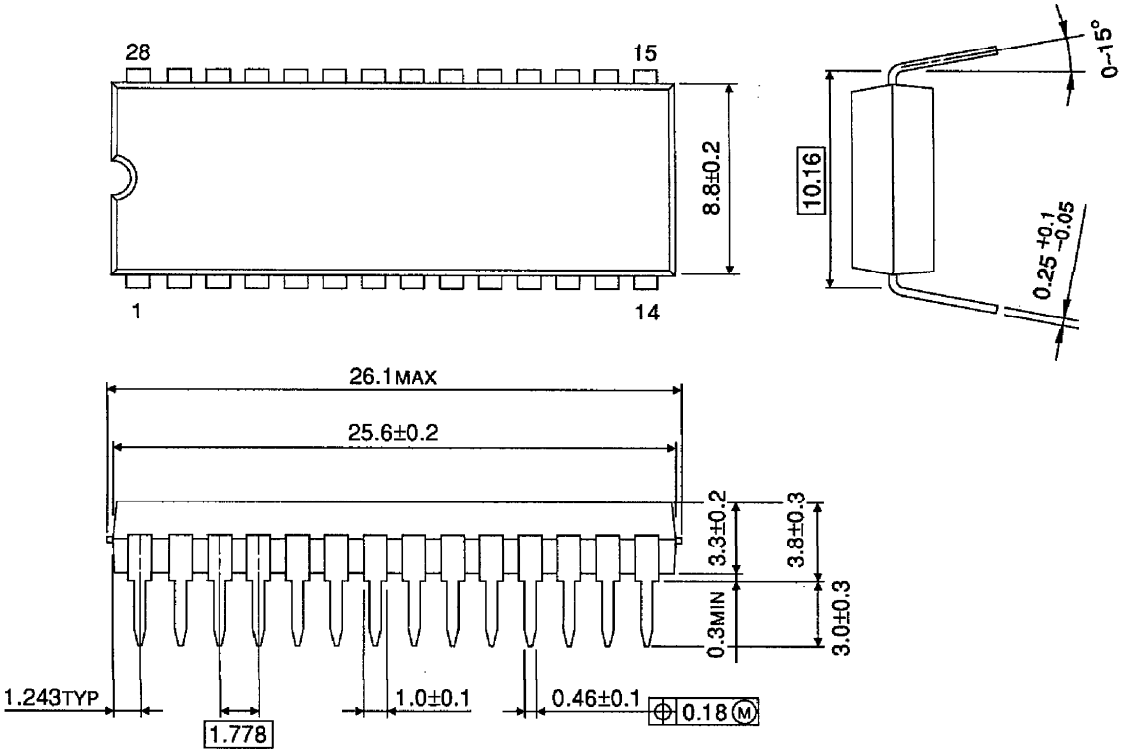
Unit : mm



Weight : 0.8g (Typ.)

OUTLINE DRAWING

SDIP28-P-400-1.78 Unit : mm



Weight : 2.2g (Typ.)