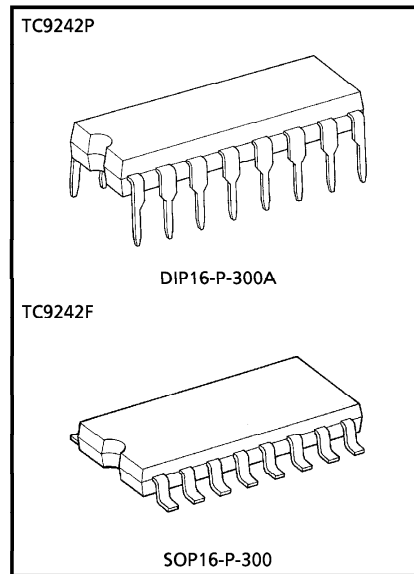


QUARTZ PLL MOTOR CONTROL

The TC9242P, TC9242F are CMOS LSIs developed for controlling the motor speed.
Since an 8bit D/A converter system has been employed for each of the speed control system (AFC) and the phase control system (APC).
Offers improved linearity.
With frequency division ratios of 1/3, 1/4 and 1/5 the standard divider is ideal for laser scanner motors.

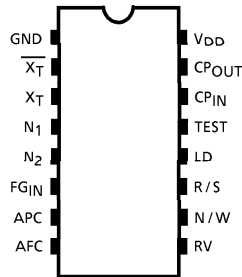
FEATURES

- Crystal can be used up to 20MHz, and crystal reference dividing frequency is selectable from three positions of 1/3, 1/4 and 1/5.
- Lock range can be selected from two positions of 1/20 and 1/27.
- External oscillator makes possible fine adjustment of speed.
- Lock detection output and reverse rotation signal output are provided.
- Package is DIP16PIN and SOP16PIN.



Weight DIP16-P-300A : 1.00g (Typ.)
SOP16-P-300 : 0.16g (Typ.)

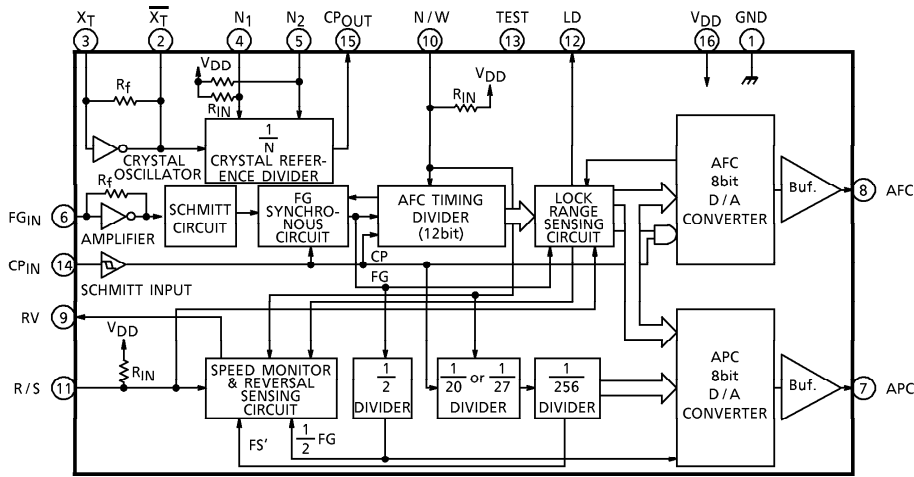
PIN CONNECTIONS (TOP VIEW)



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BLOCK DIAGRAM



FUNCTIONAL EXPLANATION OF EACH TERMINAL

PIN No.	SYMBOL	PIN NAME	FUNCTIONAL & OPERATION EXPLANATION	REMARKS
16	V _{DD}	Power Terminal	V _{DD} = 5V ± 0.5V is applied.	—
1	GND	Ground Terminal	Ground	—
2	X _T ⁻	Crystal Oscillation Terminal	Crystal oscillator is connected.	With a built-in feedback resistor.
3	X _T			
4	N ₁	Reference Divided Frequency Switching Terminal	Switching of divided frequency from the crystal reference frequency divider into 1/3, 1/4 and 1/5 is possible.	With a built-in pull-up resistor.
5	N ₂			
6	FG _{IN}	FG Pulse Input Terminal	Input terminal for pulse showing motor speed.	With a built-in amplifier.
7	APC	APC Output Terminal	Output terminal for motor phase control system. Output of 8bit D/A converter.	With a built-in buffer.
8	AFC	AFC Output Terminal	Output terminal for motor speed control system. Output of 8bit D/A converter.	With a built-in buffer.
9	RV	Reverse Signal Output Terminal	Terminal for motor reverse signal output.	CMOS OUTPUT
10	N/W	Lock range Switching Terminal	Terminal for switching motor speed. L = 1/27, H or NC = 1/20.	With a built-in pull-up resistor.
11	R/S	RUN/STOP Input Terminal	Motor RUN/STOP signal input terminal L = RUN, H or NC = STOP	With a built-in pull-up resistor.
12	LD	Lock Detecting Terminal	This terminal becomes "H" when the motor speed is within the lock range and otherwise "L".	CMOS OUTPUT
14	CP _{IN}	Reference Frequency Input Terminal	Normally connected to CPOUT. For external fine adjustment input from an external oscillator.	CMOS SCHMITT INPUT
15	CP _{OUT}	Reference Frequency Output Terminal	Terminal for divided output from the crystal reference frequency divider. Normally connected to CP _{IN} .	CMOS OUTPUT
13	TEST	Output Terminal for INTERNAL TEST	Output terminal for INTERNAL TEST. Generally open.	—

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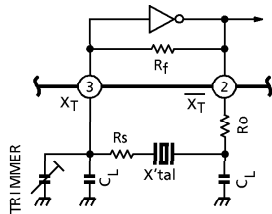
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EXPLANATION OF OPERATION

1. Crystal Oscillation Terminals (X_T , $\overline{X_T}$)

- The crystal oscillator is used by connecting as shown below.



※ CL of 10~30pF is appropriate.

- Crystal oscillation frequency is calculated by the following equation according to number of FG pulses of a motor to be used.

$$f_X = \frac{R}{60} \times FG' \times 128 \times (20 \text{ or } 27) \times N \text{ (Hz)}$$

Note : (20 or 27) : 20 at N/W = "H" or NC
27 at N/W = "L"

Further, fX : Crystal oscillation frequency, FG' : No. of FG pulses generated per revolution of motor.

N : Ratio of frequency division of the crystal reference frequency divider.
N = 3, 4, 5 (Refer to Item 9.)

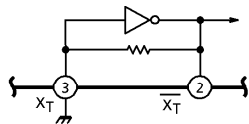
- Maximum operating frequency is above 20MHz and crystals up to 20MHz can be used.
- If necessary, adjust R_o, R_s and C_L to control noise from the crystal oscillator circuit or to control overtone oscillation.

<Reference values>

f _{X_T} (MHz)	R _o (Ω)	R _s (Ω)	C _L (pF)
20	—	220	22
12	—	220	27
8	—	220	30
4.5	2.2k	—	30
1.5	4.7k	—	30

Note : The values in the table are the reference values. Determine the values suitable for the characteristics of the crystal used.

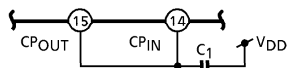
Note : When not using the crystal oscillator circuit, always connect pin 3 (X_T) to GND as shown in the diagram to overcome the effects of noise and to reduce current consumption.



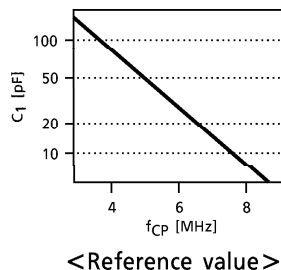
<When not using the crystal oscillator circuit>

2. Reference Frequency Input/Output Terminals (CP_{OUT}, CP_{IN})

- Divided output $\frac{f_x}{N}$ from the crystal reference frequency divider is available at CP_{OUT}, which is normally connected to CP_{IN}.
- When an external oscillator (CR oscillator, etc.) is connected to CP_{IN}, motor speed can be finally adjusted.
- If the effects of noise from CP_{IN} input signal overshoot must be controlled, connect capacitor C1 as in the following diagram.

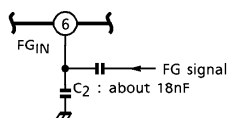


Note : When connecting capacitor C1, make sure that the input level of pin 14 (CP_{IN}) does not fall below the standard ($V_{IH} \geq 0.8 \times V_{DD}$, $V_L \leq 0.2 \times V_{DD}$)



3. FG Pulse Input Terminal (FG_{IN})

- This is the input terminal of FG pulse that shows the motor speed. This FG pulse becomes comparison frequency.
- This terminal has built-in Amplifier and Schmitt circuit. FG pulses are applied through capacitor coupling and small amplitude is enough for proper operation.
- If there is noise in the FG signal, connect capacitor C2 as shown in the diagram to control the noise.



Note : Determine the values of capacitors C1 and C2 after checking their characteristics with f_{CP} and f_{FG} used.

Note : When connecting capacitor C2, make sure that the input level of pin 6 (FG_{IN}) does not fall below the standard ($V_{inFG} \geq 0.5V_{p-p}$)

4. Lock Range Switching Terminal (N/W)

This terminal is for switching the Lock range with a pull-up resistor and chattering preventive circuit.

(TRUTH TABLE)

N / W	DIVIDED FREQUENCY	LOCK RANGE
L	$\frac{1}{27}$	+ 3.4~ - 3.9% of reference cycle
H or NC	$\frac{1}{20}$	+ 4.6~ - 5.3% of reference cycle

CAUTION reference frequency $FS = f_x / N \times (20 \text{ or } 27) \times 128 \text{ (Hz)}$, $FS' = \frac{FS}{2}$

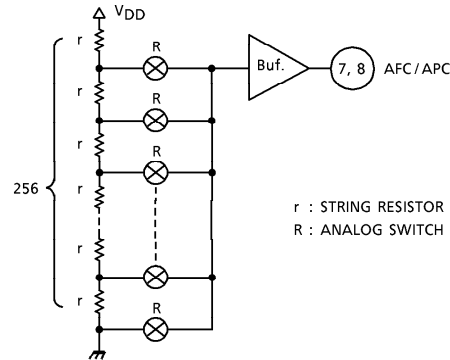
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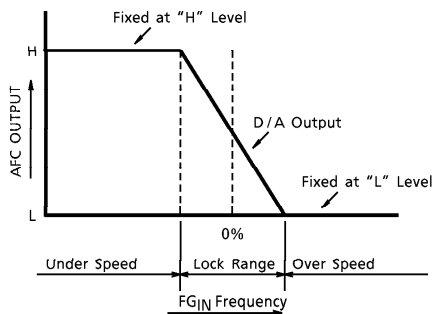
5. APC, AFC Output Terminal (APC, AFC)

- AFC (speed control output) is a F-V converter for FG frequency and is consisting of a 8bit D/A converter.
- APC (phase control output) is a phase comparator (ϕ -V converter) that compares phase difference ϕ between 1/2 FG and reference frequency FS' , and is also consisting of a 8bit D/A converter.

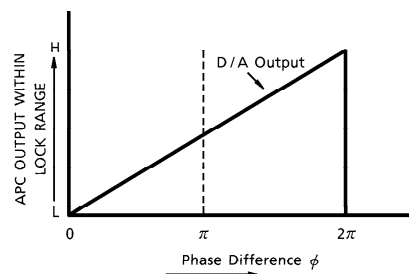


- Both APC and AFC perform the following 3 operations according to FG_{IN} frequency.
 - When FG_{IN} frequency is within the lock range:
Both APC and AFC perform the normal operation for FG_{IN} .
 - When FG_{IN} frequency is below the lock range (under speed):
APC and AFC outputs are both fixed at "H" level.
 - When FG_{IN} frequency is above the lock range (over speed):
APC and AFC outputs are both fixed at "L" level.
- When a motor is in STOP state ($P/S = H$ or NC), both AFC and APC are fixed "L" level.

AFC output change status for FG_{IN} frequency

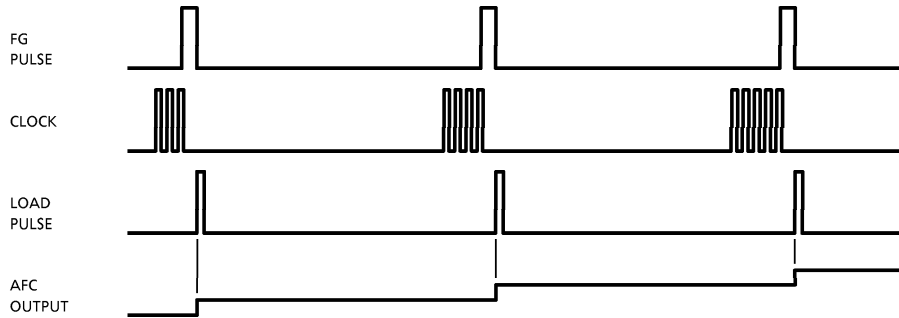


APC output change status for phase difference ϕ

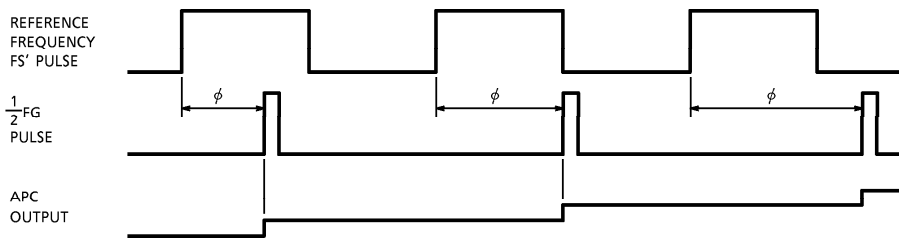


- AFC and APC timing chart within lock range.

a. AFC (SPEED CONTROL SYSTEM)



b. APC (PHASE CONTROL SYSTEM)



AFC OUTPUT with in Lock Range

6. Lock Detecting Terminal (LD)

- This terminal is the lock detecting output and is placed at "H" level when FG_{IN} frequency is within the lock range and otherwise, placed at "L" level.

7. RUN/STOP Input Terminal (R/S)

- RUN/STOP signals of the motor are input to this terminal.
PLAY=L, STOP=H or NC.
- This terminal has a pull-up resistor and a chattering preventive circuit.
- During RUN (R/S=L), AFC, APC and LD perform the above-mentioned operations for FG_{IN} frequency, and during STOP (R/S=H or NC), AFC, APC and LD are all fixed at "L" level.

8. Reverse Signal Output Terminal (RV)

- Reverse signal for braking the motor at time of switching of Lock range from 1/20 to 1/27 or the operation from RUN to STOP is output through this terminal.
- Change of RV output status

PREVIOUS STATUS	RV OUTPUT CHANGE TO "H" LEVEL	RV OUTPUT CHANGE TO "L" LEVEL
During Normal Rotation (During Lock) at 1/20	When the Lock range is switched from 1/20 to 1/27.	When the Lock range is locked at 1/27, or When $FG_{IN} \leq 1/8FS$, or when the Lock range is switched from 1/27 to 1/20.
During Normal Rotation (During Lock) at 1/20 or 1/27	When the operation is switched from RUN to STOP.	When $FG_{IN} \leq 1/8FS$ or when the operation is switched from STOP to RUN.

- In other cases than above, RV output is not changed and fixed at "L" level.
- Further, if FG frequency rises up to 1.5 times of normal rotation at 1/20 (2 times of normal rotation at 1/27), RV output is reset.

9. Reference Divided Frequency Switching Terminal (N₁, N₂)

- Divided frequency 1/N of the crystal reference frequency divider can be switched to 1/5, 1/4 or 1/3 by number of FG pulses or a crystal used.
- This terminal has a built-in pull-up resistor.

(TRUTH TABLE)

N1	N2	1/N
H	H	1/5
L	H	1/4
H	L	1/3

1/N : Crystal reference divided frequency

Note : Do not use N1=N2=L, which is used for internal test only.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	-0.3~7.0	V
Input Voltage	V _{IN}	-0.3~V _{DD} + 0.3	V
Power Dissipation	P _D	300	mW
Operating Temperature	T _{opr}	-40~85	°C
Storage Temperature	T _{stg}	-65~150	°C

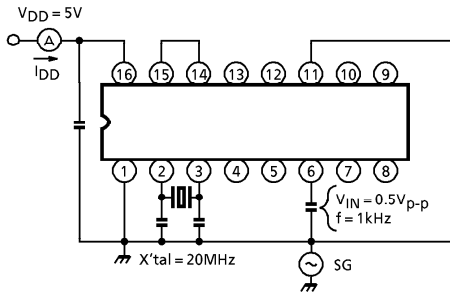
ELECTRICAL CHARACTERISTICS (Unless otherwise specified Ta = 25°C, V_{DD} = 5V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Operating Supply Voltage	V _{DD}	—	※	4.5	5.0	5.5	V	
Operating Supply Current	I _{DD}	1	X'tal = 20MHz, CP _{in} = CP _{out}	—	15.0	25.0	mA	
Operating Frequency Range	X _T	f _{XT}	2	※	1.5	~	20.0	MHz
	CP _{in}	f _{CP}	3	V _{in} Square Wave	0.3	~	10.0	MHz
	FG _{in}	f _{FG}	—	V _{in} = 0.5V _{p-p} Sine Wave	—	~	4.0	kHz
Input Amplitude Voltage	FG _{in}	V _{inFG}	4	f _{FG} = 4kHz, Sine Wave, AC input	0.5	~	V _{DD} - 0.5	V _{p-p}
AFC, APC D/A Converter	Deviation	—	—	—	±2.0	±4.0	LSB	
	Resolution	—	—	—	V _{DD} /256	—	V	
Pull-up Resistor	R _{in}	—	N1, N2, N/W, R/S	15	30	60	kΩ	
Input Voltage	"H" Level	V _{IH}	—	N1, N2, N/W, R/S, CP _{in}	V _{DD} × 0.8	~	V _{DD}	V
	"L" Level	V _{IL}	—	N1, N2, N/W, R/S, CP _{in}	0	~	V _{DD} × 0.2	
Input Leak Current	I _{IH}	—	—	CP _{in}	—	—	±1.0	μA
	I _{IL}	—	—	CP _{in}	—	—	±1.0	
Output Current	"H" Level	I _{OH}	—	RV, LD, CP _{out} V _{OH} = 4.5V	-0.5	-2.5	—	mA
	"L" Level	I _{OL}	—	RV, LD, CP _{out} V _{OL} = 0.5V	0.5	2.5	—	
	"H" Level	I _{OH}	—	APC, AFC V _{OH} = 4.5V	-0.3	-1.0	—	μA
	"L" Level	I _{OL}	—	APC, AFC V _{OL} = 0.5V	25	75	—	
Amplifier Feedback Resistor	X _T	R _f	5	—	150	330	660	kΩ
	FG _{in}	R _f	5	—	150	330	660	kΩ

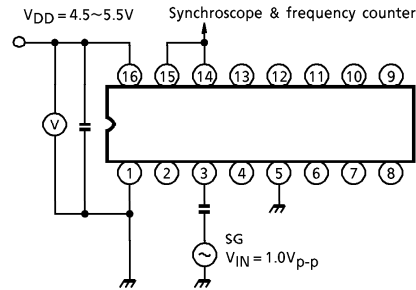
※ : Guaranteed within the range of V_{DD} = 4.5~5.5V, Ta = -40~85°C

TEST CIRCUIT

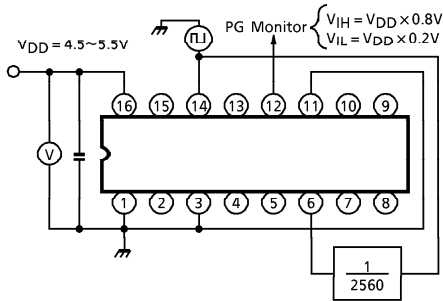
1. Operating Supply Current I_{DD}



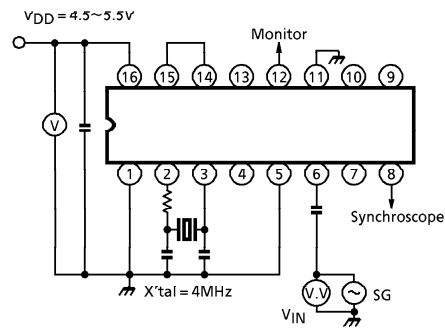
2. X_T Operating Frequency Range f_{MAX} (f_{XT})



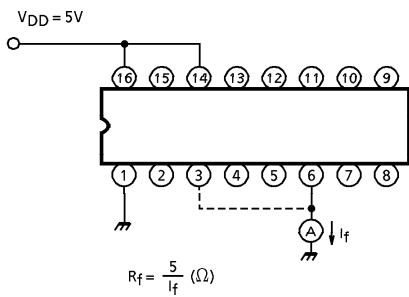
3. CP_{IN} Operating Frequency Range f_{MAX} (f_{CP})



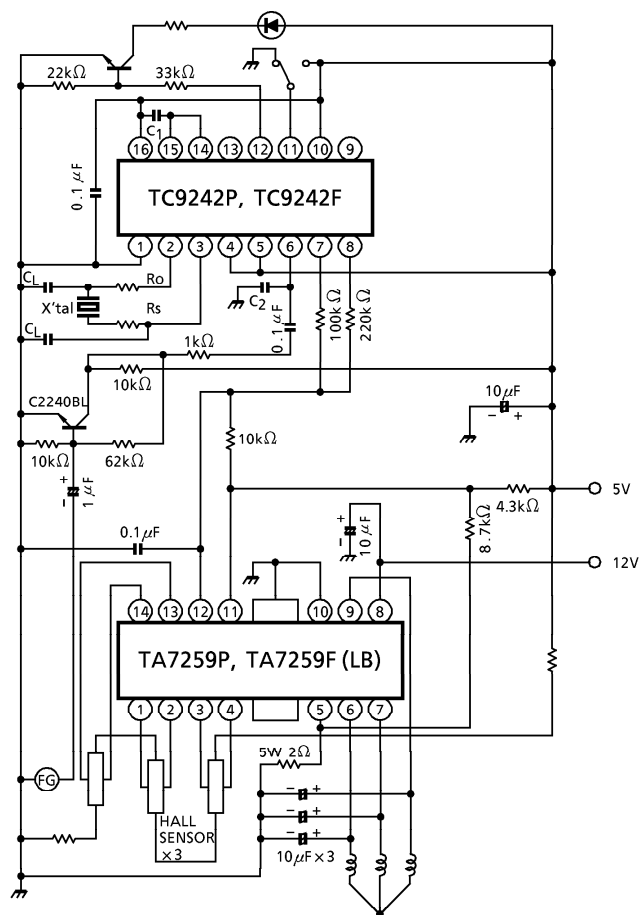
4. FG_{IN} Input Sensitivity V_{INFG}



5. Amplifier Feedback Resistor R_f



APPLICATION CIRCUIT



- Example of crystal oscillation frequency calculation.

When FG' (number of FG pulse) = 180 pulses and R (revolution of motor) = 200rpm., if the dividing frequency of reference divider and lock range is set at N = 5 dividing frequency and N/W = 20, the crystal oscillation frequency f_x is as follows :

$$f_x = \frac{R}{60} \times FG' \times 128 \times 20 \times N = \frac{200}{60} \times 180 \times 128 \times 20 \times 5 = 7.68\text{MHz}$$

- Select the external filter of the differential amplifier in the application circuit depending on the response characteristics of the motor used.
- Determine values C1, C2, CL, Ro and Rs in the application circuit depending on the characteristics of the circuit.

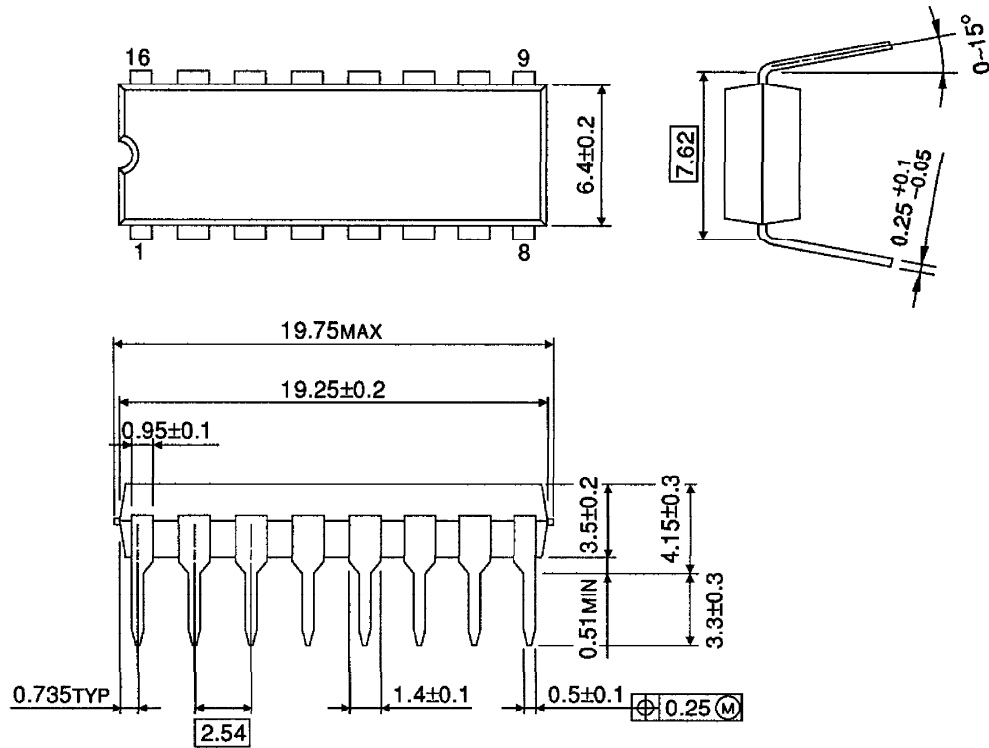
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OUTLINE DRAWING
DIP16-P-300A

Unit : mm

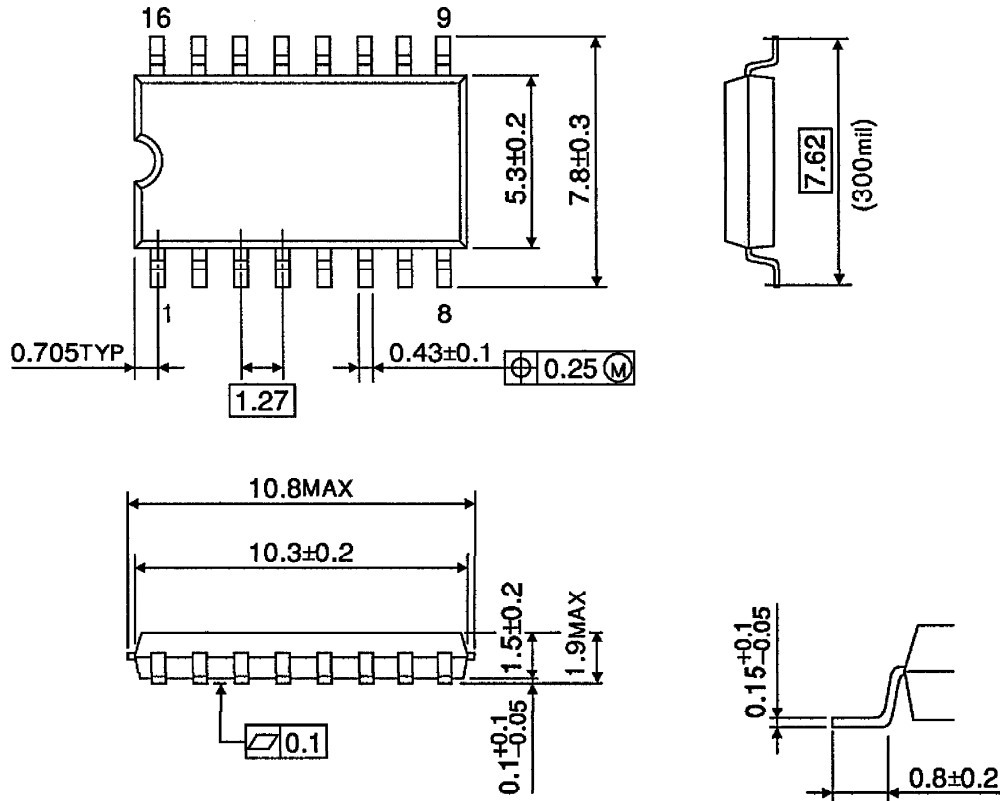


Weight : 1.00g (Typ.)

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OUTLINE DRAWING
SOP16-P-300

Unit : mm



Weight : 0.16g (Typ.)

TC9242P - 12*

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