TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

4,194,304-WORD × 16-BIT EDO (HYPER PAGE) DYNAMIC RAM

DESCRIPTION

The TC5164(5)165BFT/BFTS is an EDO (hyper page) dynamic RAM organized as 4,194,304 words by 16 bits. The TC5164(5)165BFT/BFTS utilizes TOSHIBA's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5164(5)165BFT/BFTS to be packaged in a 50-pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. Other features include a single power supply of 3.3V±0.3V tolerance and direct interfacing with high performance logic families such as LVTTL.

FEATURES

- 4,194,304-word by 16-bit organization
- Fast access time and cycle time

		TC5164(5)165BFT/BFTS	
		-40	-50
t_{RAC}	$\overline{RAS}$ Access Time	40ns	50ns
t_{AA}	Column Address Access Time	20ns	25ns
t_{CAC}	$\overline{CAS}$ Access Time	11ns	13ns
t_{RC}	Cycle Time	69ns	84ns
t_{HPC}	Hyper Page Mode Cycle Time	16ns	20ns

- Single power supply of 3.3V±0.3V with a built-in V_{BB} generator
- Low power dissipation (max)
  Operating : 306mW (TC5164165BFT/BFTS-40)
  252mW (TC5164165BFT/BFTS-50)
  432mW (TC5165165BFT/BFTS-40)
  360mW (TC5165165BFT/BFTS-50)
  Standby : 1.8mW
  0.72mW (S-version)
- Outputs unlatched at cycle end, allowing two-dimensional chip selection
- Read-Modify-Write and EDO (Hyper Page mode) capability
- All inputs and outputs LVTTL-compatible
- Package
  TSOP II 50-P-400-0.80D, 0.50 grams

Part No.	Row Add.	Col. Add.	Refresh	Refresh Cycle
TC5164165BFT	A0 to A12	A0 to A8	$\overline{RAS}$-Only refresh	8192/64 ms
			$\overline{CAS}$-before-$\overline{RAS}$ refresh, Hidden refresh	4096/64 ms
TC5165165BFT	A0 to A11	A0 to A9	$\overline{RAS}$-Only refresh, $\overline{CAS}$ -before-$\overline{RAS}$ refresh, Hidden refresh	4096/64 ms
TC5164165BFTS (S-version)	A0 to A12	A0 to A8	$\overline{RAS}$-Only refresh	8192/128 ms
			$\overline{CAS}$-before-$\overline{RAS}$ refresh, Hidden refresh, Self-refresh	4096/128 ms
TC5165165BFTS (S-version)	A0 to A11	A0 to A9	$\overline{RAS}$-Only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, Hidden refresh, Self-refresh	4096/128 ms

TC5164165BFT/BFTS

PIN ASSIGNMENT (TOP VIEW)

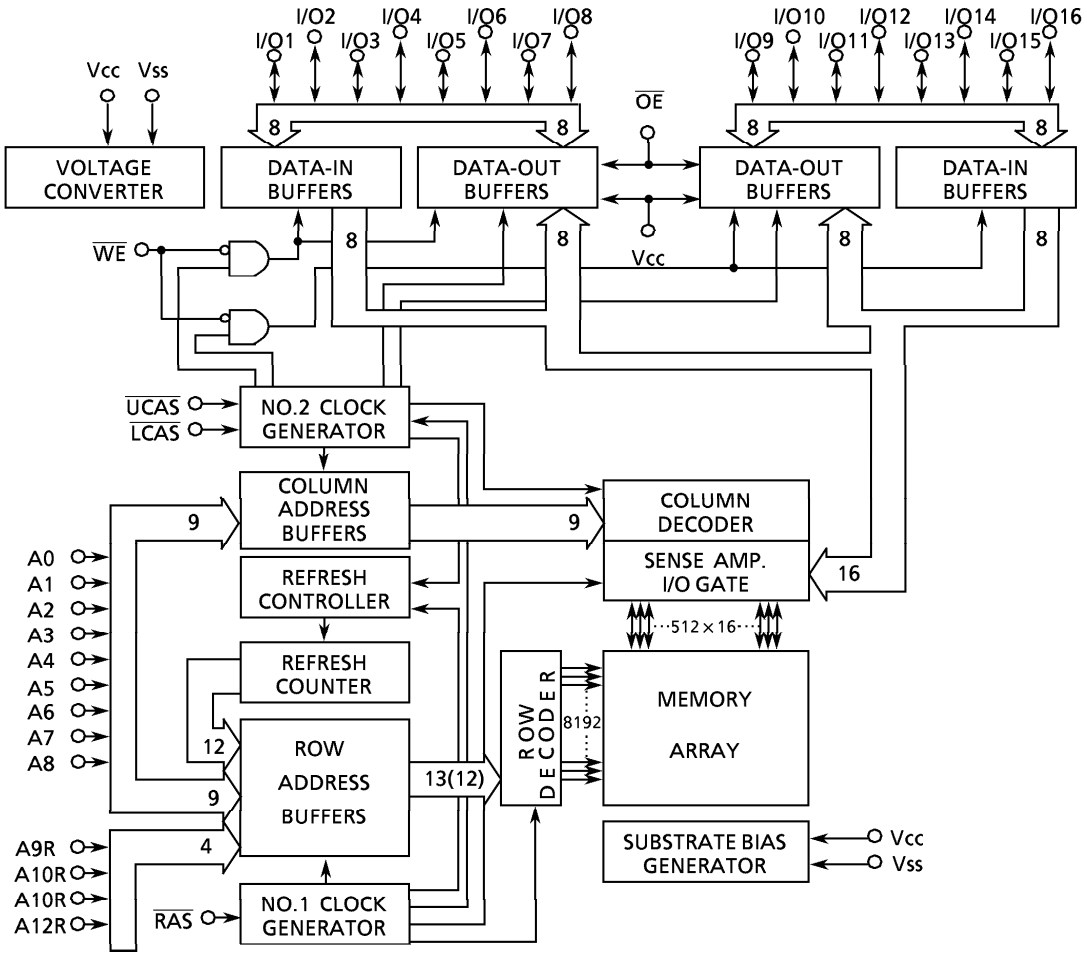
Plastic TSOP
(Normal Bend Type)

V_{CC}	1	50	V_{SS}
I/O1	2	49	I/O16
I/O2	3	48	I/O15
I/O3	4	47	I/O14
I/O4	5	46	I/O13
V_{CC}	6	45	V_{SS}
I/O5	7	44	I/O12
I/O6	8	43	I/O11
I/O7	9	42	I/O10
I/O8	10	41	I/O9
NC	11	40	NC
V_{CC}	12	39	V_{SS}
$\overline{WE}$	13	38	$\overline{LCAS}$
$\overline{RAS}$	14	37	$\overline{UCAS}$
NC	15	36	$\overline{OE}$
NC	16	35	NC
NC	17	34	NC
NC	18	33	A12R
A0	19	32	A11R
A1	20	31	A10R
A2	21	30	A9R
A3	22	29	A8
A4	23	28	A7
A5	24	27	A6
V_{CC}	25	26	V_{SS}

PIN NAMES

A0 to A12	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe / Upper Byte Control
$\overline{LCAS}$	Column Address Strobe / Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O1 to I/O16	Data Input/Output
V_{CC}	Power (+ 3.3V)
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



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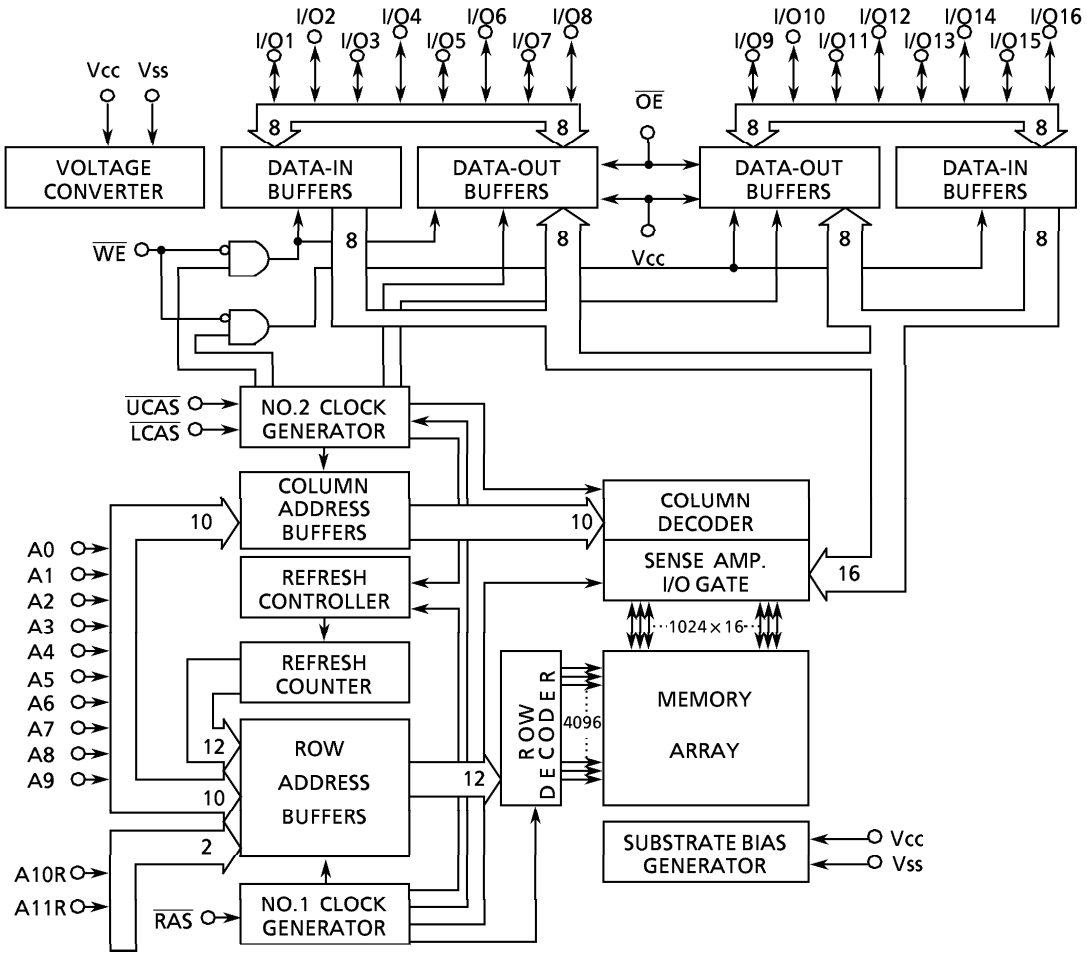
Plastic TSOP
(Normal Bend Type)

V_{CC}	1	50	V_{SS}
I/O1	2	49	I/O16
I/O2	3	48	I/O15
I/O3	4	47	I/O14
I/O4	5	46	I/O13
V_{CC}	6	45	V_{SS}
I/O5	7	44	I/O12
I/O6	8	43	I/O11
I/O7	9	42	I/O10
I/O8	10	41	I/O9
NC	11	40	NC
V_{CC}	12	39	V_{SS}
$\overline{WE}$	13	38	$\overline{LCAS}$
$\overline{RAS}$	14	37	$\overline{UCAS}$
NC	15	36	$\overline{OE}$
NC	16	35	NC
NC	17	34	NC
NC	18	33	NC
A0	19	32	A11R
A1	20	31	A10R
A2	21	30	A9
A3	22	29	A8
A4	23	28	A7
A5	24	27	A6
V_{CC}	25	26	V_{SS}

PIN NAMES

A0 to A11	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe / Upper Byte Control
$\overline{LCAS}$	Column Address Strobe / Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O1 to I/O16	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTES
Input Voltage	V_{IN}	– 0.3 to Vcc + 0.3	V	1
Output Voltage	V_{OUT}	– 0.3 to Vcc + 0.3	V	1
Power Supply Voltage	V_{CC}	– 0.3 to 4.6	V	1
Operating Temperature	T_{OPR}	0 to 70	°C	1
Storage Temperature	T_{STG}	– 55 to 150	°C	1
Soldering Temperature (10 s)	T_{SOLDER}	260	°C	1
Power Dissipation	P_D	1.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to 70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	2
V_{IH}	Input High Voltage	2.0	–	Vcc + 0.3*	V	2
V_{IL}	Input Low Voltage	– 0.3**	–	0.8	V	2

* Vcc + 1.2V at pulse width ≦ 20ns (pulse width is measured at Vcc)
** – 1.2V at pulse width ≦ 20ns (pulse width is measured at Vss)

CAPACITANCE (V_{CC} = 3.3V ± 0.3V, f = 1 MHz, Ta = 0 to 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (Address)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	–	7	pF
C_O	I/O Capacitance (I/O1 to I/O16)	–	7	pF

DC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V, Ta = 0 to 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ min)	TC5164165BFT/BFTS-40	–	85	mA	3, 4, 5
		TC5164165BFT/BFTS-50	–	70		
		TC5165165BFT/BFTS-40	–	120		
		TC5165165BFT/BFTS-50	–	100		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	1	mA	
I_{CC3}	$\overline{RAS}$-ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$-Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ min)	TC5164165BFT/BFTS-40	–	85	mA	3, 5
		TC5164165BFT/BFTS-50	–	70		
		TC5165165BFT/BFTS-40	–	120		
		TC5165165BFT/BFTS-50	–	100		
I_{CC4}	HYPER PAGE MODE CURRENT Average Power Supply Current, Hyper Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{HPC} = t_{HPC}$ min)	TC5164165BFT/BFTS-40	–	90	mA	3, 4, 5
		TC5164165BFT/BFTS-50	–	75		
		TC5165165BFT/BFTS-40	–	90		
		TC5165165BFT/BFTS-50	–	75		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	500 200 (S-version)	μA	
I_{CC6}	$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ min)	TC5164165BFT/BFTS-40	–	120	mA	3, 5
		TC5164165BFT/BFTS-50	–	100		
		TC5165165BFT/BFTS-40	–	120		
		TC5165165BFT/BFTS-50	–	100		
I_{CC7}	BATTERY BACK-UP CURRENT Average Power Supply Current, Battery Back-up Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = $\overline{CAS}$-before-$\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$, $\overline{WE}$, Address = V_{CC} – 0.2V or 0.2V, I/O1 to I/O16 = V_{CC} – 0.2V, 0.2V or Hi-Z: t_{RC} = 31.2μs $t_{RAS} = t_{RAS}$ min to 300ns)		–	500 (S-version)	μA	
I_{CCS}	SELF-REFRESH CURRENT Average Power Supply Current, Self-Refresh Mode ($\overline{RAS} = \overline{CAS} = V_{IL}$, $\overline{OE}$, $\overline{WE}$, Address = V_{CC} – 0.2V or 0.2V, I/O1 to I/O16 = V_{CC} – 0.2V, 0.2V or Hi-Z)		–	400 (S-version)	μA	
$I_{I\ (L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, Any Input (0 V ≦ V_{IN} ≦ Vcc, All Other Pins Not under Test = 0 V)		– 10	10	μA	
$I_{O\ (L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} Is Disabled, 0 V ≦ V_{OUT} ≦ Vcc)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output H Level Voltage (I_{OUT} = – 2mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output L Level Voltage (I_{OUT} = 2mA)		–	0.4	V	

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 3.3V ± 0.3V, Ta = 0 to 70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC5164(5)165BFT/BFTS				UNIT	NOTES
		-40		-50			
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read-or-Write Cycle Time	69	–	84	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	92	–	111	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	40	–	50	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	–	11	–	13	ns	9, 14
t_{AA}	Access Time from Column Address	–	20	–	25	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	22	–	28	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	11	0	13	ns	10, 16
t_T	Transition Time (Rise and Fall)	1	50	1	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	25	–	30	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	40	10,000	50	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Hyper Page Mode)	40	100,000	50	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	6	–	8	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Hyper Page Mode)	22	–	28	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	30	–	35	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	6	10,000	8	10,000	ns	
t_{RCD}	$\overline{RAS}$-to-$\overline{CAS}$ Delay Time	10	29	12	37	ns	14
t_{RAD}	$\overline{RAS}$-to-Column-Address Delay Time	8	20	10	25	ns	15
t_{CRP}	$\overline{CAS}$-to-$\overline{RAS}$ Precharge Time	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	6	–	8	–	ns	
t_{ASR}	Row Address Set up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	6	–	8	–	ns	
t_{ASC}	Column Address Set up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	6	–	8	–	ns	
t_{RAL}	Column-Address-to-$\overline{RAS}$ Lead Time	20	–	25	–	ns	
t_{RCS}	Read Command Set up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	6	–	8	–	ns	
t_{WP}	Write Command Pulse Width	6	–	8	–	ns	
t_{RWL}	Write-Command-to-$\overline{RAS}$ Lead Time	6	–	8	–	ns	
t_{CWL}	Write-Command-to-$\overline{CAS}$ Lead Time	6	–	8	–	ns	
t_{DS}	Data Set up Time	0	–	0	–	ns	12
t_{DH}	Data Hold Time	6	–	8	–	ns	12

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC5164(5)165BFT/BFTS				UNIT	NOTES
		-40		-50			
		MIN	MAX	MIN	MAX		
t_{REF}	Refresh Period	–	64	–	64	ms	
		–	128 (S-version)	–	128 (S-version)		
t_{WCS}	Write Command Set up Time	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$-to-$\overline{WE}$ Delay Time	26	–	30	–	ns	13
t_{RWD}	$\overline{RAS}$-to-$\overline{WE}$ Delay Time	55	–	67	–	ns	13
t_{AWD}	Column-Address-to-$\overline{WE}$ Delay Time	35	–	42	–	ns	13
t_{CPWD}	$\overline{CAS}$-Precharge-to-$\overline{WE}$ Delay Time	37	–	45	–	ns	13
t_{CSR}	$\overline{CAS}$ Set up Time ($\overline{CAS}$-before-$\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Cycle)	6	–	8	–	ns	
t_{RPC}	$\overline{RAS}$-to-$\overline{CAS}$ Precharge Time	5	–	5	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	6	–	8	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	11	–	13	ns	9
t_{OED}	$\overline{OE}$-to-Data Delay	11	–	13	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	ns	
t_{OEZ}	Output Buffer Turn-off Delay Time from $\overline{OE}$	0	11	0	13	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	6	–	8	–	ns	
t_{ODS}	Output Disable Set up Time	0	–	0	–	ns	
t_{WRP}	$\overline{WE}$-to-$\overline{RAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{WRH}	$\overline{WE}$-to-$\overline{RAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Cycle)	6	–	8	–	ns	
t_{RNCD}	$\overline{RAS}$-to-Next-$\overline{CAS}$ Delay Time (Hyper Page Mode)	40	–	50	–	ns	
t_{HPC}	Hyper Page Mode Cycle Time	16	–	20	–	ns	
t_{HPRWC}	Hyper Page Mode Read-Modify-Write Cycle Time	47	–	57	–	ns	
t_{COH}	Output Data Hold Time	5	–	5	–	ns	
t_{REZ}	Output Buffer Turn-off Delay from $\overline{RAS}$	0	11	0	13	ns	10, 16
t_{WEZ}	Output Buffer Turn-off Delay from $\overline{WE}$	0	11	0	13	ns	10
t_{WED}	$\overline{WE}$-to-Data Delay	11	–	13	–	ns	
t_{OE}	$\overline{OE}$ Pulse Width	11	–	13	–	ns	
t_{OEP}	$\overline{OE}$ Precharge Time	6	–	8	–	ns	
t_{CPO}	$\overline{CAS}$-to-$\overline{OE}$ Precharge Time	5	–	5	–	ns	
t_{OCH}	$\overline{CAS}$ Hold Time Referenced to $\overline{OE}$	6	–	8	–	ns	
t_{RASS}	$\overline{RAS}$ Pulse Width ($\overline{CAS}$-before-$\overline{RAS}$ Self-Refresh) (S-version only)	100	–	100	–	μs	
t_{RPS}	$\overline{RAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ Self-Refresh) (S-version only)	69	–	84	–	ns	
t_{CHS}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Self-Refresh) (S-version only)	– 50	–	– 50	–	ns	

NOTES:

1. Conditions outside the limits listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on the cycle rate.
4. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. The address can be changed once at most while $\overline{RAS}=V_{IL}$. In the case of I_{CC4}, it can be changed once at most during a Hyper Page Mode cycle (t_{HPC}).
6. An initial pause of 200μs is required after power-up followed by a minimum of eight $\overline{RAS}$-Only refresh cycles before proper device operation is achieved. When using the internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles instead of eight $\overline{RAS}$-Only refresh cycles is required.
7. AC measurements assume $t_T=2$ns.
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Also, transition times are measured between the V_{IH} and V_{IL} levels.
9. This is measured with a load equivalent to 100pF at V_{OH} = 2.0V (I_{OUT} = −2mA), V_{OL} = 0.8V (I_{OUT} = 2mA).
10. t_{OFF} (max), t_{OEZ} (max), t_{REZ} (max) and t_{WEZ} (max) define the time at which the output goes open circuit and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a Read cycle.
12. These parameters are referenced to the leading edge of $\overline{CAS}$ in Early Write cycles and to the leading edge of $\overline{WE}$ in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an Early Write cycle and the Data-out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min), $t_{AWD} \geqq t_{AWD}$ (min) and $t_{CPWD} \geqq t_{CPWD}$ (min) (Hyper Page mode), the cycle is a Read-Modify-Write cycle and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the data output (at access time) is indeterminate.
14. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then the access time is determined by t_{CAC}.
15. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then the access time is determined by t_{AA}.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ goes high, the output goes open circuit when $\overline{CAS}$ goes high (t_{OFF}). If $\overline{CAS}$ goes high before $\overline{RAS}$ goes high, the output goes open circuit when $\overline{RAS}$ goes high (t_{REZ}).

DATA-OUT HI-Z CONTROL LOGIC

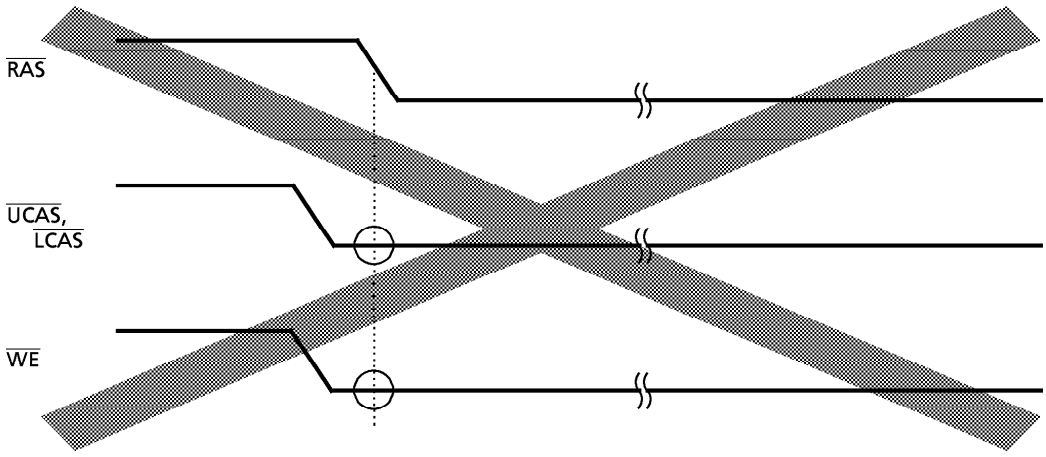
$\overline{RAS}$	$\overline{UCAS}$, $\overline{LCAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
H	↗	L	H	t_{OFF}
↗	H	L	H	t_{REZ}
L	L	↗	H	t_{OEZ}
L	H	L	↘	t_{WEZ}

DATA-OUT LO-Z CONTROL LOGIC

$\overline{RAS}$	$\overline{UCAS}$, $\overline{LCAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
L	↘	L	H	t_{CLZ}
L	L	↘	H	t_{OLZ}
L	L	↗↘	H	t_{OLZ}

CAUTION

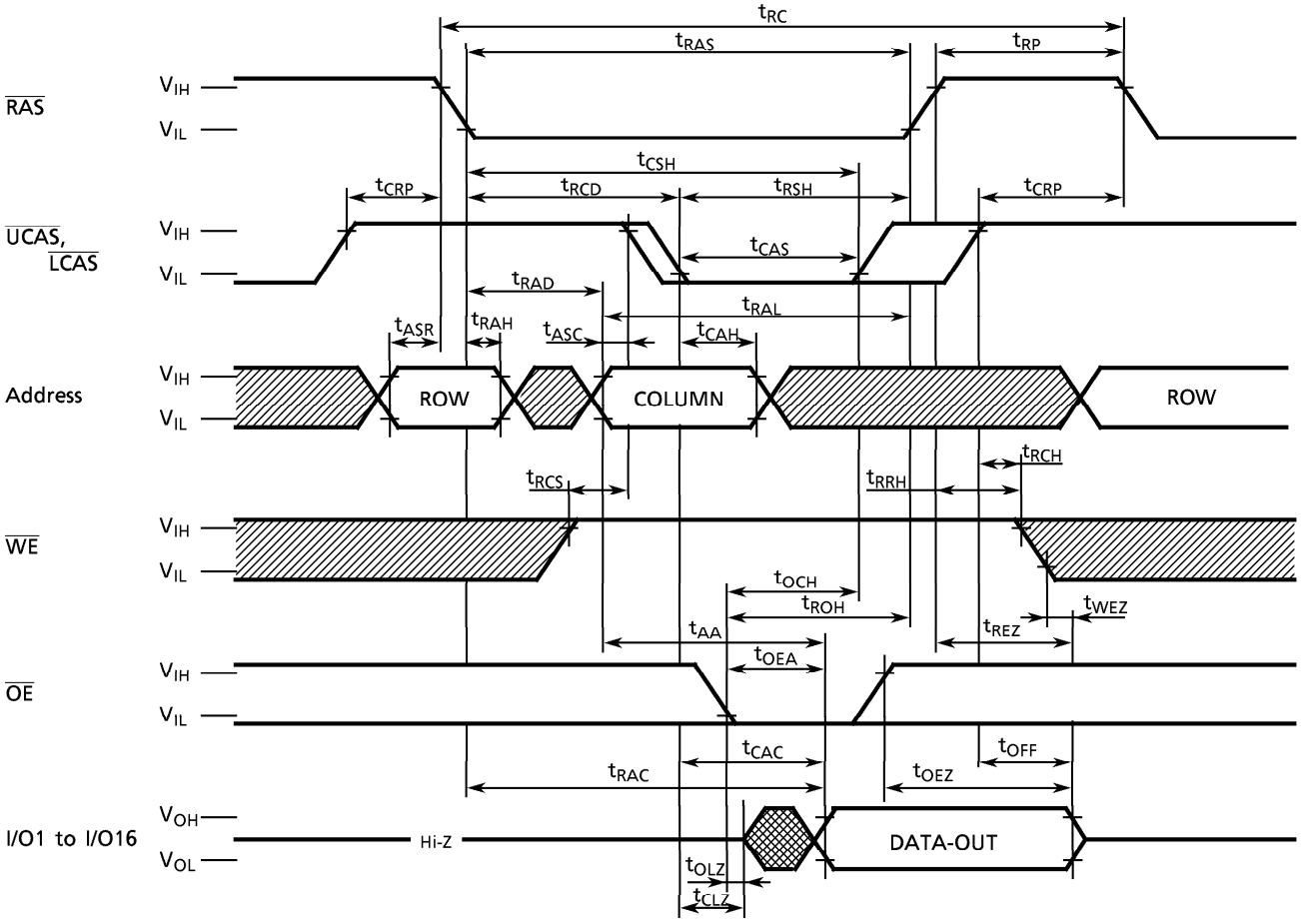
The WCBR ($\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$) timing shown below is not allowed during normal operation, such as during Read, Write and Refresh operations. When WCBR is input, a malfunction may occur due to the change in internal circuit operation status.



WCBR timing

TIMING DIAGRAMS

READ CYCLE

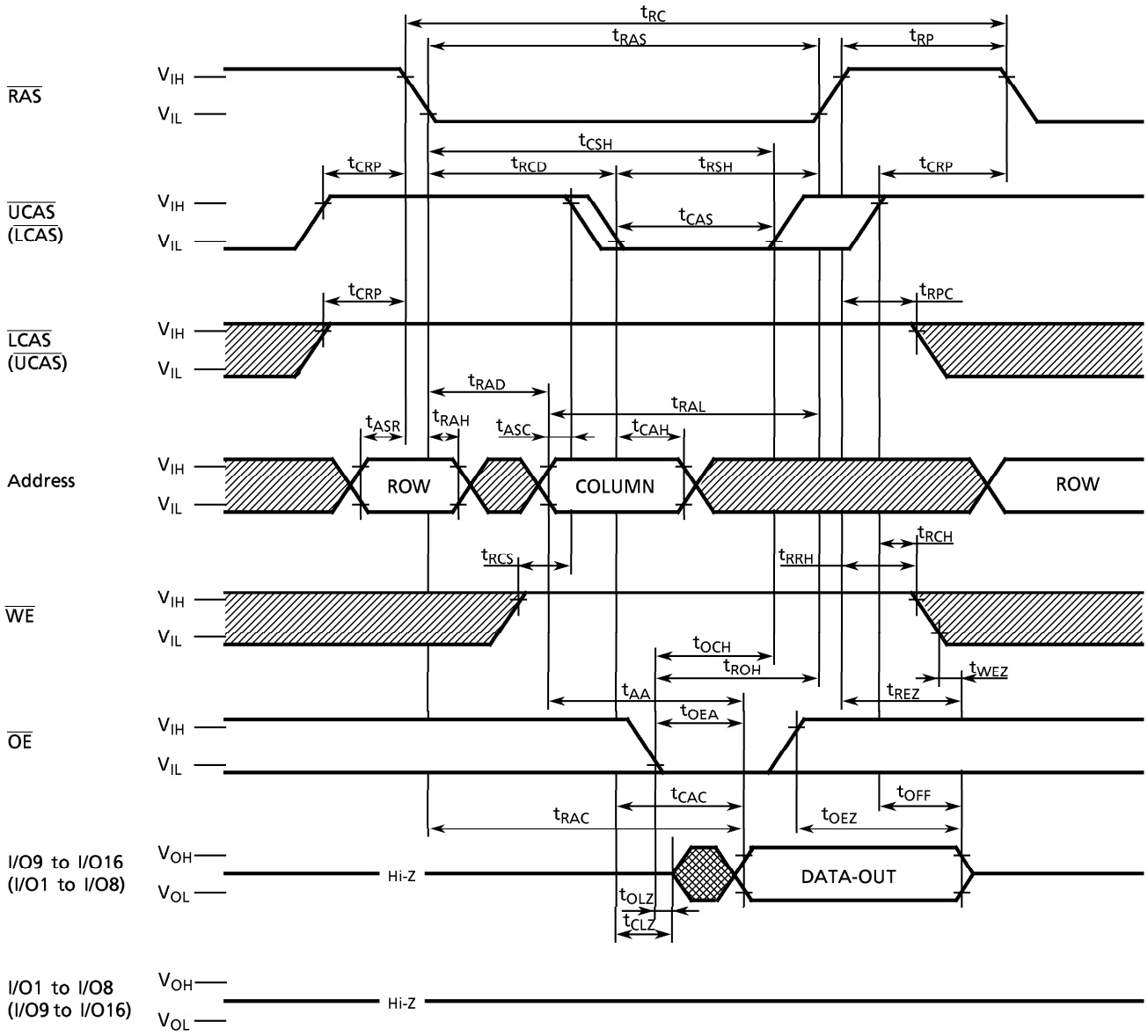


Note: D_{IN} = Hi-Z

: H or L

: Invalid Data

BYTE READ CYCLE

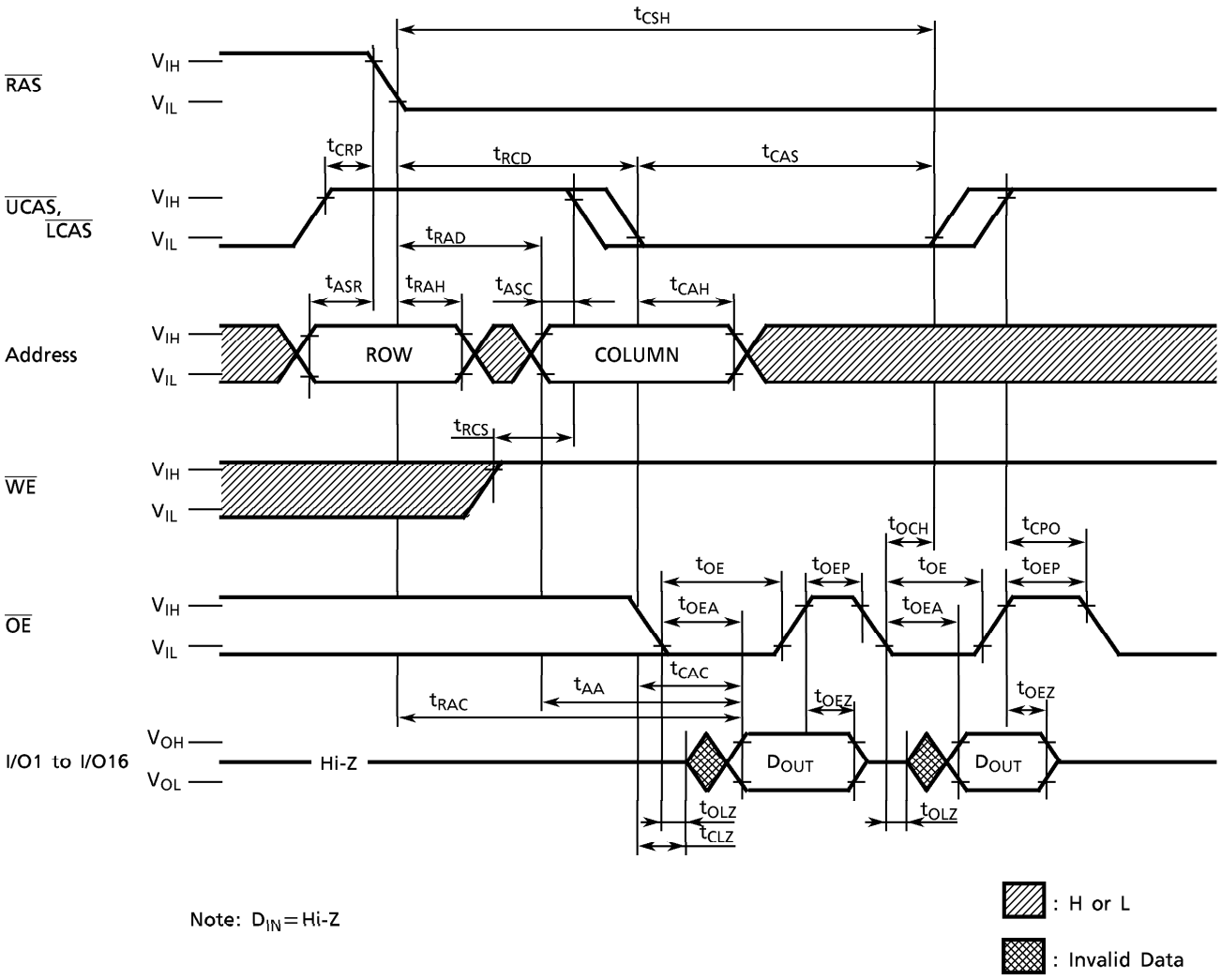


Note: D_{IN} (I/O1 to I/O8) = Don't Care
D_{IN} (I/O9 to I/O16) = Hi-Z
(D_{IN} (I/O1 to I/O8) = Hi-Z
D_{IN} (I/O9 to I/O16) = Don't Care)

: H or L

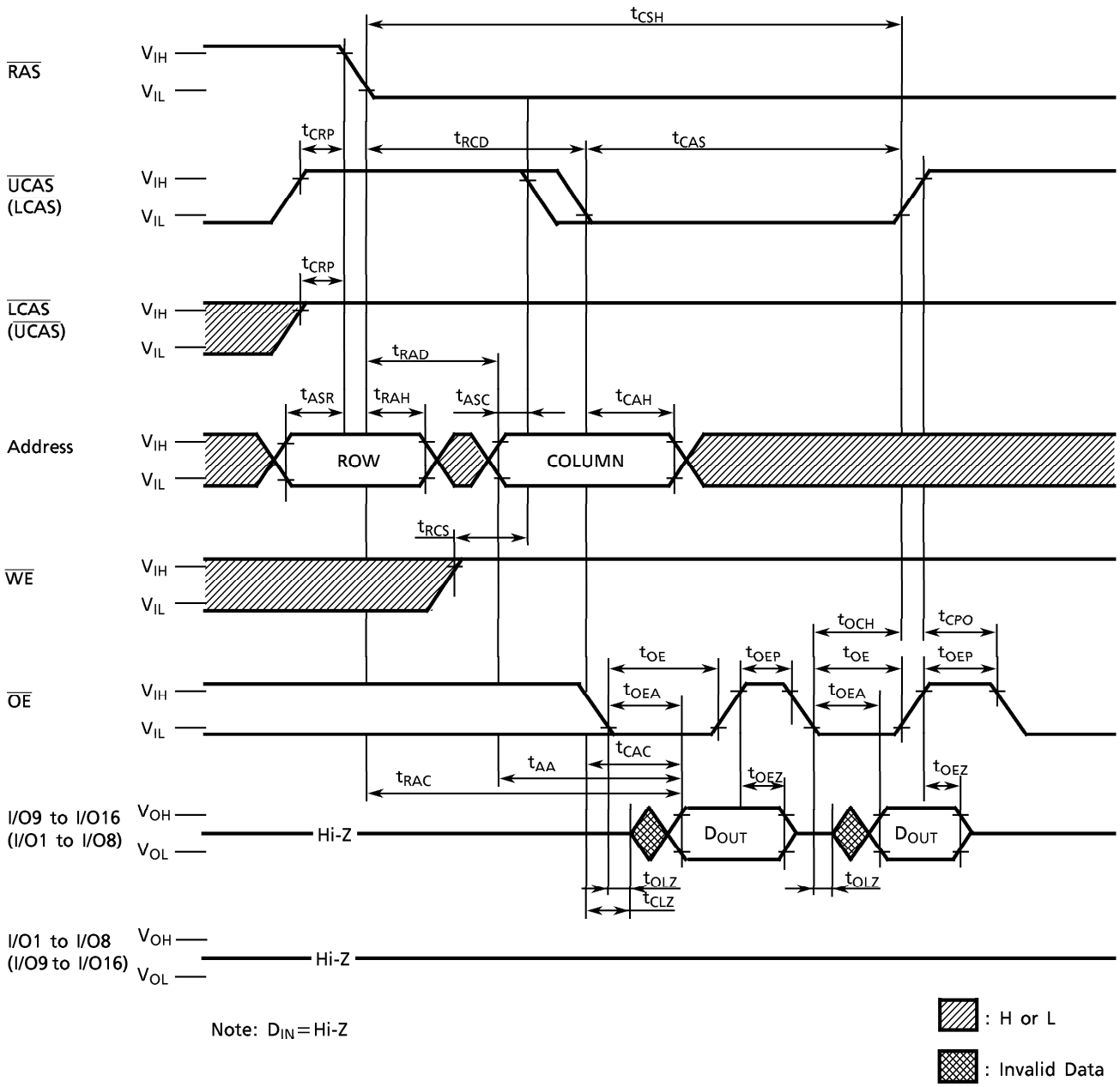
: Invalid Data

$\overline{OE}$-CONTROLLED READ CYCLE



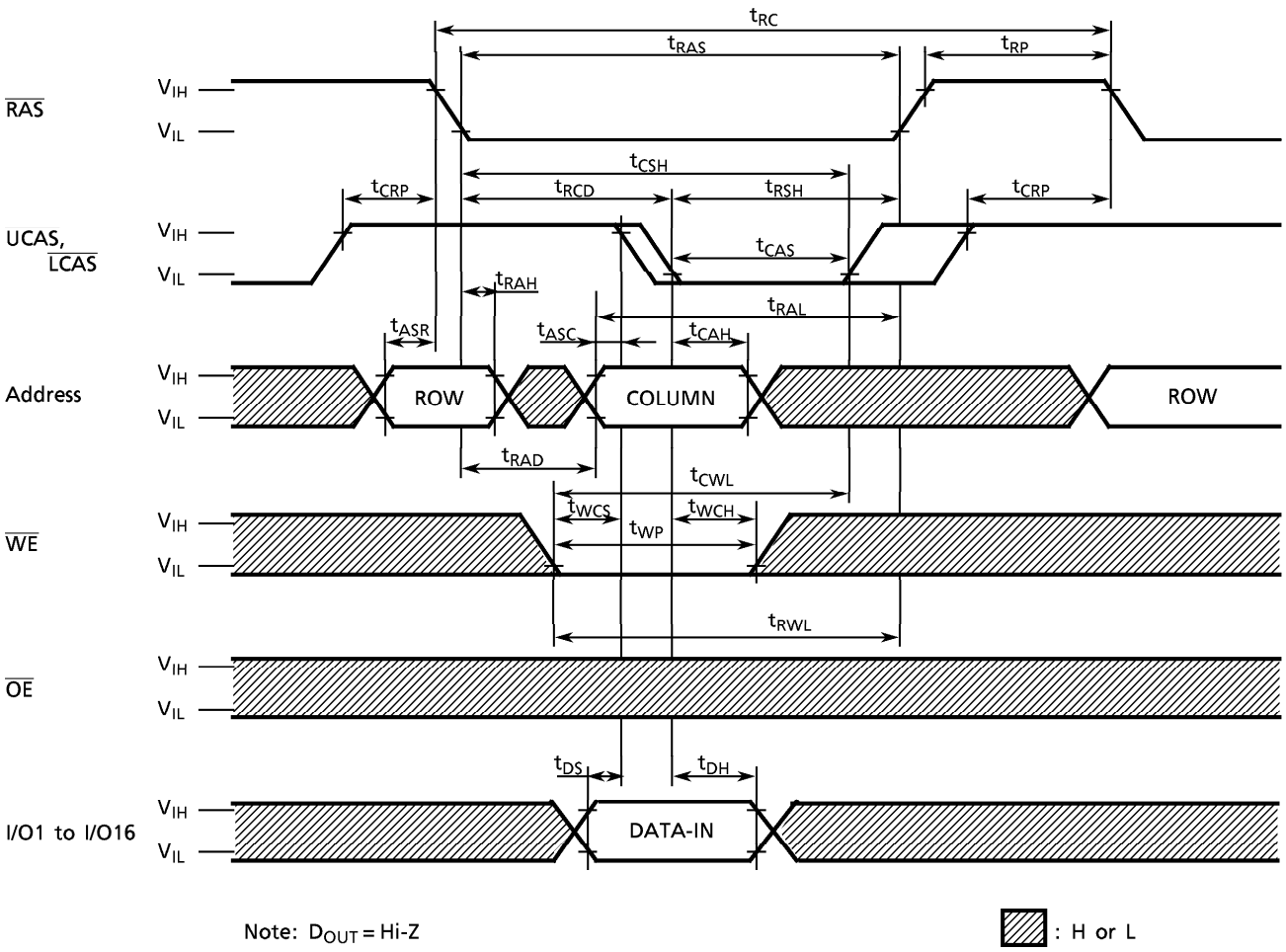
Note: D_{IN} = Hi-Z

$\overline{OE}$-CONTROLLED BYTE READ CYCLE



Note: D_{IN} = Hi-Z

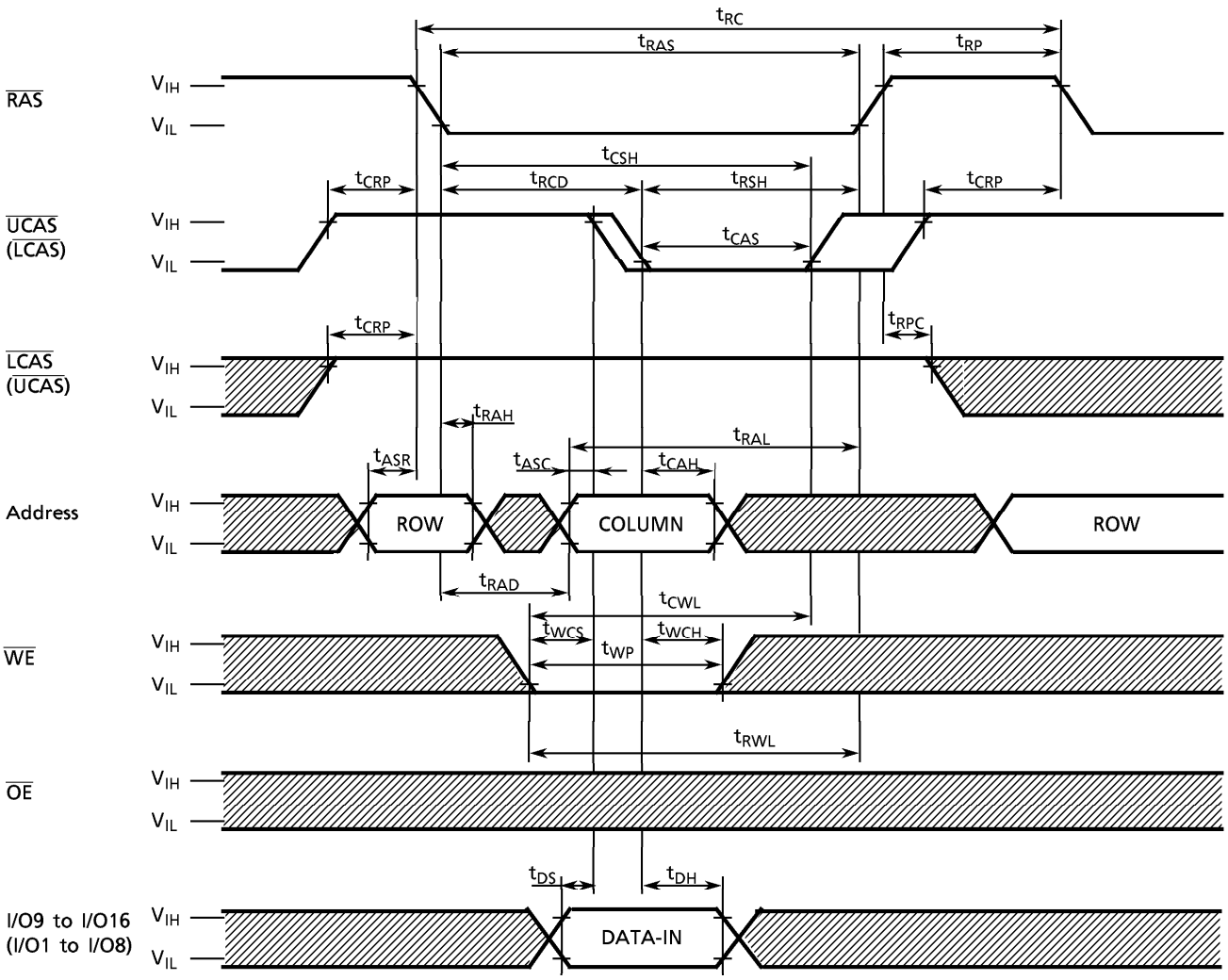
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = Hi-Z

▨ : H or L

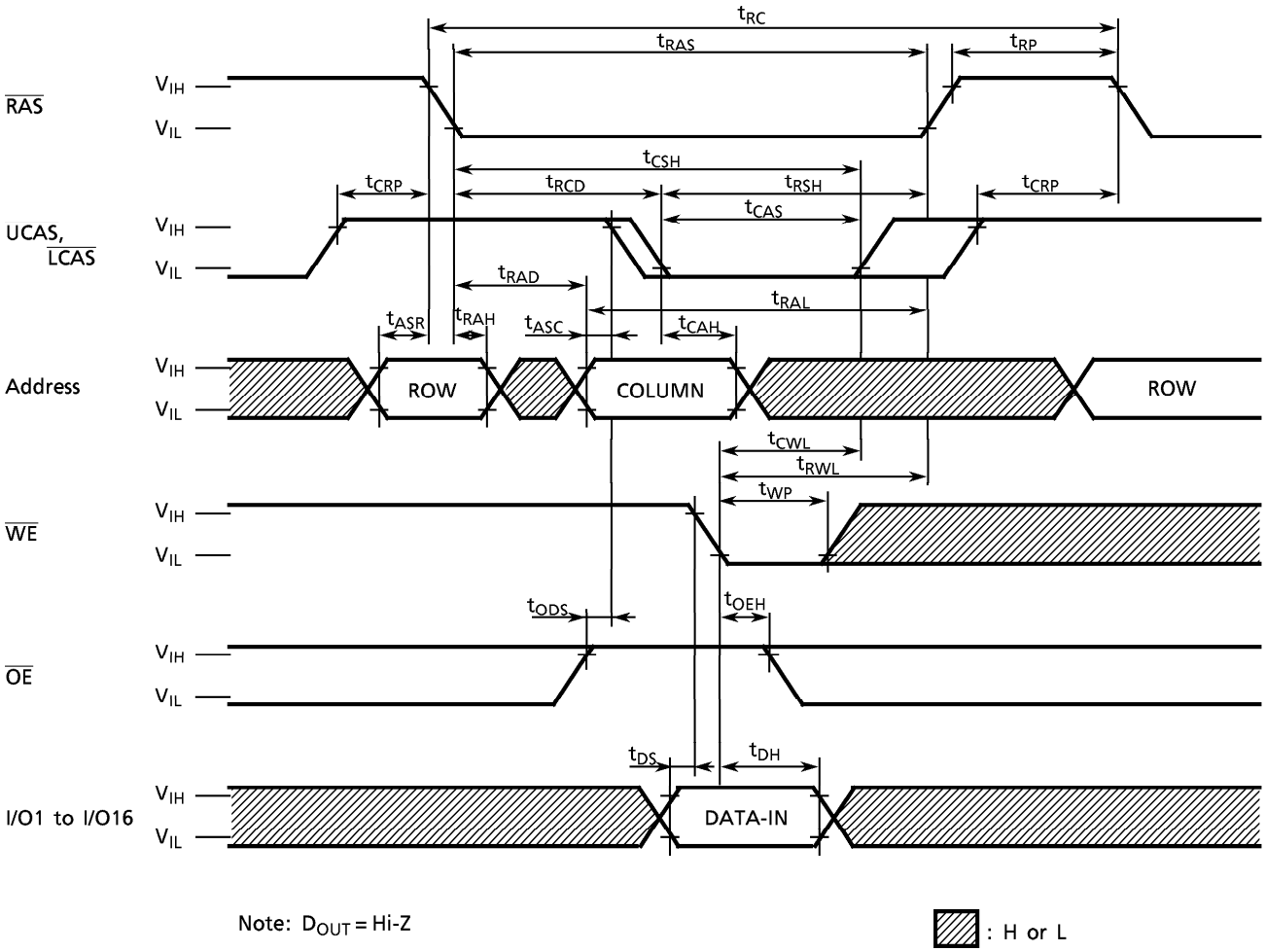
BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{IN} (I/O1 to I/O8) = Don't Care
D_{OUT} = Hi-Z
(D_{IN} (I/O9 to I/O16) = Don't Care
D_{OUT} = Hi-Z)

: H or L

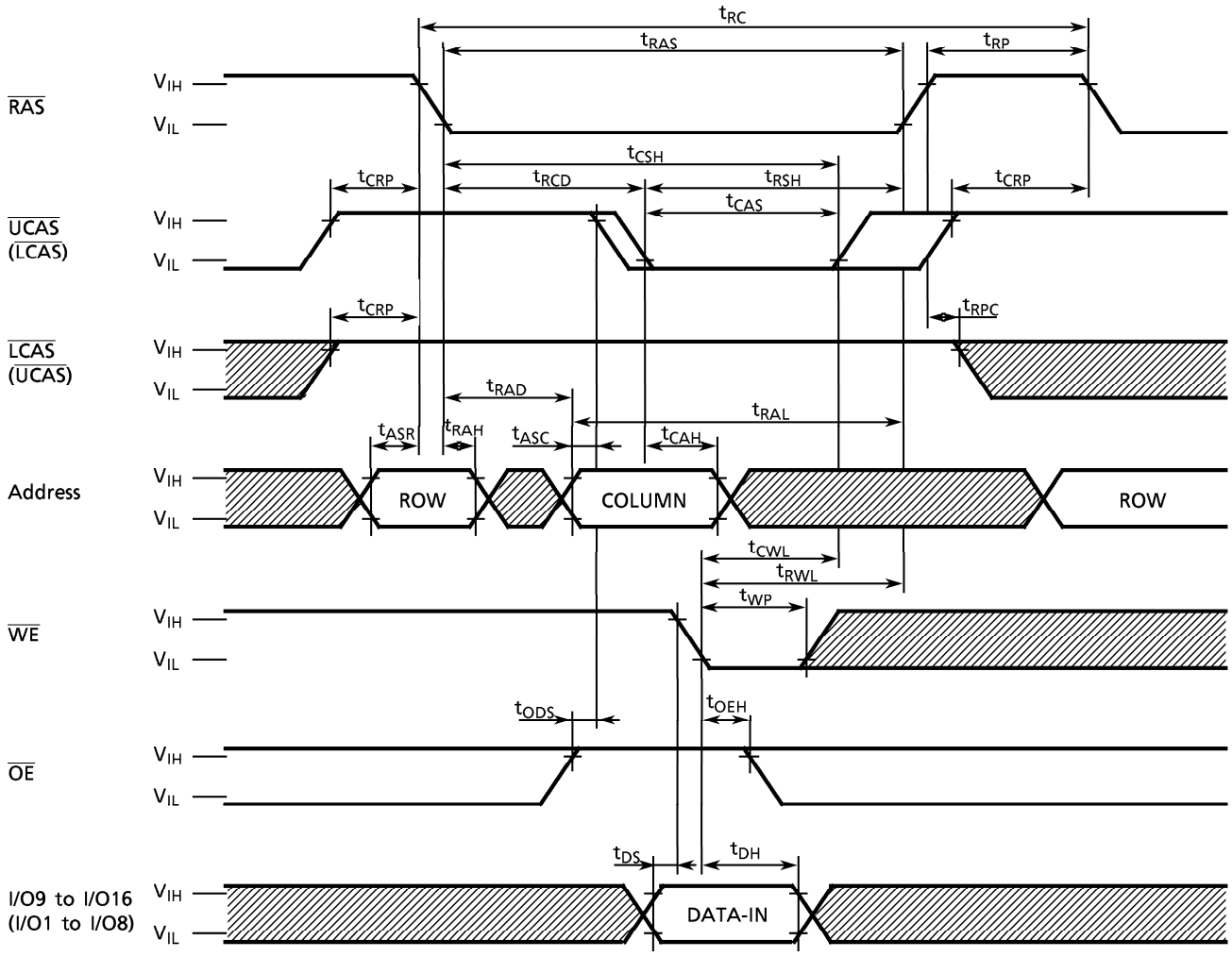
$\overline{OE}$-CONTROLLED WRITE CYCLE



Note: D_{OUT} = Hi-Z

▨ : H or L

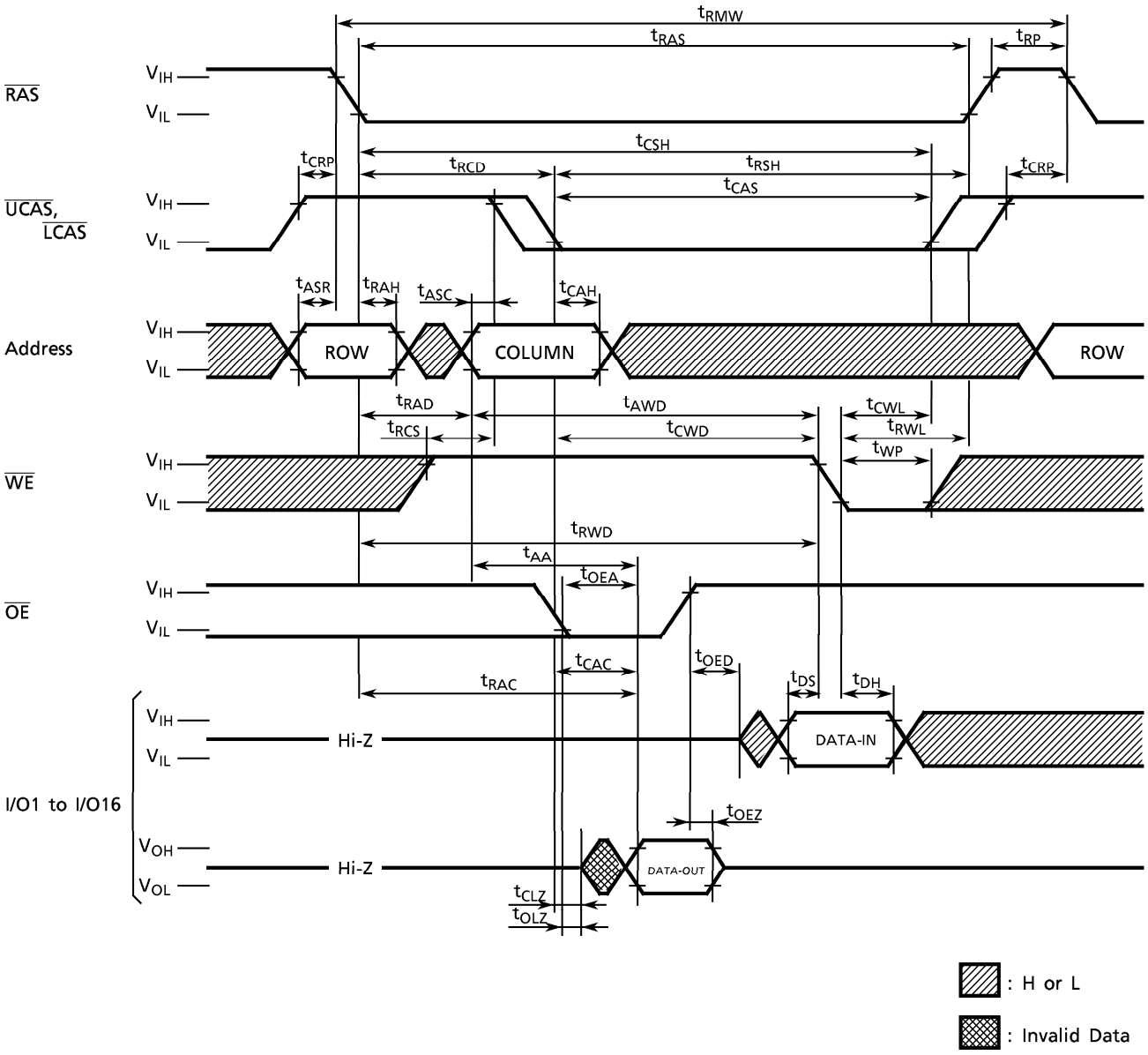
$\overline{OE}$-CONTROLLED BYTE WRITE CYCLE



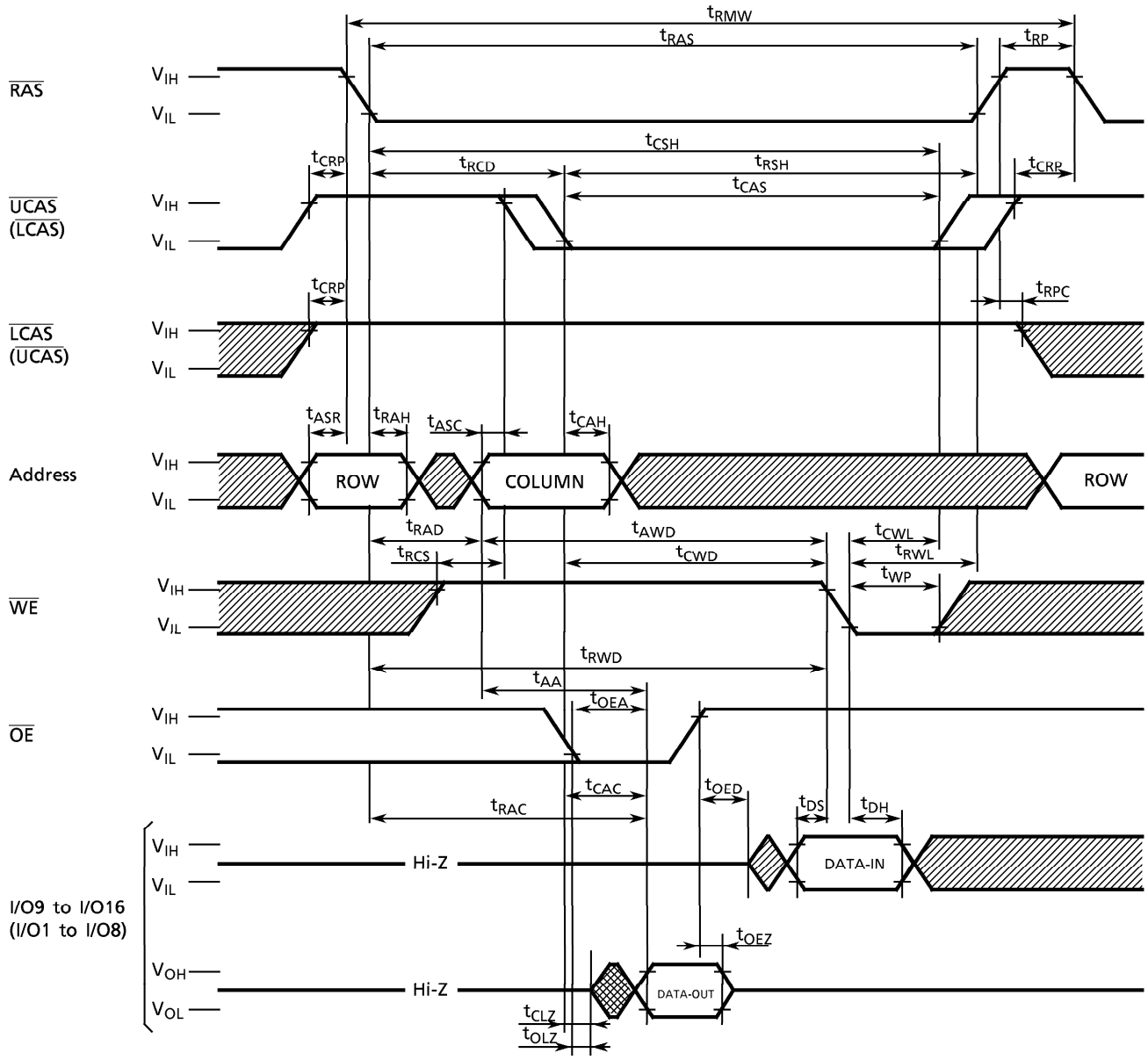
Note: D_{IN} (I/O1 to I/O8) = Don't Care
D_{OUT} = Hi-Z
(D_{IN} (I/O9 to I/O16) = Don't Care
D_{OUT} = Hi-Z)

: H or L

READ-MODIFY-WRITE CYCLE



BYTE READ-MODIFY-WRITE CYCLE

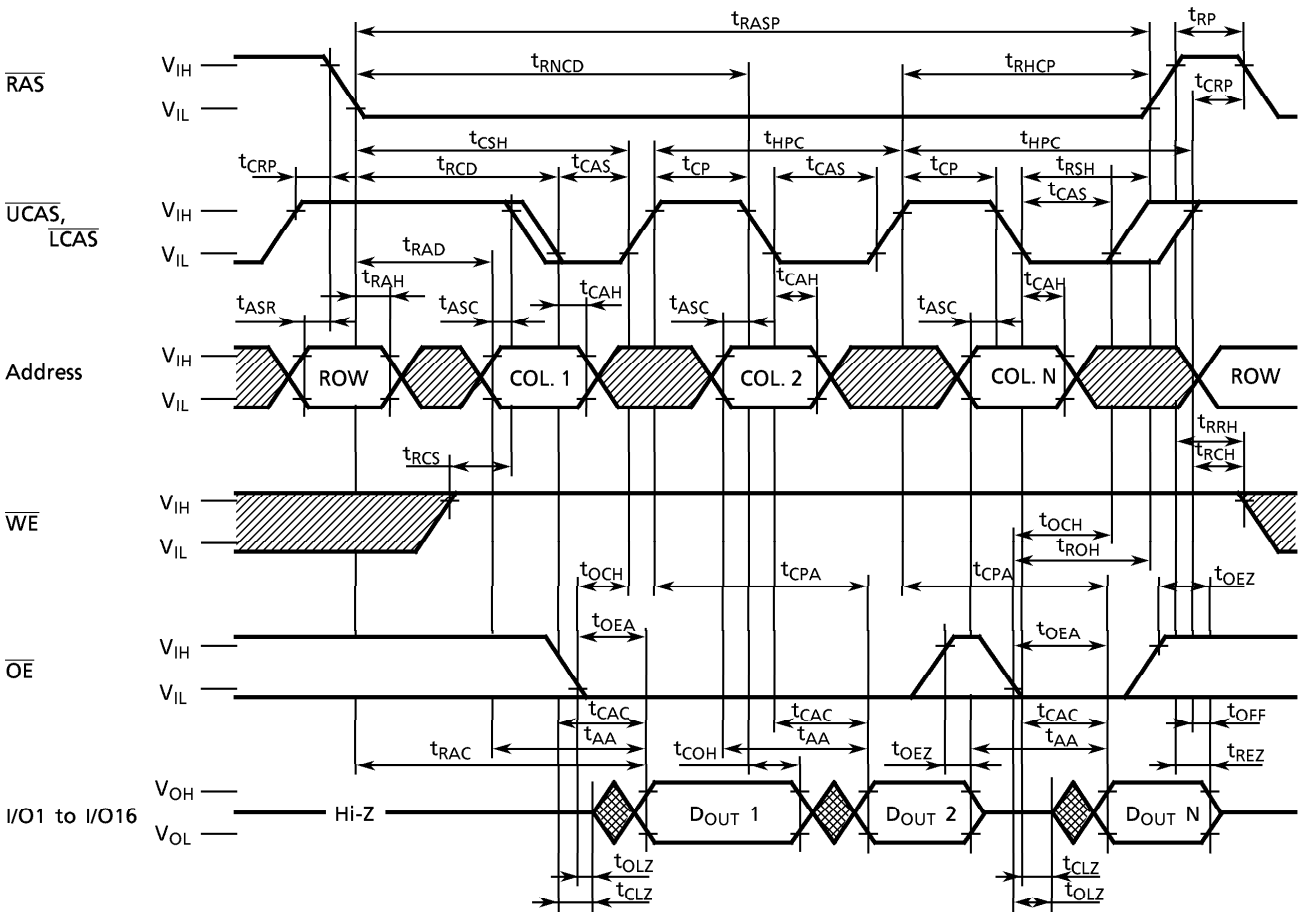


Note: D_{IN} (I/O1 to I/O8) = Don't Care
D_{OUT} (I/O1 to I/O8) = Hi-Z
(D_{IN} (I/O9 to I/O16) = Don't Care
D_{OUT} (I/O9 to I/O16) = Hi-Z)

: H or L

: Invalid Data

HYPER PAGE MODE READ CYCLE

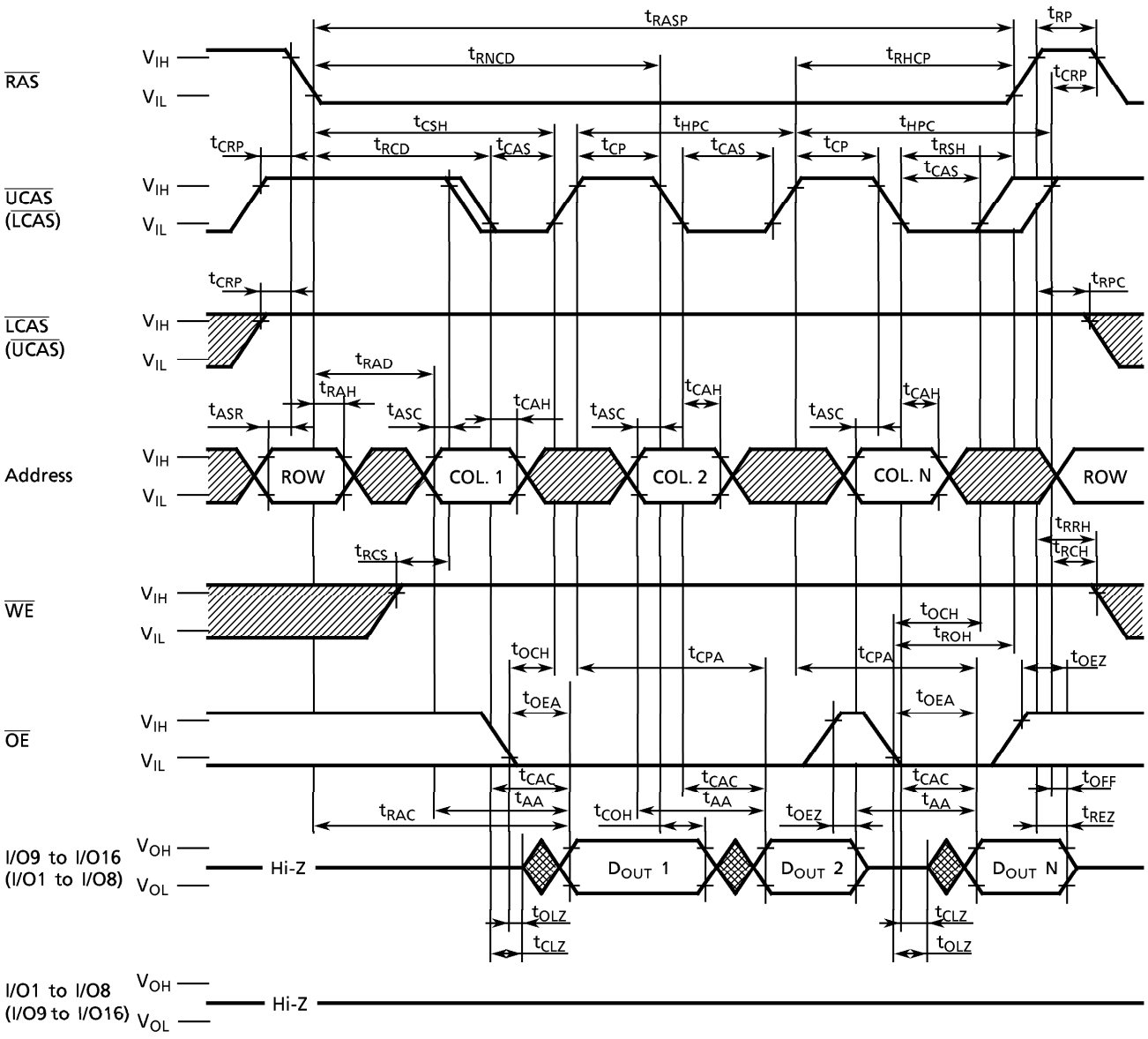


Note: D_{IN} = Hi-Z

: H or L

: Invalid Data

HYPER PAGE MODE BYTE READ CYCLE

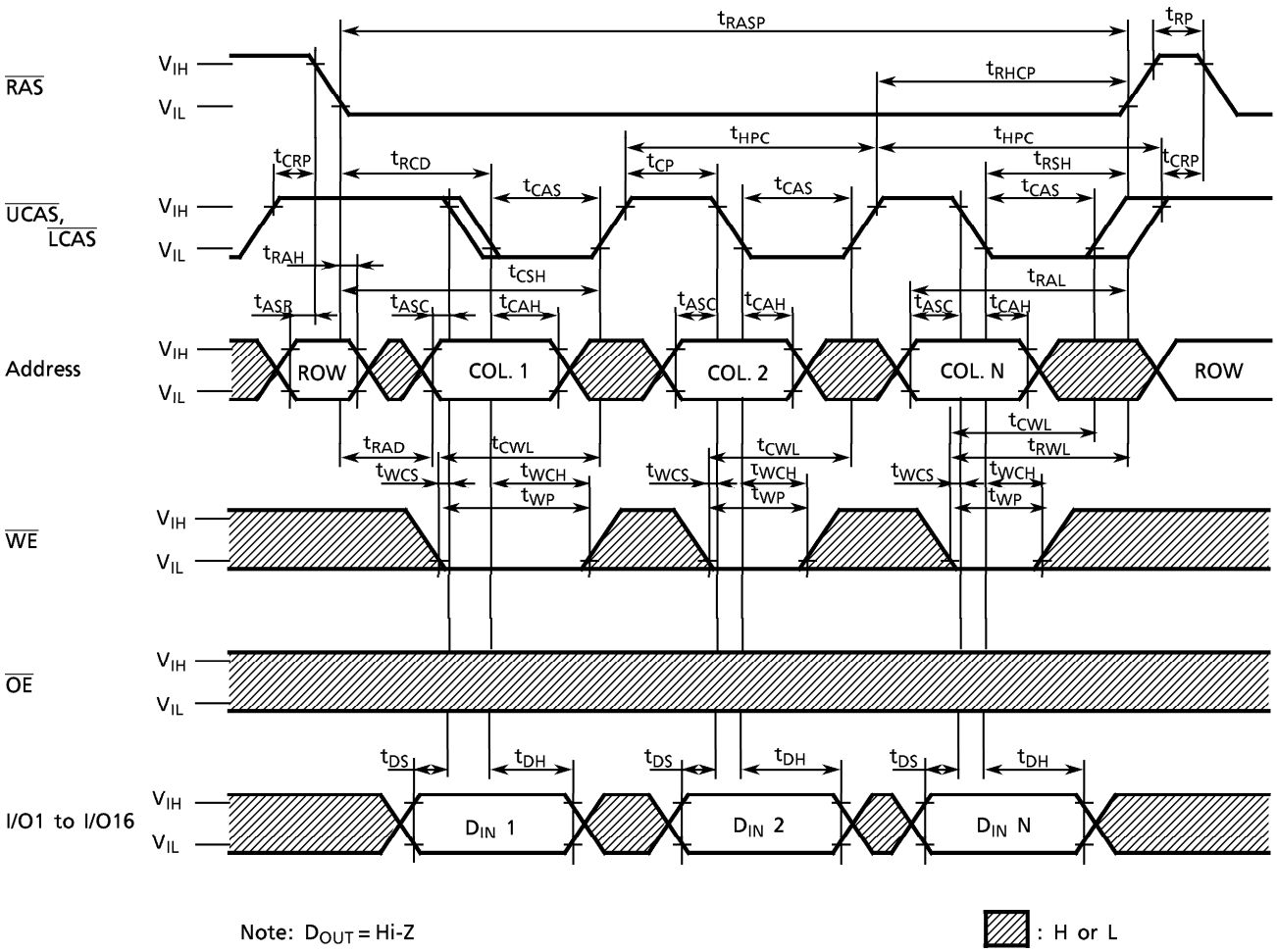


Note: D_{IN} (I/O1 to I/O8) = Don't Care
D_{OUT} (I/O9 to I/O16) = Hi-Z
(D_{IN} (I/O1 to I/O8) = Hi-Z
D_{OUT} (I/O9 to I/O16) = Don't Care)

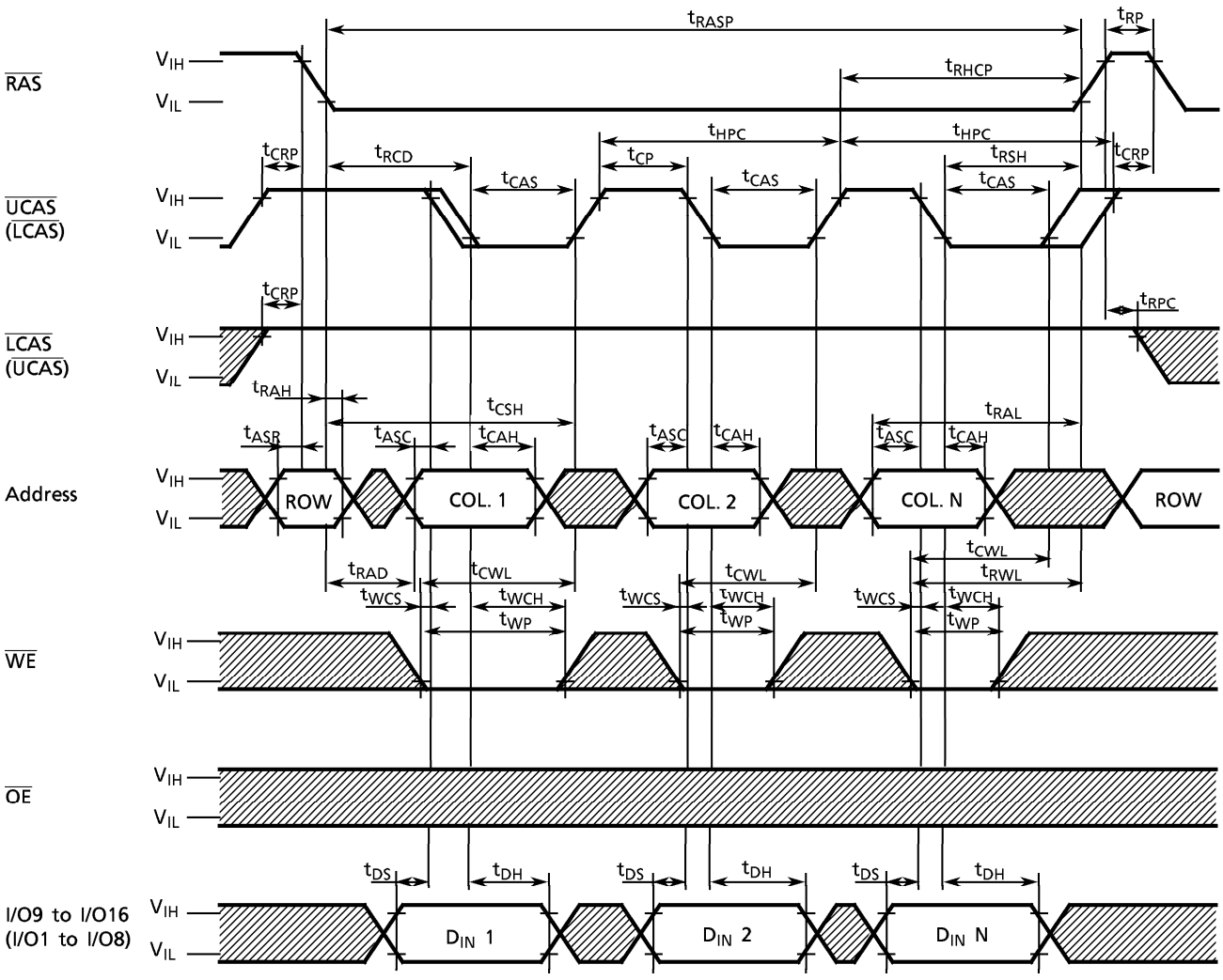
: H or L

: Invalid Data

HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)



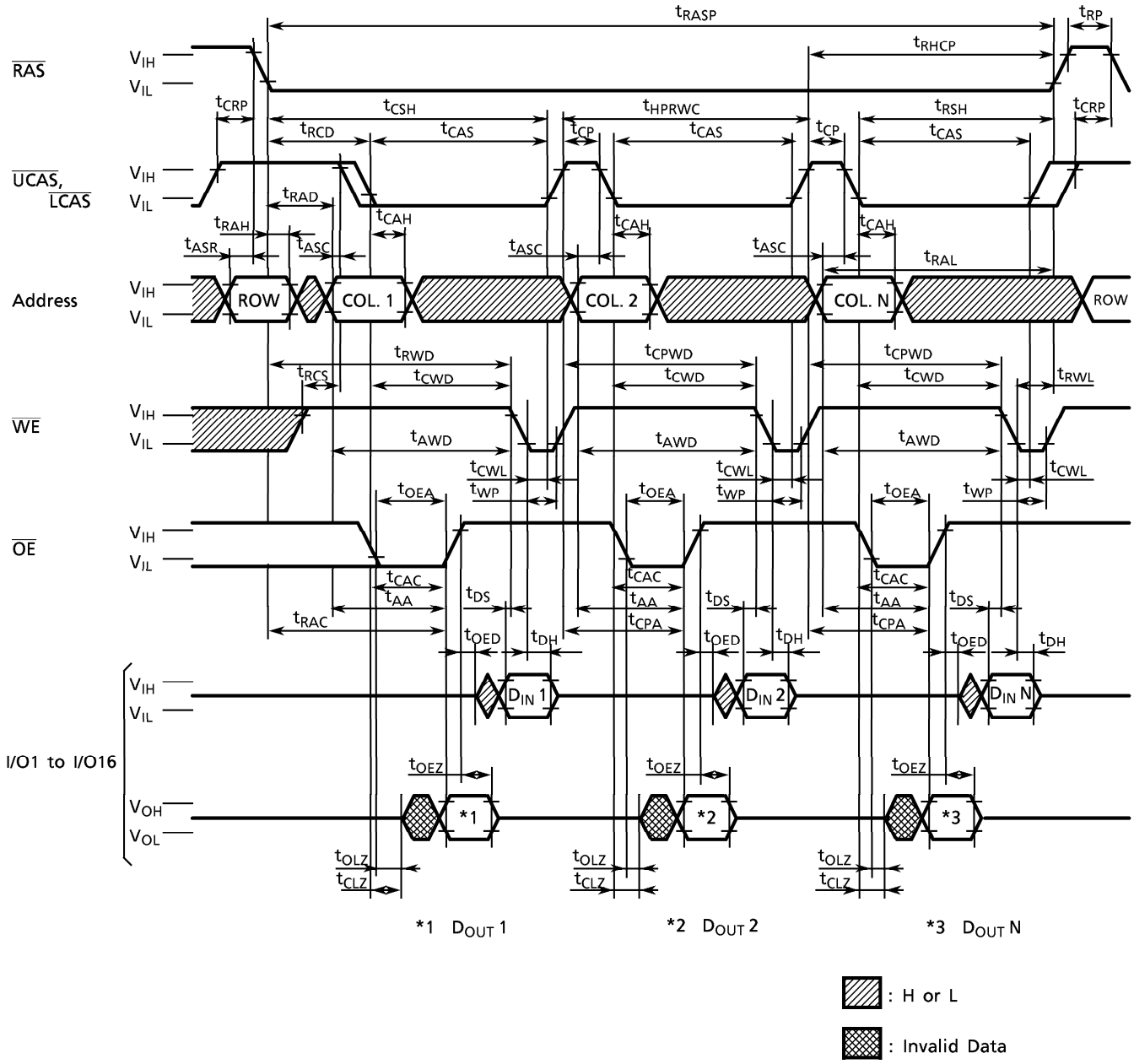
HYPER PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



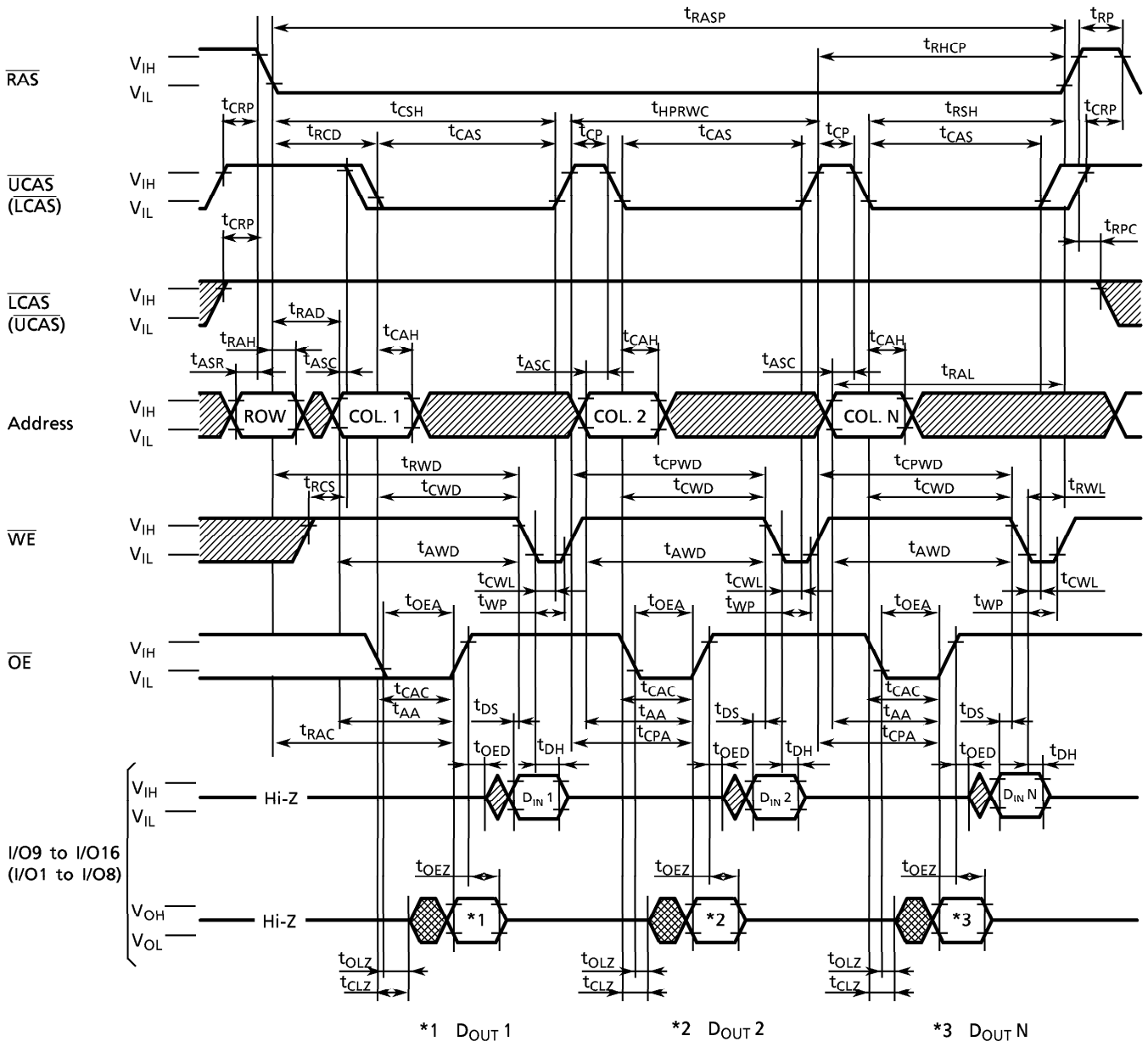
Note: D_{IN} (I/O1 to I/O8) = Don't Care
D_{OUT} = Hi-Z
(D_{IN} (I/O9 to I/O16) = Don't Care
D_{OUT} = Hi-Z)

: H or L

HYPER PAGE MODE READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE BYTE READ-MODIFY-WRITE CYCLE

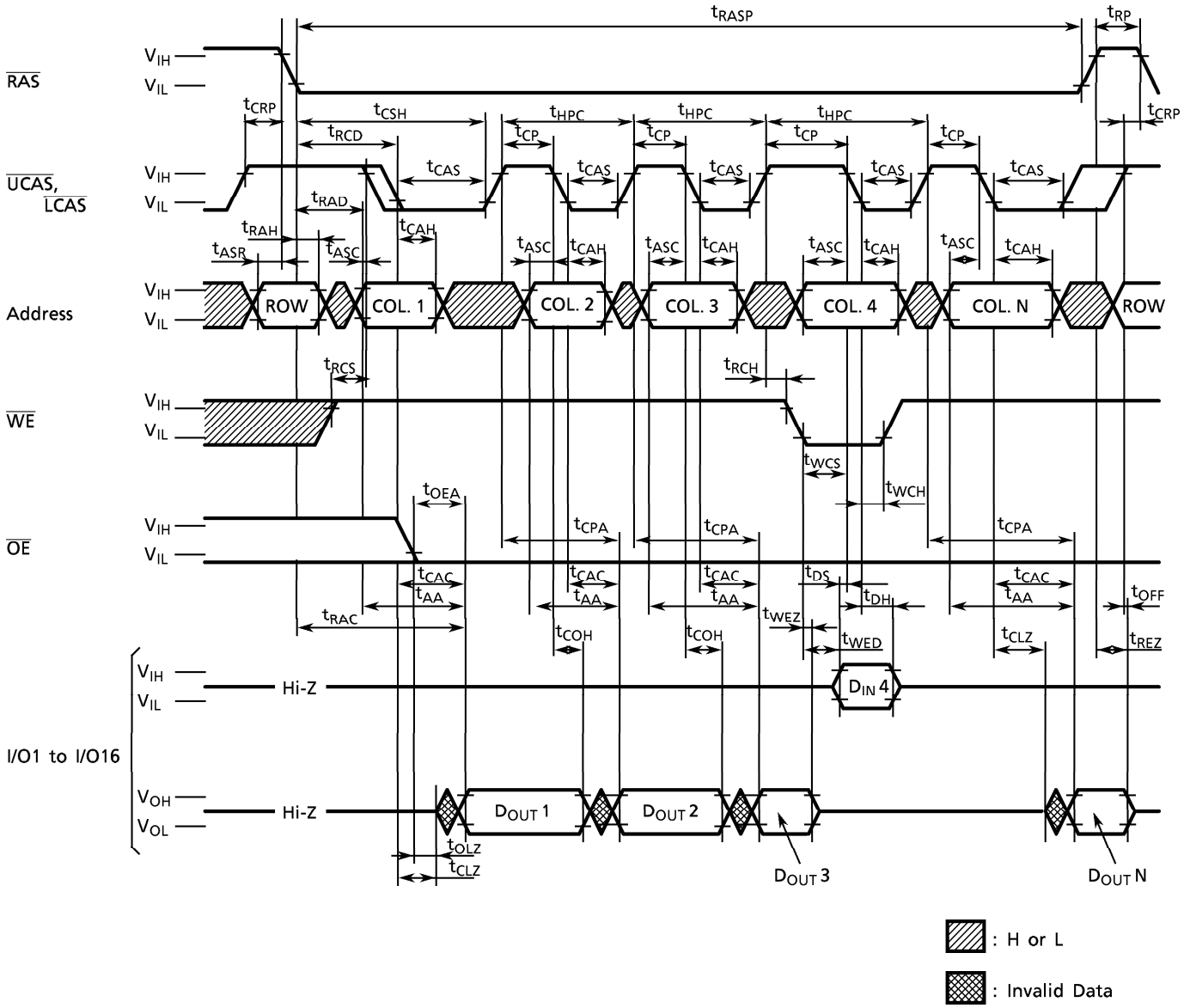


Note: D_{IN} (I/O1 to I/O8) = Don't Care
D_{OUT} (I/O1 to I/O8) = Hi-Z
(D_{IN} (I/O9 to I/O16) = Don't Care
D_{OUT} (I/O9 to I/O16) = Hi-Z)

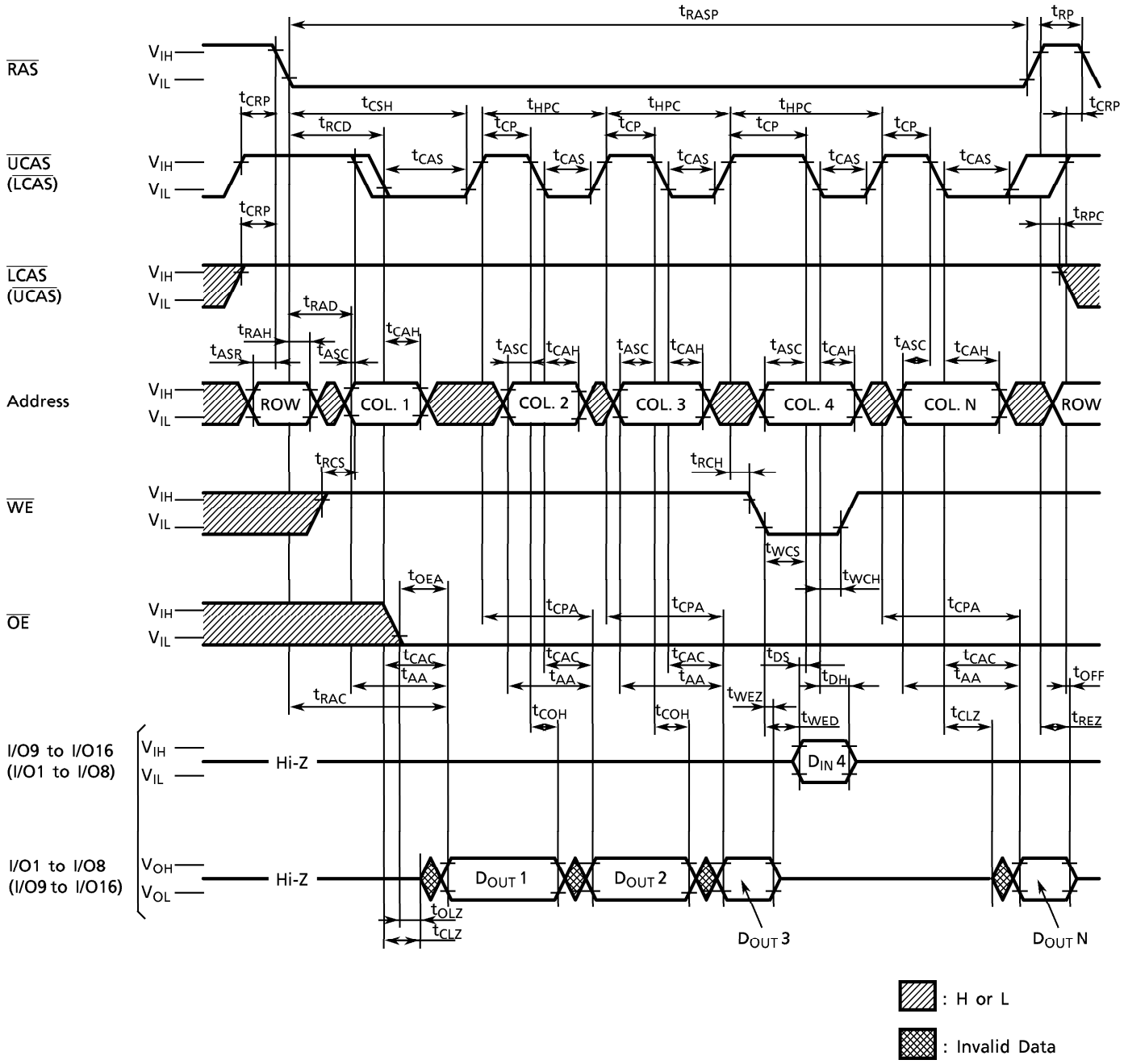
: H or L

: Invalid Data

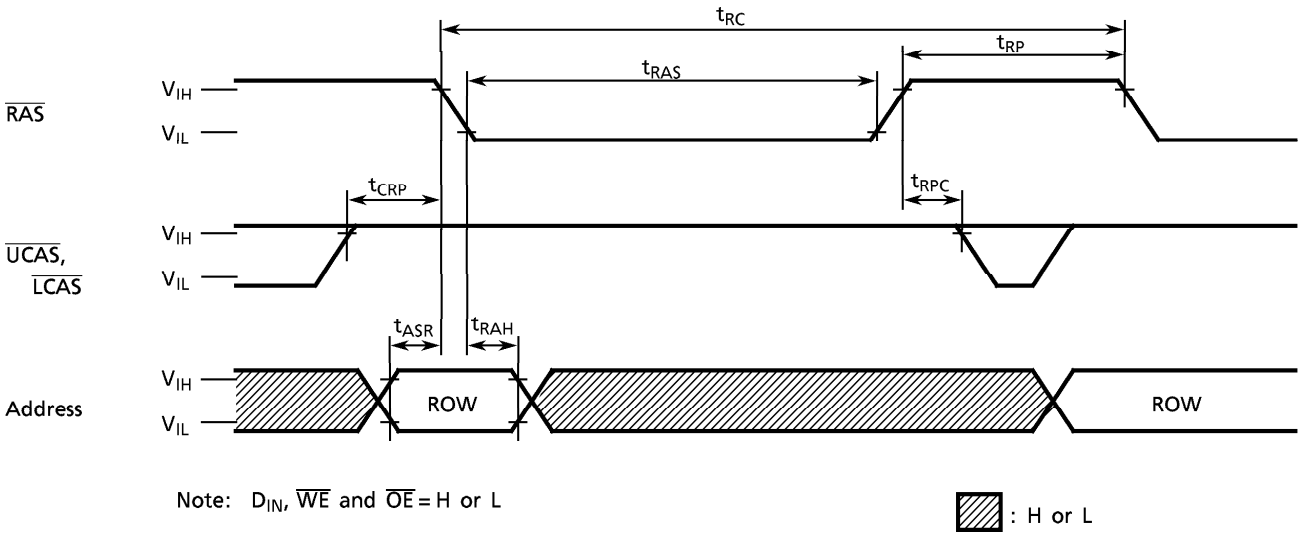
HYPER PAGE MODE READ-WRITE MIXED CYCLE



HYPER PAGE MODE BYTE READ-WRITE MIXED CYCLE



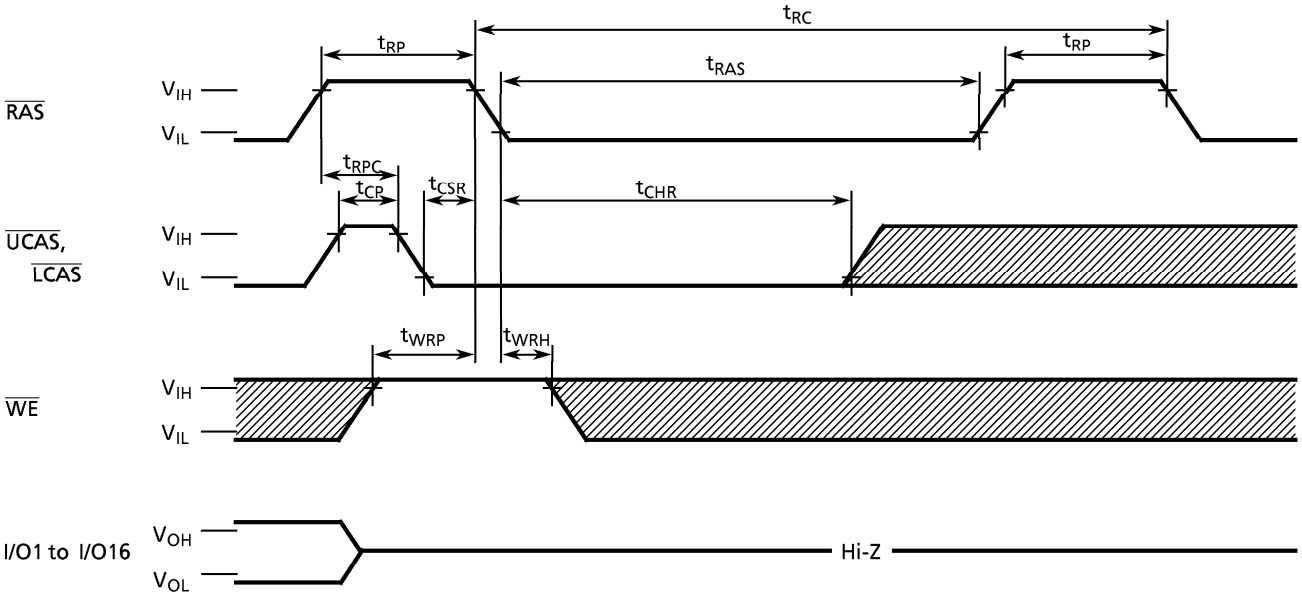
$\overline{RAS}$-ONLY REFRESH CYCLE



Note: D_{IN}, $\overline{WE}$ and $\overline{OE}$ = H or L

: H or L

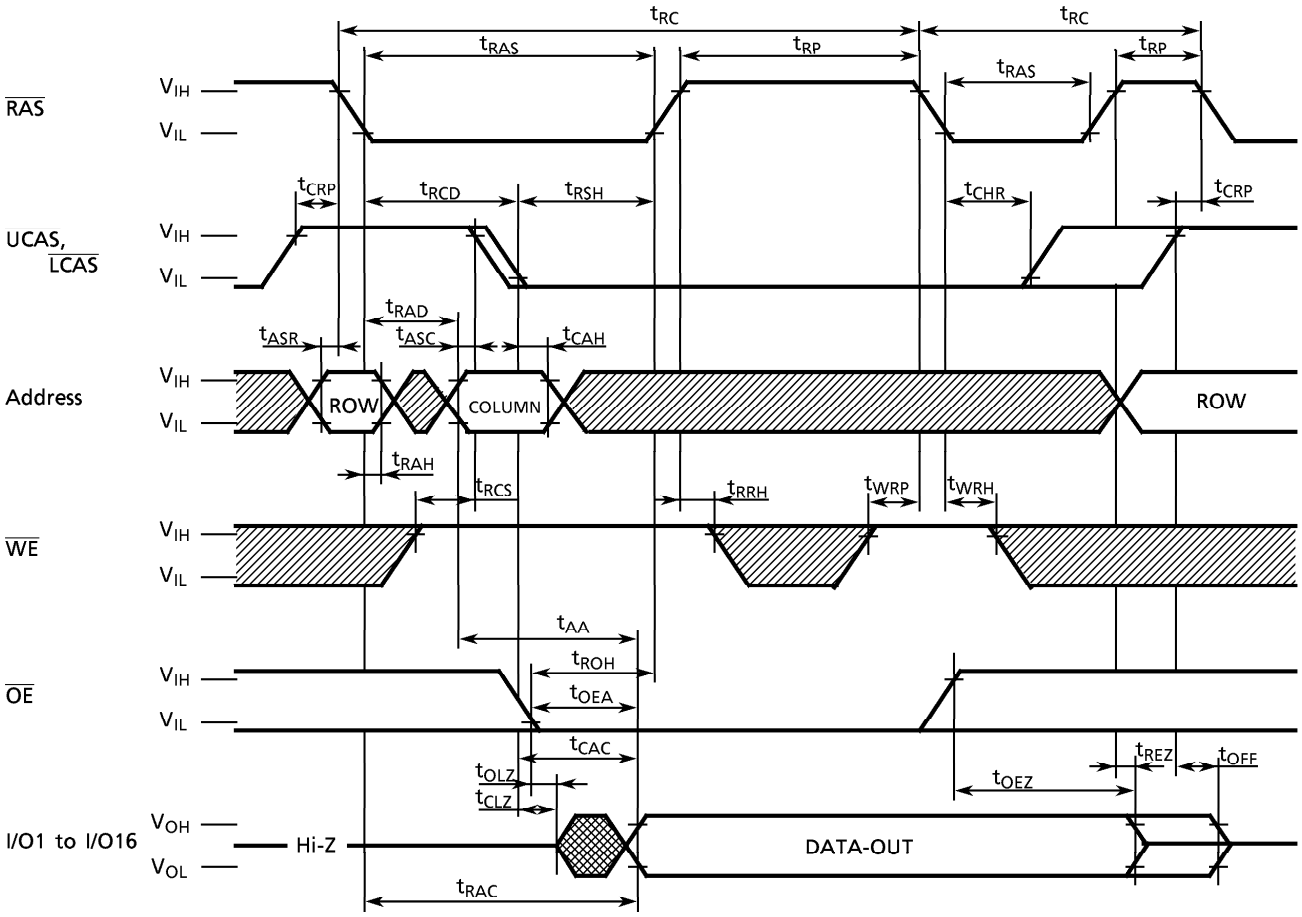
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



: H or L

Note: D_{IN}, $\overline{OE}$ and Address = H or L

HIDDEN REFRESH CYCLE (READ)

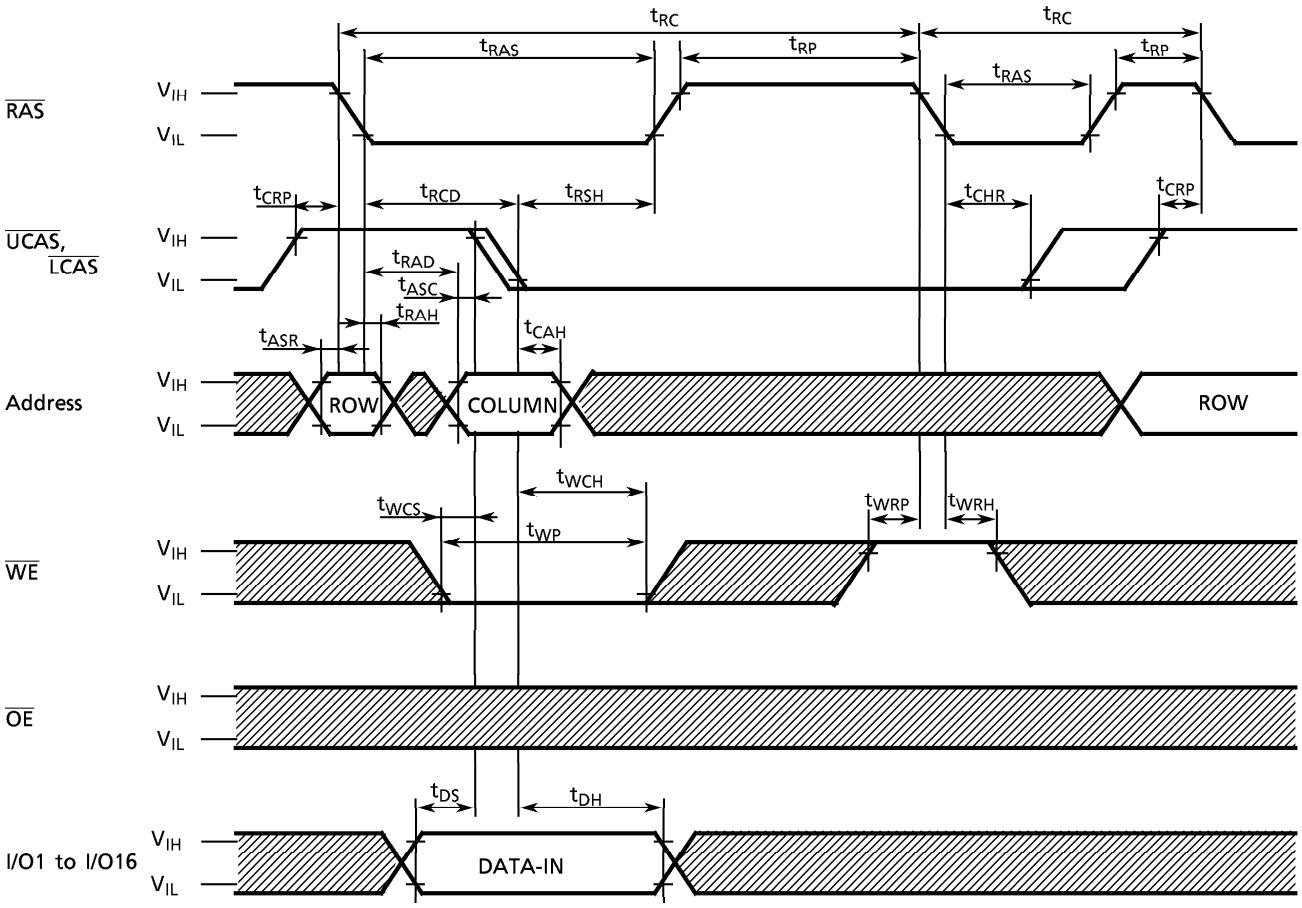


Note: D_{IN} = Hi-Z

: H or L

: Invalid Data

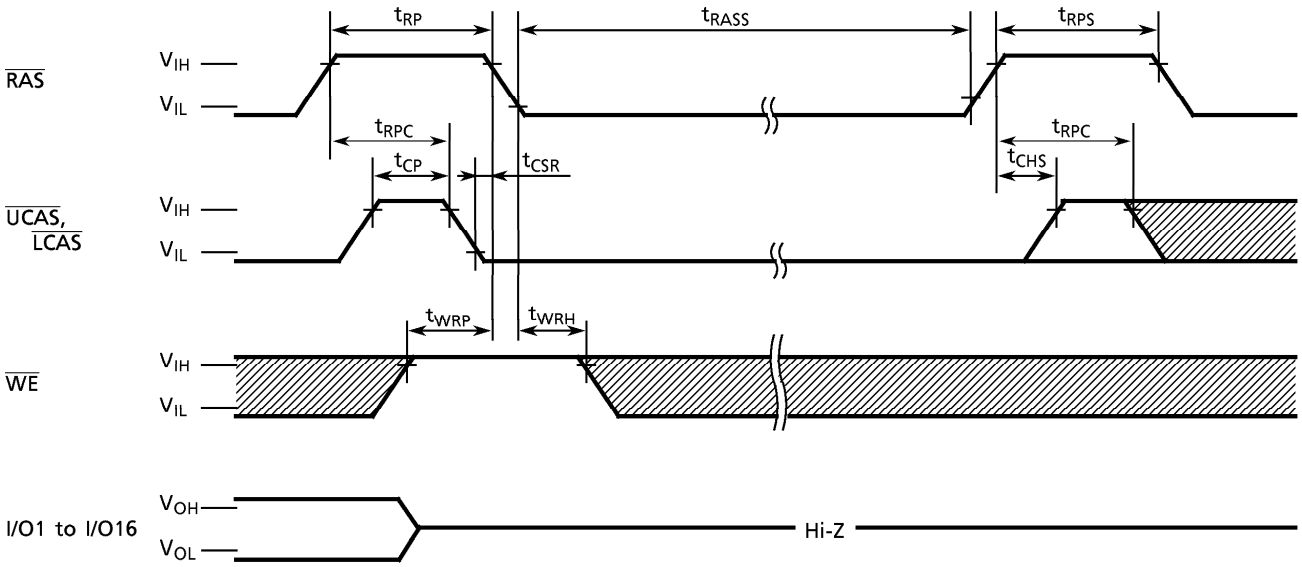
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = Hi-Z

▨ : H or L

$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ SELF-REFRESH CYCLE (S-version only)



Note: D_{IN}, $\overline{OE}$ and Address = H or L

▨ : H or L

PACKAGE DIMENSIONS (TSOPII 50 – P – 400 – 0.80D)

Unit: mm