+1.8V, Low Power, Quad-Input, 16-Bit $\Sigma - \Delta$ A/D Converter with a Power Fault Monitor

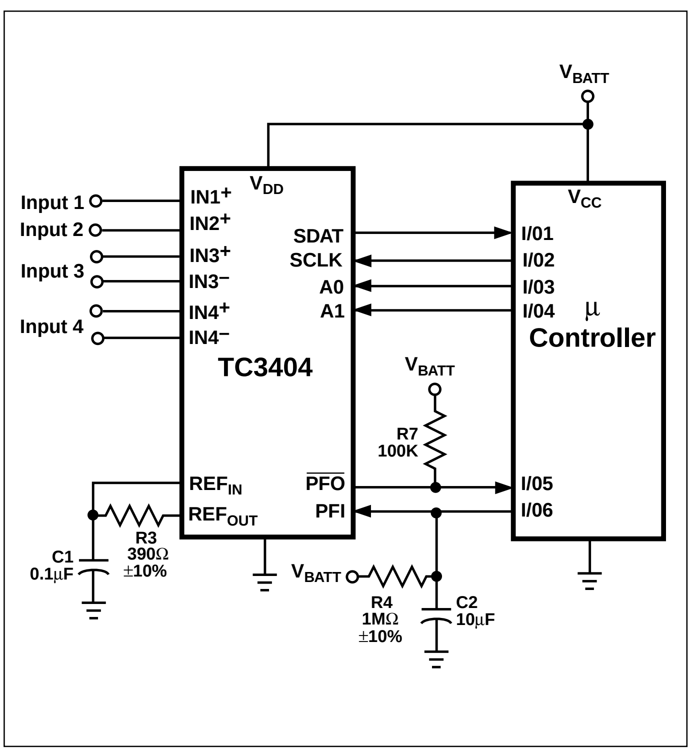
FEATURES

- **16-Bit Resolution at Eight Conversions Per Second, Adjustable Down to 10-Bit Resolution at 512 Conversions Per Second**
- **1.8V – 5.5V Operation, Low Power Operating .... 280µA .... Sleep: 37µA**
- **Two Differential and Two Single Ended Inputs with Built-In Multiplexer**
- **MicroPort™ Serial Bus Requires Only Two Interface Lines**
- **Uses Internal or External Reference**
- **Early Warning Power Fail Detector, Also Suitable as Wake-Up Timer Operational in Shutdown Mode**
- **Automatically Enters Sleep Mode When Not In Use**
- **16-Pin QSOP and PDIP Packages**

TYPICAL APPLICATIONS

- **Consumer Electronics, Thermostats, CO Monitors, Humidity Meters, Security Sensors**
- **Embedded Systems, Data Loggers, Portable Equipment**
- **Medical Instruments**

TYPICAL APPLICATION



GENERAL DESCRIPTION

The TC3404 is a low cost, low power analog-to-digital converter based on Microchip's Sigma-Delta technology. It will perform 16-bit conversions (15-bit plus sign) at up to eight per second. The TC3404 is optimized for use as a microcontroller peripheral in low cost, battery operated systems. A voltage reference is included, or an external reference can be used. Threshold detector is provided for use as an early warning power fail detector, or as a wake-up timer.

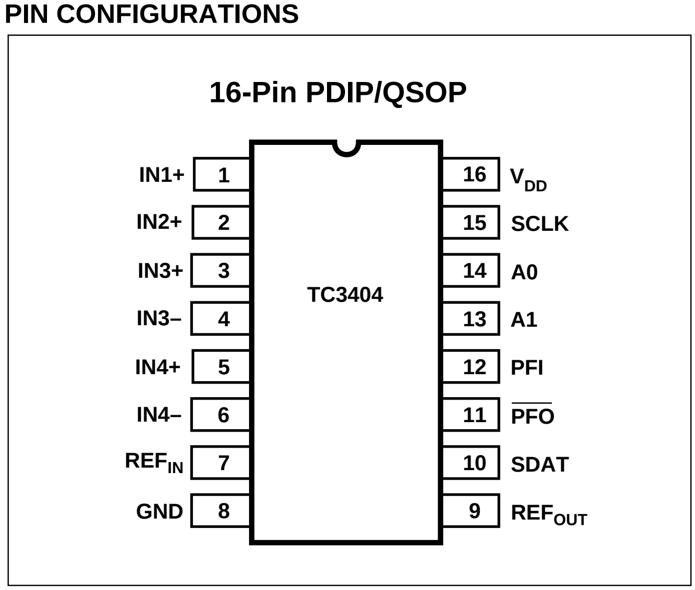
The TC3404's 2-wire MicroPort™digital interface is used for starting conversions and for reading out the data. Driving the SCLK line low starts a conversion. After the conversion starts, each additional falling edge (up to six) detected on SCLK for t4 seconds reduces the A/D resolution by one bit and cuts conversion time in half. After a conversion is completed, clocking the SCLK line puts the MSB through LSB of the resulting data word onto the SDAT line, much like a shift register. The part automatically sleeps when not performing a data conversion.

The TC3404 is available in 16-Pin PDIP and 16-Pin QSOP packages.

ORDERING INFORMATION

Part No.	Package	Temp. Range
TC3404VPE	16-Pin PDIP (Narrow)	0°C to +85°C
TC3404VQR	16-Pin QSOP (Narrow)	0°C to +85°C

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 6.0V
Voltage on Pins:
PFO .... (GND – 0.3V) to 5.5V
Input Voltage (All Other Pins) ....
.... (GND – 0.3V) to (V_{DD} + 0.3V)
Operating Temperature .... 0°C to 85°C
Maximum Chip Temperature .... +150°C
Storage Temperature Range .... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS: T_A = 25°C and V_{DD} = 2.7V, unless otherwise specified. Specifications in Bold type apply over a temperature range of 0°C to 85°C. V_{REF} =1.25V, Internal Clock Freq = 520kHz

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
V_{DD}	Supply Voltage		1.8	—	5.5	V
I_{DD}	Supply Current, During Data Conversion		—	280	—	µA
$I_{DD(SLEEP)}$	Supply Current, Sleep Mode	T_A = +25°C	—	37	50	µA
$I_{DD(SLEEP)}$			—	**46**	**60**	µA
ACCURACY						
RES	Resolution		—	16	—	Bits
INL	Integral Non-Linearity	V_{DD} = 2.7V	—	.0038	—	%FSR
V_{OS}	Offset Error	$IN^+ = IN^- = 0V$	—	—	±**1.0**	%FSR
V_{NOISE}	Refered to input		—	60	—	µVrms
CMR	Common Mode Rejection	at DC	—	75	—	dB
FSE	Full Scale Error		—	0.4%	—	%FS
PSRR	Power Supply Rejection Ratio	V_{DD} = 2.5V to 3.5V	—	75	—	dB
INn^+						
V_{IN}	Input Voltage	(Note 1)	—	—	V_{DD}	V
	Absolute Voltage Range INn		GND	—	V_{DD}	V
	Input Bias Current		—	1	100	nA
C_{IN}	Input Sampling Capacitance		—	2	—	pF
R_{IN}	Input Resistance	(Note 2)	—	2.0	—	MΩ
REF_{IN}, REF_{OUT}						
V_{REF}	REF_{IN} Voltage Range		0	—	1.25	V
I_{REF}	REF_{IN} Input Current		—	1	—	µA
V_{REFOUT}	REF_{OUT} Voltage		1.175	1.193	1,210	V
REF_{SINK}	REF_{OUT} Current Sink Capability		—	10	—	µA
REF_{SRC}	REF_{OUT} Current Source Capability		300	—	—	µA
SCLK, ADDR						
V_{IL}	Input Low Voltage		—	—	**0.3 x V_{DD}**	V
V_{IH}	Input High Voltage		**0.7 x V_{DD}**	—	—	V
I_{LEAK}	Leakage Current		—	1	—	µA

Notes: 1. Input voltage defined as (V_{IN}+ – GND or V_{IN}+ – V_{IN}–)
2. Resistance from INn+ to GND.

DC ELECTRICAL CHARACTERISTICS (CONT.): T_A = 25°C and V_{DD} = 2.7V, unless otherwise specified. Specifications in Bold type apply over a temperature range of 0°C to 85°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SDAT						
V_{OL}	Output Low Voltage	I_{OL} = 1.5mA	—	—	0.4	V
V_{OH}	Output High Voltage (SDAT)	I_{SOURCE} = 400µa (Note 2)	0.9 x V_{DD}	—	—	V
$V_{DD(MIN)}$	Minimum V_{DD} for $\overline{PFO}$, $\overline{RESET}$ Valid		—	1.1	1.3	V
V_{TH}						
V_{CCPFI}	PFI Input Voltage Range		0	—	V_{DD}	V
	V_{TH}, PFI Input Current		–0.1	.01	0.1	µa
V_{THR}	Threshold		—	1.23	—	V
	Threshold Hysteresis		—	30	—	mV

AC ELECTRICAL CHARACTERISTICS: T_A = 25°C and V_{DD} = 2.7V, unless otherwise specified. Specifications in Bold type apply over a temperature range of 0°C to 85°C. V_{REF} =1.25V, Internal Clock Freq = 520kHz

Symbol	Parameter	Description	Min	Typ	Max	Unit
t_1		Width of SCLK (Negative)	1	—	—	µsec
t_2	Resolution Reduction Clock Width	Width of SCLK (Positive)	1	—	—	µsec
t_3	Conversion Time (15-Bit Plus Sign)	16-bit conversion, T_A = 25° (Note 1)	—	125	—	msec
	Conversion Time (14-Bit Plus Sign)	15-bit conversion	—	t3/2.0	—	msec
	Conversion Time (13-Bit Plus Sign)	14-bit conversion	—	t3/4.0	—	msec
	Conversion Time (12-Bit Plus Sign)	13-bit conversion	—	t3/7.8	—	msec
	Conversion Time (11-Bit Plus Sign)	12-bit conversion	—	t3/15.1	—	msec
	Conversion Time (10-Bit Plus Sign)	11-bit conversion	—	t3/28.6	—	msec
	Conversion Time (9-Bit Plus Sign)	10-Bit conversion	—	t3/51.4	—	msec
t_4	Resolution Reduction Window	Width of SCLK	—	t3/85.7	—	msec
t_5	SCLK to Data Valid	SCLK falling edge to SDAT valid	**1000**	—	—	nsec
t_6	Address Setup	Address valid to SCLK	**0**	—	—	nsec
t_7	Address Hold	SCLK to address valid hold	**1000**	—	—	nsec
t_8	Acknowledge Delay	SCLK to SDAT delay	—	—	**1000**	nsec
t_{10}	$\overline{PFO}$ Delay	PFI to $\overline{PFO}$ delay	—	25	—	µsec

Notes: 1. Nominal temperature drift is -2830 ppm/°C for temperature less than 25°C and -1340 ppm/°C for temperatures greater than 25°C.
2. @V_{DD} =1.8V, $I_{SOURCE} \leq$ 200µa

PIN DESCRIPTION

TC3404 Pin No.	Name	Description
1,2	IN_n^+	Analog Input. This is the positive terminal of a true differential input with the negative input tied internally to GND. (See *Electrical Characteristics*.)
3,5	IN_n^+	Analog Input. This is the positive terminal of a true differential input consisting of INn^+ and INn^-. $V_{IN(n)} = (INn^+ - INn^-)$.(See *Electrical Characteristics*.)
4,6	IN_n^-	Analog Input. This is the negative terminal of a true differential input consisting of INn^+ and INn^- . $V_{IN(n)} = (INn^+ - INn^-)$ INn^- can swing to, but not below, ground. (See *Electrical Characteristics*.)
7	REF_{IN}	Analog Input. The converter's reference voltage is the differential between this pin and ground times two. It may be connected to REF_{OUT} as shown on page 1 or scaled using a resistor divider. Any user supplied reference voltage or the power supply rail may be used in place of REF_{OUT}.
8	GND	Ground Terminal.
9	REF_{OUT}	Analog Output. The internal reference connects to this pin. It may be scaled externally, if desired, and tied to the REF_{IN} input to provide the converter's reference voltage. Care must be taken in connecting external circuitry to this pin. (See *Electrical Characteristics*.)
10	SDAT	Digital Output (push-pull). This is the MicroPort™ serial data output. SDAT is driven low while the TC3404 is converting data, effectively providing a "busy" signal. After the conversion is complete, every high-to-low transition on the SCLK pin puts a bit from the resulting data word on the SDAT pin (from MSB to LSB).
11	$\overline{PFO}$	Digital Output (open drain). This is the output of the internal threshold detector. When PFI is less than the internal reference, $\overline{PFO}$ is driven low.
12	PFI	Analog Input. This is the positive input to an internal comparator used as a threshold detector. The negative input is tied to an internal reference.
13	A1	Digital Input. Controls analog multiplexer in conjunction with A0 to select one of the four Input channels. This address is latched at the falling edge of the SCLK, which starts an A/D conversion. A1,A0 = 00 = Input 1; 01 = Input 2; 10 = Input 3; 11 = Input 4.
14	A0	Digital Input. Controls analog multiplexer in conjunction with A1 to select one of four Input channels. This address is latched at the falling edge of the SCLK, which starts an A/D conversion. A1,A0 = 00 = Input 1; 01 = Input 2; 10 = Input 3; 11 = Input 4.
15	SCLK	Digital Input. This is the MicroPort™ serial clock input. After the conversion starts, each additional falling edge (up to six) detected on SCLK for t4 seconds reduces the A/D resolution by one bit. When the conversion is complete, the data word can be shifted out on the SDAT pin by clocking the SCLK pin.
16	V_{DD}	Power Supply Input. (See *Electrical Characteristics*.)

GENERAL THEORY OF OPERATION

The TC3404 is a 16-bit sigma-delta A/D converter.It has two differential single-ended inputs, an analog multiplexer, and an early warning power fail detector. The detailed description of the key components of the TC3404 is outlined below. (Also refer to the A/D Operational Flowchart on page 10 and the Timing Diagrams in Figures 2 through 5).

A/D Converter Operation

When the TC3404 is not converting, it is in sleep mode with both the SCLK and SDAT lines high. An A/D conversion is initiated by a high to low transition on the SCLK line at which time the internal clock of the TC3404 is started and the address value (A0 and A1) is internally latched. The address value steers the analog multiplexer to select the input channel to be converted. Each additional high to low transition of SCLK (following the initial SCLK falling edge) and during the time interval t4 will decrement the conversion accuracy by one bit and reduce the conversion time by one half. The time interval t4 is referred to as the resolution reduction window. The minimum conversion resolution is 10 bits so any more than 6 SCLK transitions during t4 will be ignored.

After each high to low transition of SCLK, in the t4 interval, the SDAT output is driven high by the TC3404 to acknowledge that the conversion has been decremented. When the SCLK returns high or the t4 interval ends, the SDAT line returns low (see Figure 2). When the conversion is complete SDAT is driven high. The 3404 now enters sleep mode and the conversion value can be read as a serial data word on the SDAT line.

Reading the Data Word

After the conversion is complete and SDAT goes high, the conversion value can be clocked serially onto the SDAT line by high to low transitions of the SCLK. The data word is in two's compliment format with the sign bit clocked onto the SDAT line first followed by the MSB and ending in the LSB. For a 16 bit conversion the data word would consist of a sign bit followed by 15 magnitude bits, Table 1 shows the data word versus input voltage for a 16 bit conversion. Note that the full scale input voltage range is $\pm(2\,REF_{IN} - 1LSB)$. When REF_{OUT} is fed back directly to REF_{IN}, an LSB is 73µV for a 16 bit convertion, as REF_{OUT} is typically 1.193V.

Figure 3 shows typical SCLK and SDAT waveforms for 16, 12 and 10 bit conversions. Note that any complete convert and read cycle requires 17 negative edge clock pulses. The first is the convert command. Then, up to six of these can occur in the resolution reduction window, t4, to decrement accuracy. The remaining pulses clock out the conversion data word.

Table 1. Data Conversion Word vs. Voltage Input (REF_{IN} = 1.193V)

Data Word	$INn^+ - INn^-$ (Volts)
0111 1111 1111 1111	2.38596 (Positive Full Scale)
0000 0000 0000 0001	72.8 E – 6
0000 0000 0000 0000	0
1111 1111 1111 1111	–72.8 E – 6
1000 0000 0000 0001	–2.38596 (Negative Full Scale)
1000 0000 0000 0000	Reserved Code

The SCLK input has a filter which rejects any positive or negative pulse of width less than 50ns to reduce noise. The rejection width of this pulse can vary between 50ns and 750ns depending on processing parameters and supply voltage.

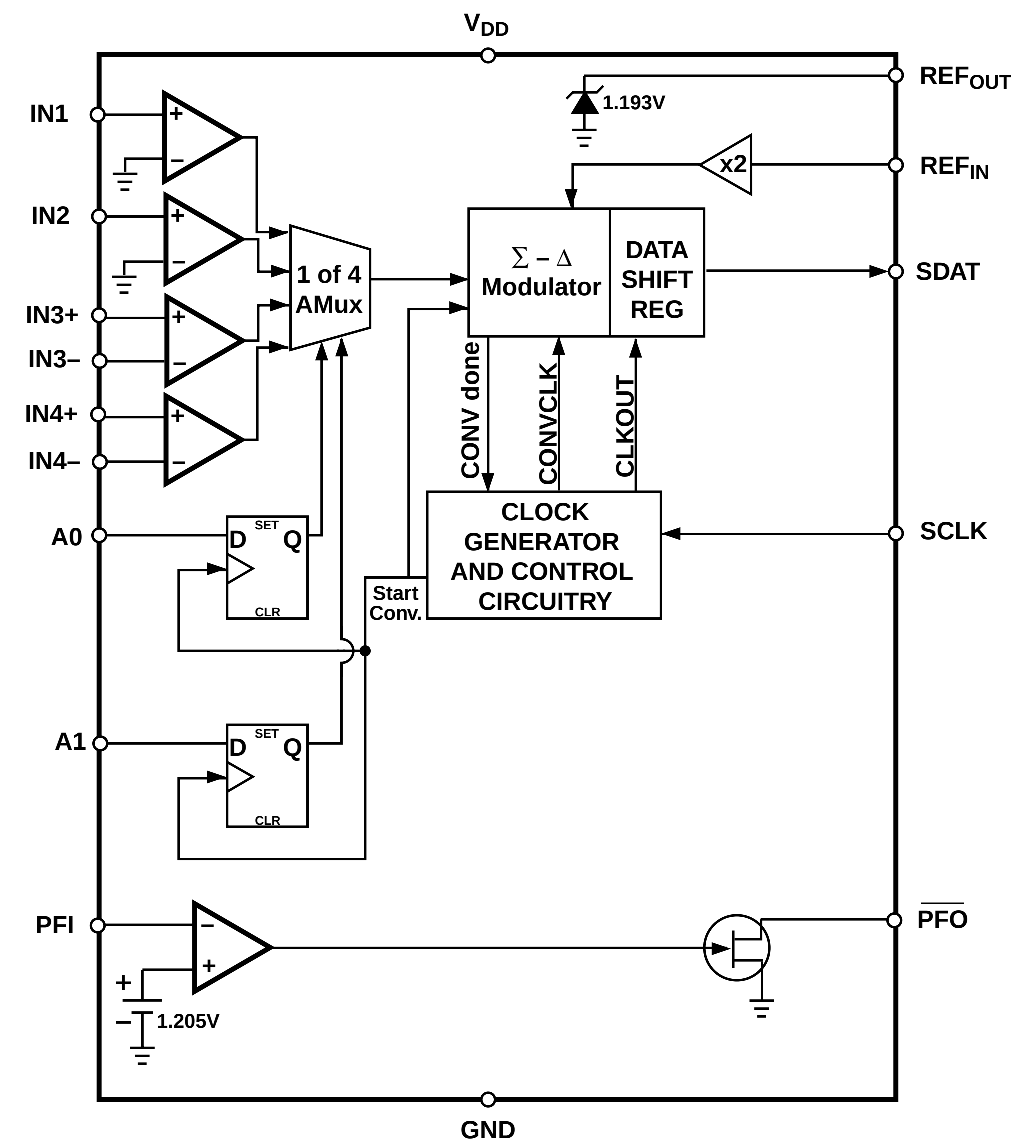
Figure 3 shows a truth table for determining the mode of operation for the TC3404 part by recording the value of SDAT for SCLK in a high, then low, then high state. For example, if SCLK goes through a 1-0-1 transition and the corresponding values of SDAT are 1-1-0, then the SCLK falling edge started a new data conversion. A 0-1-0 for SDAT would have indicated a resolution reduction had occurred. This is useful if the microcontroller has a watchdog reset or otherwise loses track of where the TC3404 part is in the conversion and data readout sequence. The microcontroller can simply transition SCLK until it "finds" a Start Conversion condition.

Power Fail Detector

The power fail detector is a comparator in which the inverting input is connected to the internal voltage reference, the non-inverting input is the PFI pin of the TC3404 and the PFO pin is the active low, open collector output. This comparator is suitable as an early warning fail or low battery indicator. In a typical application, where a voltage regulator is being used to supply power to a system, the power fail comparator would monitor the input voltage to the regulator while the V_{DD} monitor would measure the output voltage of the regulator. PFO would drive the interrupt pin of a microcontroller.

The Power Fail detector, may be used as a Wake-up or Watch-dog Timer. The Typical Application Circuit on Page 1 shows an RC network on PFI with the capacitor tied to a tri-stated µC I/O pin. If R4 is 1 MΩ and C2 is 10µF, the time constant is roughly ten seconds. The µC resets the RC network by driving the I/O tied to PFI low and then tri-stating it. The RC network will ramp to 1.23V in roughly 9 seconds, assuming a V_{BATT} of 3.0V. With $\overline{PFO}$ tied to a µC input or interrupt, the µC will see a low-to-high transition on $\overline{PFO}$ when voltage on PFI exceeds 1.23V. The $\overline{PFO}$ output is guaranteed to be valid for V_{DD} = 1.3 to 5.5V.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAMS

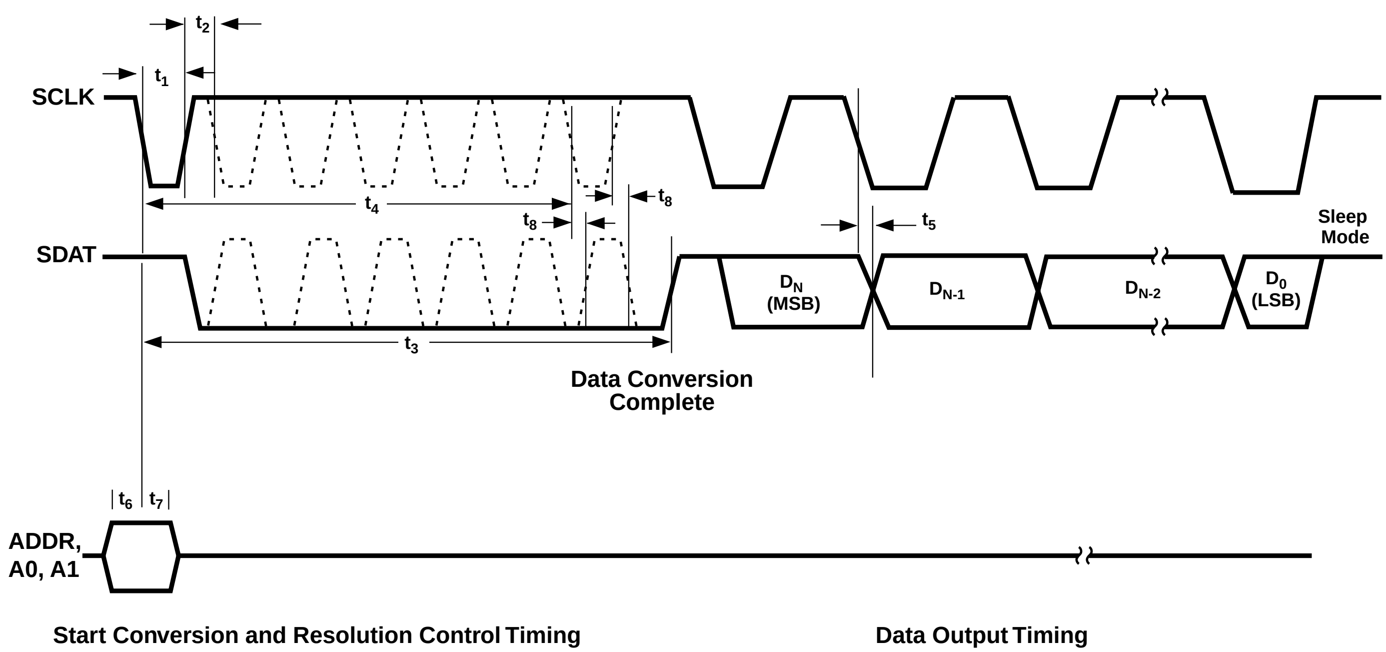
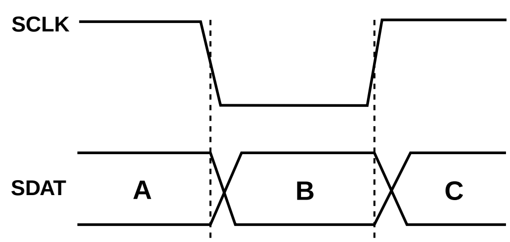


Figure 2. Conversion and Data Output Timing



A	B	C	Status
1	1	0	Start Conversion
0	1	0	Resolution Reduction
x	1	1	Data Transfer
x	0	0	Data Transfer or Busy*
x	0	1	Data Transfer of LSB

*Note: The code x00 has a dual meaning: Data Transfer or Busy Converting.To avoid confusion, the user should send only the required number of pulses for the desired resolution, then wait for SDAT to rise to 1, indicating conversion complete before clocking SCLK again to read out data bits.

Figure 3. SCLK, SDAT Logic State Table

TIMING DIAGRAMS (CONT.)

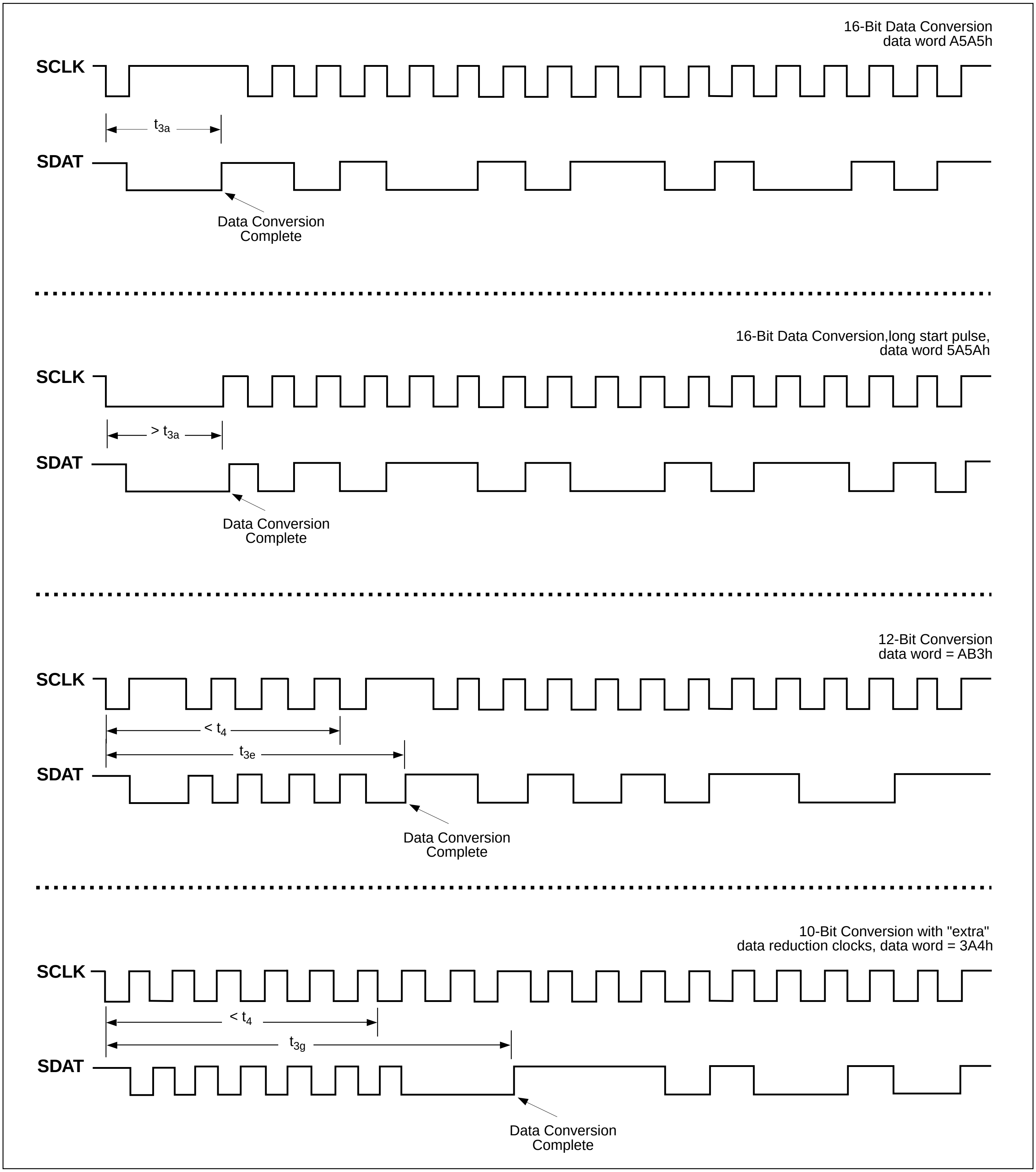


Figure 4. Example Timing Diagrams

TIMING DIAGRAMS (CONT.)

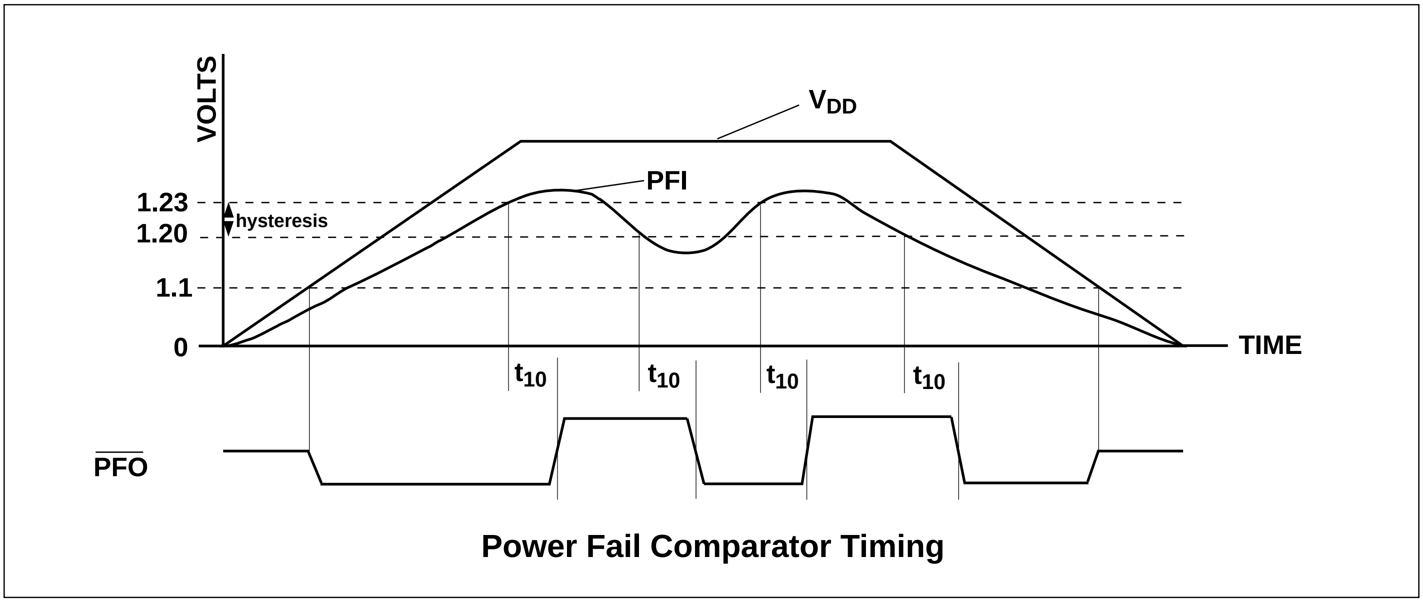
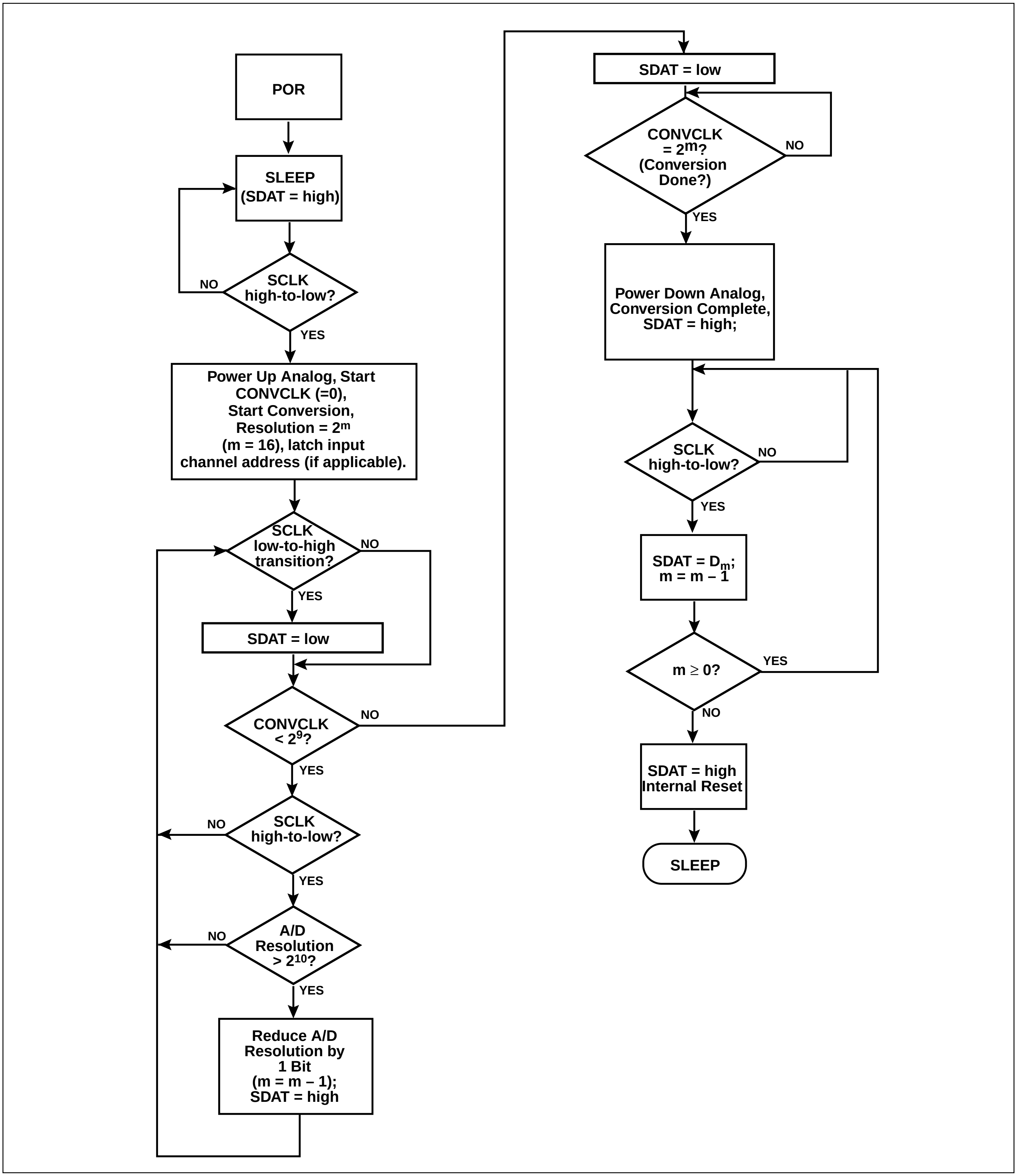
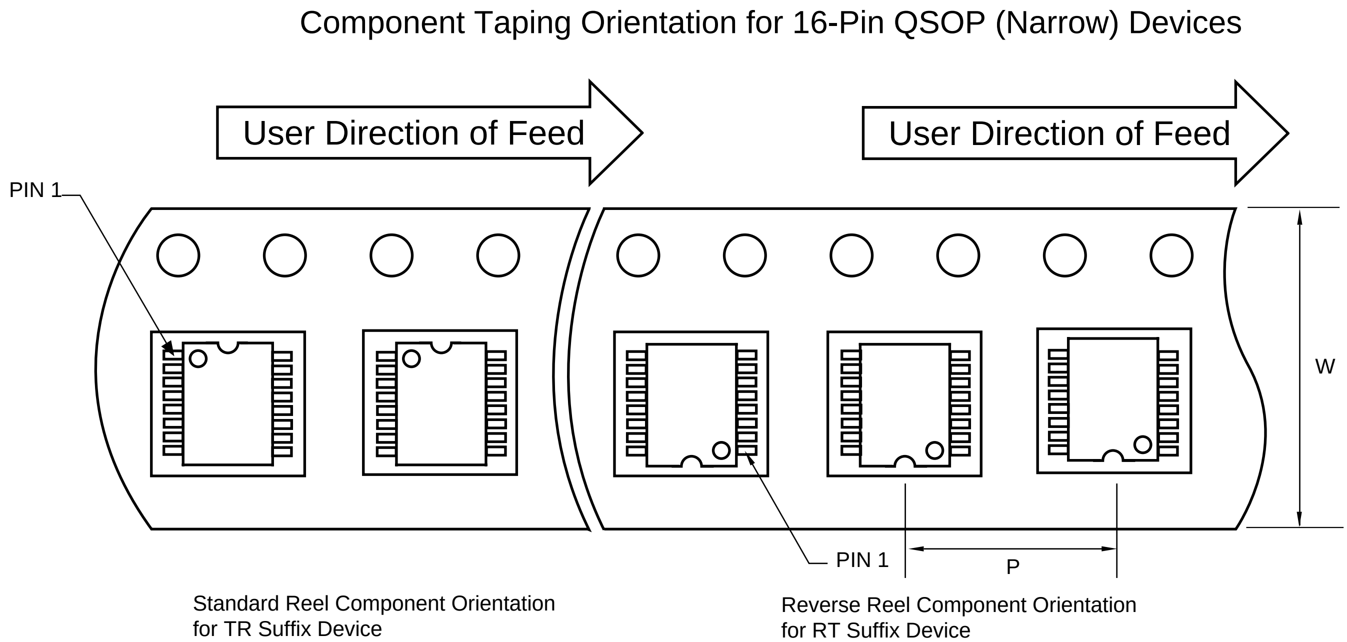


Figure 5. Power Fail Timing

A/D OPERATIONAL FLOWCHART



TAPING FORM

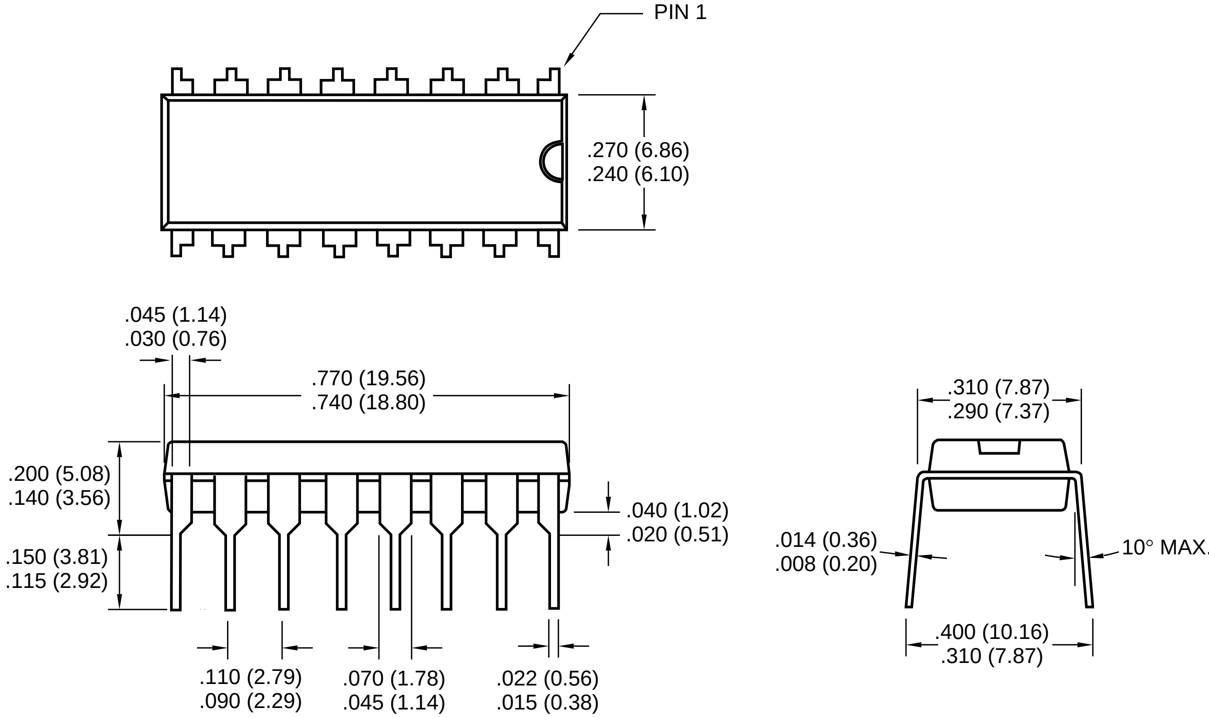


Carrier Tape, Reel Size, Number of Components Per Reel and Reel Size

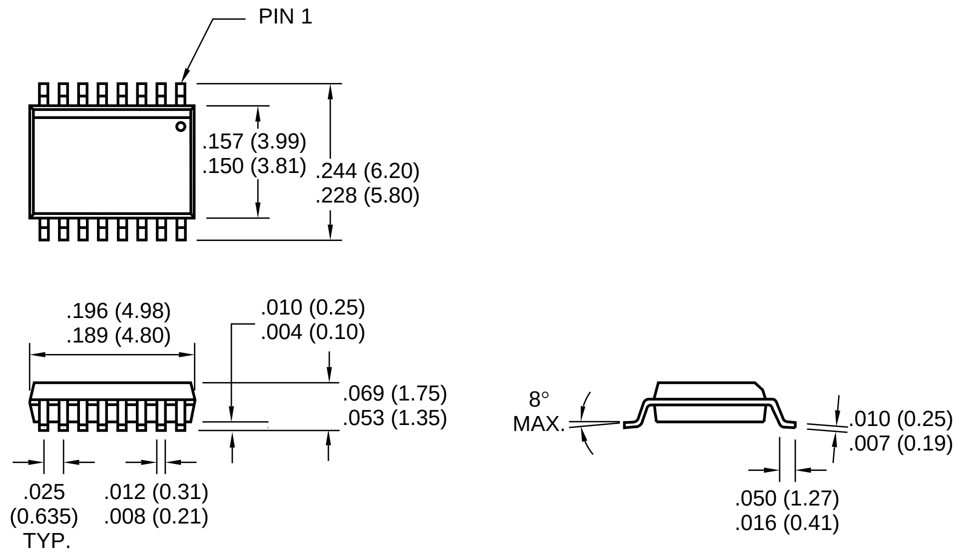
Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
16-Pin QSOP (N)	12 mm	8 mm	2500	13 in

PACKAGE DIMENSIONS

16-Pin PDIP (Narrow)



16-Pin QSOP (Narrow)



DImensions: inches(mm)

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