100mA Charge Pump Voltage Converter with Shutdown

FEATURES

- Optional High-Frequency Operation Allows Use of Small Capacitors
- Low Operating Current (FC = GND) 50µA
- High Output Current 100mA
- Converts a 2.4V to 5.5V Input Voltage to a Corresponding Negative Output Voltage (Inverter Mode)
- Uses Only 2 Capacitors; No Inductors Required!
- Selectable Oscillator Frequency .... 10kHz to 200kHz
- Power-Saving Shutdown Input
- Small Packages .... 8-Pin MSOP, 8-Pin PDIP, 8-Pin SOIC

APPLICATIONS

- Laptop Computers
- Medical Instruments
- Disk Drives
- µP-Based Controllers
- Process Instrumentation

ORDERING INFORMATION

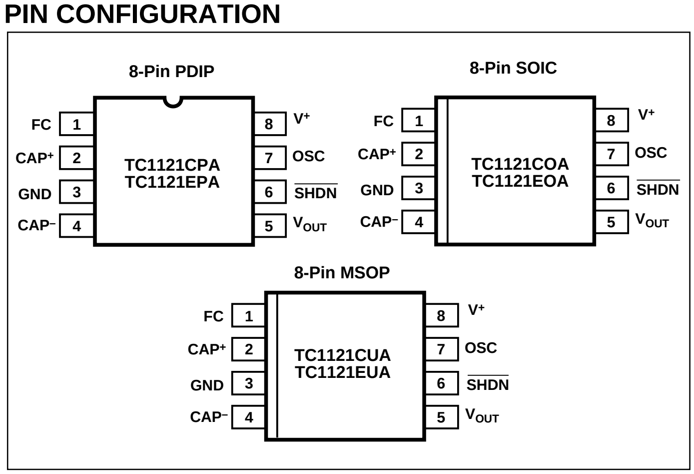
Part No.	Package	Temp. Range
TC1121COA	8-Pin SOIC	0°C to +70°C
TC1121CPA	8-Pin PDIP	0°C to +70°C
TC1121CUA	8-Pin MSOP	0°C to +70°C
TC1121EOA	8-Pin SOIC	– 40°C to +85°C
TC1121EPA	8-Pin PDIP	– 40°C to +85°C
TC1121EUA	8-Pin MSOP	– 40°C to +85°C

GENERAL DESCRIPTION

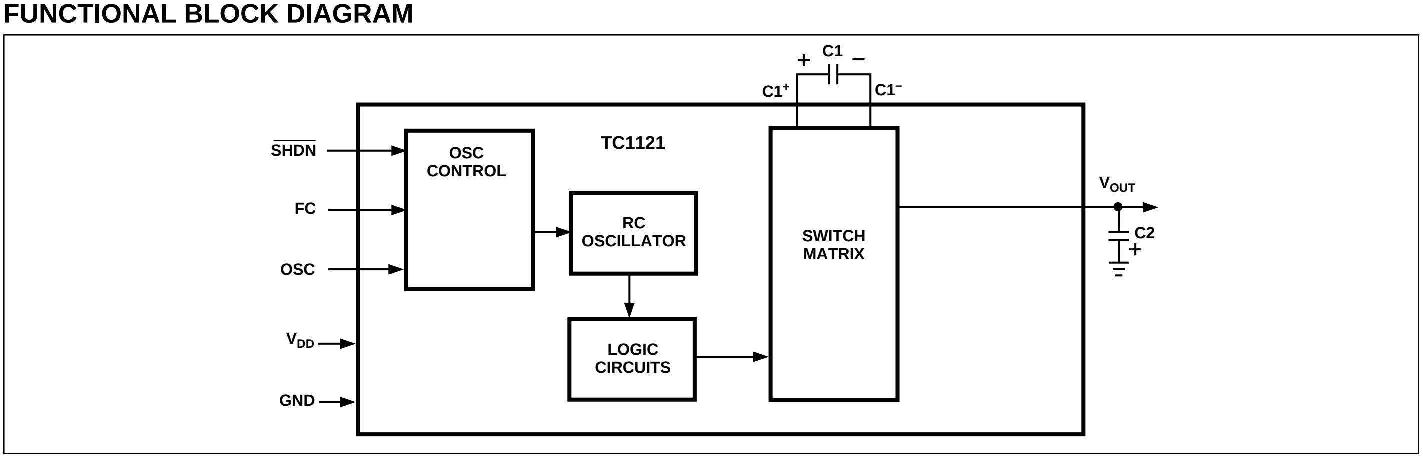
The TC1121 is a charge pump converter with 100mA output current capability. It converts a 2.4V to 5.5V input to a corresponding negative output voltage. As with all charge pump converters, the TC1121 uses no inductors saving cost, size, and EMI.

An on-board oscillator operates at a typical frequency of 10kHz (at V^+ = 5V) when the frequency control input (FC) is connected to ground. The oscillator frequency increases to 200kHz when FC is connected to V^+, allowing the use of smaller capacitors. Operation at sub-10kHz frequencies results in lower quiescent current and is accomplished with the addition of an external capacitor from OSC (pin 7) to ground. The TC1121 also can be driven from an external clock connected OSC. Typical supply current at 10kHz is 50µA, and falls to less than 1µA when the shutdown input is brought low, whether the internal or an external clock is used. The TC1121 is available in 8-pin SOIC, MSOP, and PDIP packages.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

V_{DD} Supply Voltage 6V
Operating Temperature
C Suffix .... 0°C to 70°C
E Suffix .... – 40°C to +85°C
OSC, FC, $\overline{SHDN}$ Input Voltage .... – 0.3V to (V^+ + 0.3V)
Output Short Circuit Duration .... 10 Sec.
Storage Temperature .... – 65°C to +150°C
Power Dissipation ($T_A \leq 70°C$)
PDIP 730mW
SOIC 470mW
MSOP 333mW
Lead Temperature (Soldering,10 sec) .... +300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

T_A = 0°C to 70°C (C suffix), – 40°C to +85° (E suffix), V^+ = 5V ±10% C_{OSC} = OPEN, C1, C2 = 10µF, FC = V^+, $\overline{SHDN}$ = V_{IH}, unless otherwise specified. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{DD}	Active Supply Current	R_L = Open, FC = Open or GND R_L = Open, FC = V^+	— —	50 0.6	100 1	µA mA
$I_{SHUTDOWN}$	Shutdown Supply Current	$\overline{SHDN}$ = 0V	—	0.2	1.0	µA
V^+	Supply Voltage		2.4	—	5.5	V
V_{IH}	$\overline{SHDN}$ Logic High Input Voltage		V_{DD} x 0.8	—	—	V
V_{IL}	$\overline{SHDN}$ Logic Low Input Voltage		—	—	0.4	V
I_{IN}	Input Leakage Current	$\overline{SHDN}$, OSC FC Pin	– 1 – 4	— —	1 4	µA
R_{OUT}	Output Source Resistance	I_{OUT} = 60 mA	—	12	20	Ω
I_{OUT}	Output Current	V_{OUT} more negative than – 3.75V	60	100	—	mA
F_{OSC}	Oscillator Frequency	Pin 7 Open, Pin 1 Open or GND $\overline{SHDN}$ = V_{IH}, Pin 1 = V^+	5 100	10 200	— —	kHz
P_{EFF}	Power Efficiency	FC = GND For All R_L = 2k between V^+ and V_{OUT} R_L = 1 kΩ between V_{OUT} and GND I_L = 60 mA to GND	— 93 94 —	— 97 97 92	— — — —	%
V_{EFF}	Voltage Conversion Efficiency	R_L = OPEN	99	99.9	—	%

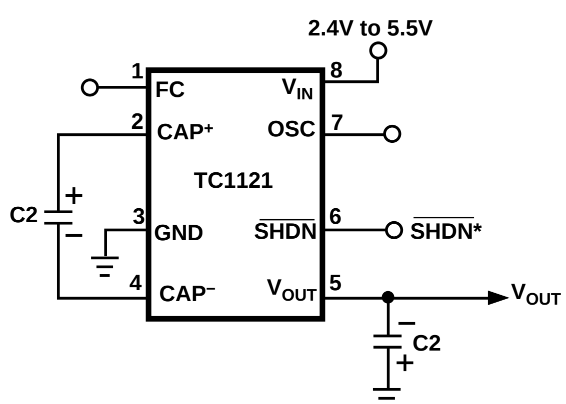
PIN DESCRIPTION

Pin No. (8-Pin MSOP, PDIP, SOIC)	Symbol	Function Inverter
1	FC	Frequency control for internal oscillator, FC = open, F_{OSC} = 10kHz typ; FC = V^+, F_{OSC} = 200kHz typ,FC has no effect when OSC pin is driven externally.
2	CAP^+	Charge-pump capacitor, positive terminal.
3	GND	Power-supply ground input.
4	CAP^-	Charge-pump capacitor, negative terminal.
5	OUT	Output, negative voltage.
6	$\overline{SHDN}$	Shutdown.
7	OSC	Oscillator control input. An external capacitor can be added to slow the oscillator. Take care to minimize stray capacitance. An external oscillator also may be connected to overdrive OSC.
8	V^+	Power-supply positive voltage input.

APPLICATIONS

Negative Voltage Converter

The TC1121 is typically used as a charge-pump voltage inverter. C1 and C2 are the only two external capacitors used in the operating circuit (see Figure 1).



NOTES: *$\overline{SHDN}$ should be tied to V_{IN} if not used.

Figure 1. Charge Pump Inverter

The TC1121 is not sensitive to load current changes, although its output is not actively regulated. A typical output source resistance of 11.8Ω means that an input of +5V results in – 5V output voltage under light load, and only decreases to – 3.8V typ with a 100mA load.

The supplied output current is from capacitor C2 during one-half the charge-pump cycle. This results in a peak-to-peak ripple of:

$$V_{RIPPLE} = I_{OUT}/2(f_{PUMP})\ (C2) + I_{OUT}\ (ESR_{C2})$$

Where f_{PUMP} is 5kHz (one half the nominal 10kHz oscillator frequency), and C2 = 150µF with an ESR of 0.2Ω, ripple is about 90mV with a 100mA load current. If C2 is raised to 390µF, the ripple drops to 45mV.

Changing Oscillator Frequency

The TC1121's clock frequency is controlled by four modes:

FC	OSC	Oscillator Frequency
Open	Open	10kHz
FC = V^+	Open	200kHz
Open or FC = V^+	External Capacitor	See Typical Operating Characteristics
Open	External Clock	External Clock Frequency

The oscillator runs at 10kHz (typical) when FC and OSC are not connected. The oscillator frequency is lowered by connecting a capacitor between OSC and GND, but FC can still multiply the frequency by 20 times in this mode.

An external clock source that swings within 100mV of V^+ and GND may overdrive OSC in the inverter mode. OSC can be driven by any CMOS logic output. When OSC is overdriven, FC has no effect.

Note that the frequency of the signal appearing at CAP^+ and CAP^- is half that of the oscillator. In addition, by lowering the oscillator frequency, the effective output resistance of the charge-pump increases. To compensate for this, the value of the charge-pump capacitors may be increased.

Because the 5kHz output ripple frequency may be low enough to interfere with other circuitry, the oscillator frequency can be increased with the use of the FC pin or an external oscillator. The output ripple frequency is half the selected oscillator frequency. Although the TC1121's quiescent current will increase if the clock frequency is increased, it allows smaller capacitance values to be used for C1 and C2.

Capacitor Selection

In addition to load current, the following factors affect the TC1121 output voltage drop from its ideal value 1) output resistance, 2) pump (C1) and reservoir (C2) capacitor ESRs, and 3) C1 and C2 capacitance.

The voltage drop is the load current times the output resistance. The loss in C2 is the load current times C2's ESR; C1's loss is larger because it handles currents greater than the load current during charge-pump operation. Therefore, the voltage drop due to C1 is about four times C1's ESR multiplied by the load current, and a low (or high) ESR capacitor has a greater impact on performance for C1 than for C2.

In general, as the TC1121's pump frequency increases, capacitance values needed to maintain comparable ripple and output resistance diminish proportionately.

Cascading Devices

To produce greater negative magnitudes of the initial supply voltage, the TC1121 may be cascaded (see Figure 3). Resulting output resistance is approximately equal to the sum of individual TC1121 R_{OUT} values. The output voltage (where n is an integer representing the number of devices cascaded) is defined by $V_{OUT} = -n(V_{IN})$.

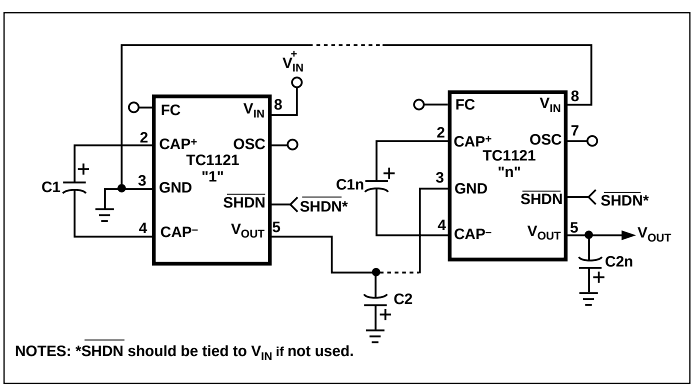


Figure 3. Cascading TC1121s to Increase Output Voltage

Paralleling Devices

To reduce output resistance, multiple TC1121s may be paralleled (see Figure 4). Each device needs a pump capacitor C1, but the reservoir capacitor C2 serves all devices. The value of C2 should be increased by a factor of n (the number of devices).

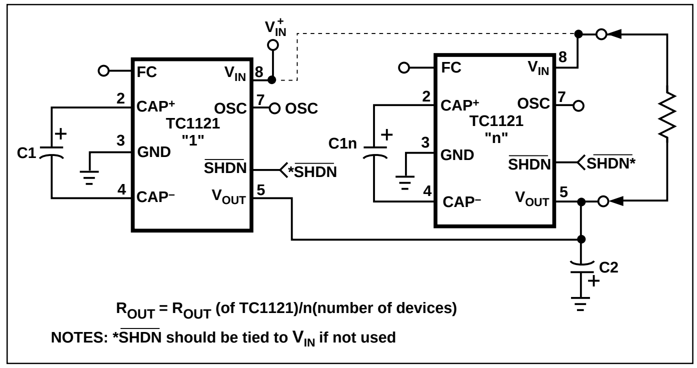


Figure 4. Paralleling TC1121s to Reduce Output Resistance

Combined Positive Supply Multiplication and Negative Voltage Conversion

Figure 5 shows this dual function circuit, in which capacitors C1 and C2 perform pump and reservoir functions to generate negative voltage. Capacitors C2 and C4 are the respective capacitors for multiplied positive voltage. This particular configuration leads to higher source impedances of the generated supplies due to the finite impedance of the common charge-pump driver.

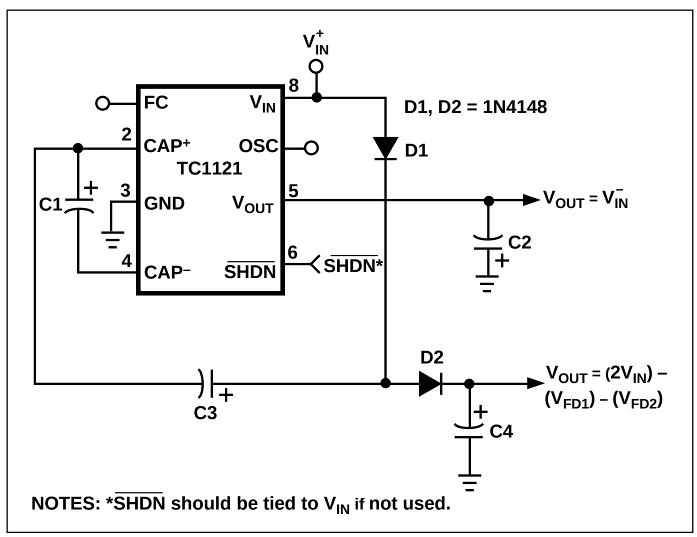
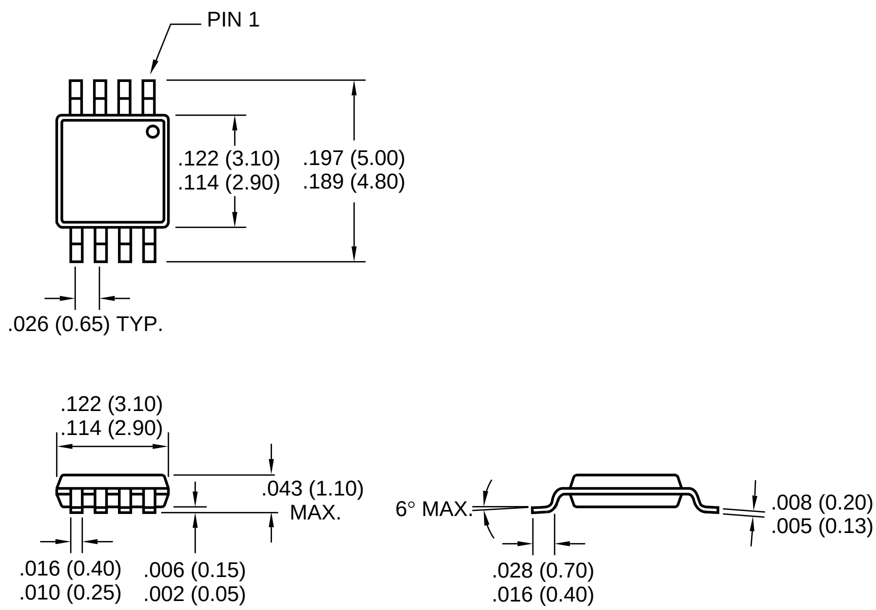


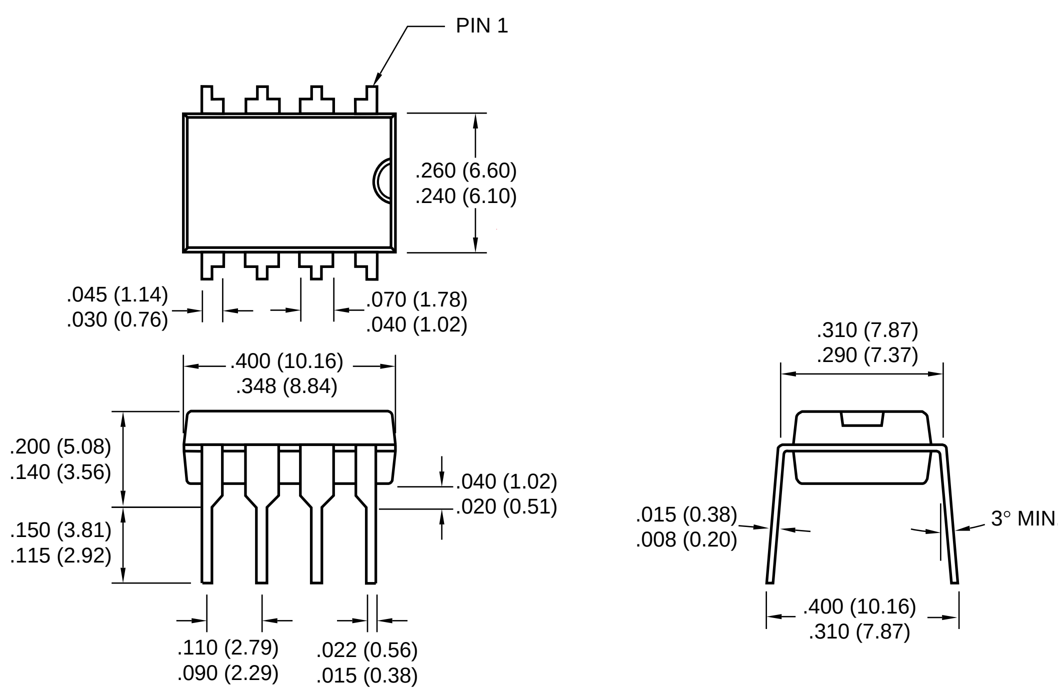
Figure 5. Combined Positive Multiplier and Negative Converter

PACKAGE DIMENSIONS

8-Pin MSOP



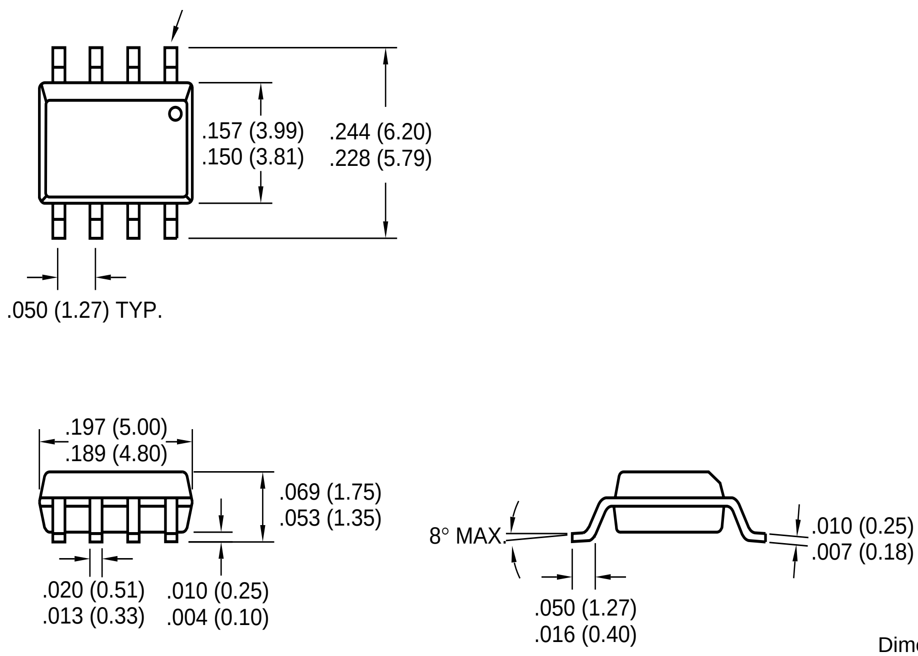
8-Pin plastic DIP



Dimensions: inches (mm)

PACKAGE DIMENSIONS (Cont.)

8-Pin SOIC



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