Linear Building Block – Low-Power Voltage Reference with Dual Op Amp, Dual Comparator, and Shutdown Mode

FEATURES

- **Combines Two Op Amps, Two Comparators and a Voltage Reference into a Single Package**
- **Optimized for Single-Supply Operation**
- **Small Package ..... 16-Pin QSOP**
- **Ultra Low Input Bias Current ..... Less than 100pA**
- **Low Quiescent Current .... Operating 16μA (Typ.) Shutdown 6μA (Typ.)**
- **Rail-to-Rail Inputs and Outputs**
- **Operates Down to V_{DD} = 1.8V**
- **Reference and One Comparator Remain Active in Shutdown to Provide Supervisory Functions**

APPLICATIONS

- **Power Management Circuits**
- **Battery Operated Equipment**
- **Consumer Products**
- **Replacements for Discrete Components**

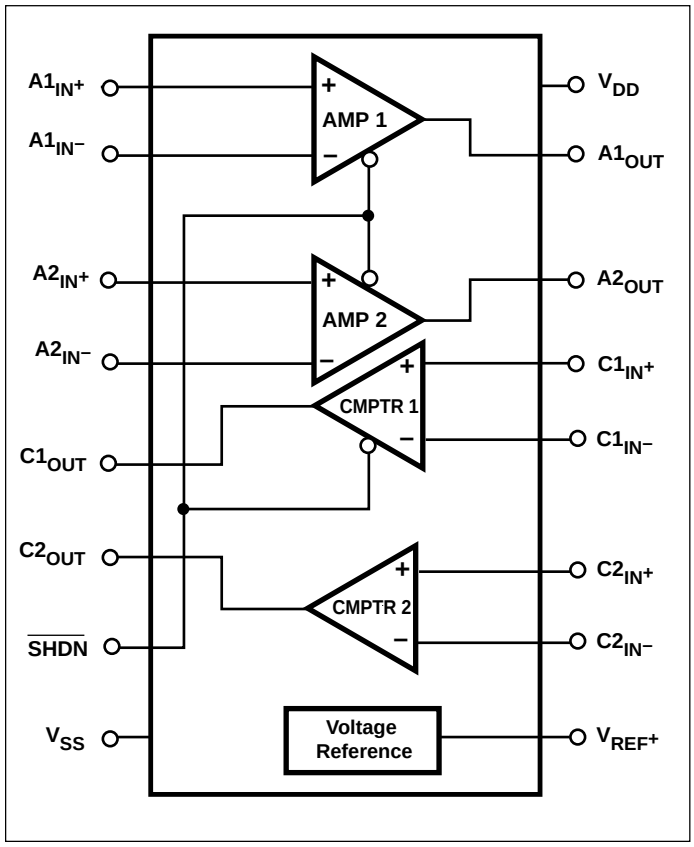
GENERAL DESCRIPTION

The TC1043 is a mixed-function device combining two general purpose op amps, two general purpose comparators, and a voltage reference in a single 16-Pin package.

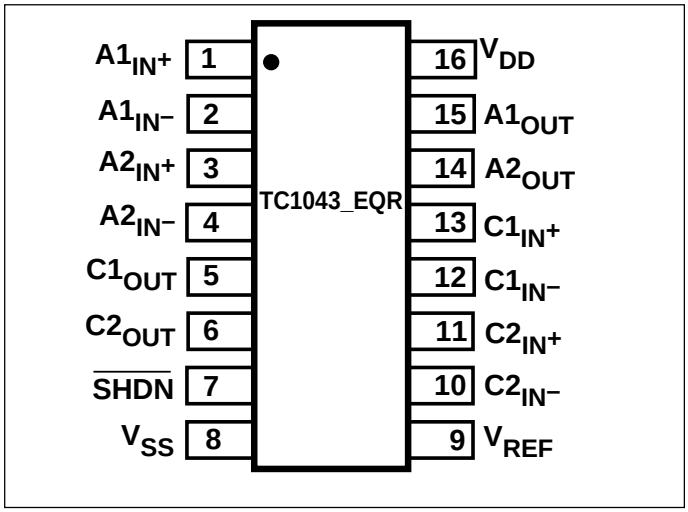
This increased integration allows the user to replace two or three packages, saving space, lowering supply current, and increasing system performance. A Shutdown input, $\overline{SHDN}$, disables the op amps and one of the comparators, placing their outputs in a high-impedance state. The reference and one comparator stay active in Shutdown mode. Standby power consumption is typically 6μA.Both the Op Amps and comparators have rail-to-rail inputs and outputs which allows operation from low supply voltages with large input and output signal swings.

Packaged in a 16-Pin QSOP, the TC1043 is ideal for applications requiring high integration, small size, and low power.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (QSOP)



ORDERING INFORMATION

Part No.	Package	Temperature Range
TC1043CEQR	16-Pin QSOP	–40°C to +85°C

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 6.0V
Voltage on Any Pin:
(With Respect to Supplies) .. (V_{SS} – 0.3V) to (V_{DD} +0.3V)
Operating Temperature Range: ..... – 40°C to + 85°C
Storage Temperature Range ..... – 55°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +260°C

* Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: Typical values apply at 25°C and V_{DD} = 3.0V. Minimum and maximum values apply for T_A = –40° to +85°C and V_{DD} = 1.8V to 5.5V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		1.8	—	5.5	V
I_Q	Supply Current, Operating	All outputs unloaded, $\overline{SHDN}$ = V_{DD}	—	16	30	µA
I_{SHDN}	Supply Current, Shutdown	CMPTR2 and V_{REF} Outputs unloaded, $\overline{SHDN}$ = V_{SS}	—	6	10	µA
Shutdown Input						
V_{IH}	Input High Threshold		80% V_{DD}	—	—	V
V_{IL}	Input Low Threshold		—	—	20% V_{DD}	V
I_{SI}	Shutdown Input Current		—	—	±100	nA
Op Amps						
T_{SEL}	Select Time	(V_{OUT} from $\overline{SHDN}$ = V_{IH}) R_L =10KΩ to V_{SS}	—	15	—	µsec
T_{DESEL}	Deselect Time	(V_{OUT} from $\overline{SHDN}$ = V_{IL}) R_L =10KΩ to V_{SS}	—	100	—	nsec
R_{OUT}(SD)	Output Resistance in Shutdown	$\overline{SHDN}$ = V_{SS}	20	—	—	MΩ
C_{OUT}(SD)	Output Capacitance in Shutdown	$\overline{SHDN}$ = V_{SS}	—	—	5	pF
A_{VOL}	Large Signal Voltage Gain	R_L = 10 KΩ, V_{DD} = 5V	—	100	—	V/mV
V_{ICMR}	Common Mode Input Voltage Range		V_{SS} – 0.2	—	V_{DD} +0.2	V
V_{OS}	Input Offset Voltage	V_{DD} = 3V, V_{CM} = 1.5V, T_A = 25°C, T_A = –40°C to 85°C		±100 ±0.3	±500 ±1.5	µV mV
I_B	Input Bias Current	T_A = 25°C, V_{CM} = V_{DD} to V_{SS}	–100	50	100	pA
$V_{OS\ (DRIFT)}$	Average Iz–ut Offset Voltage Drift	V_{DD} = 3V, V_{CM} = 1.5V	—	4	—	µV/°C
GBWP	Gain-Bandwidth Product	V_{DD} = 1.8V to 5.5V; V_O = V_{DD} to V_{SS}	—	90	—	KHz
SR	Slew Rate	C_L = 100pF R_L = 1MΩ to GND Gain = 1 V_{IN} = V_{SS} to V_{DD}	—	35	—	mV/µsec
V_{OUT}	Output Signal Swing	R_L = 10 KΩ	V_{SS}+ 0.05	—	V_{DD}– 0.05	V
CMRR	Common Mode Rejection Ratio	T_A = 25°C, V_{DD} = 5V V_{CM} = V_{DD} to V_{SS}	70	—	—	dB
PSRR	Power Supply Rejection Ratio	T_A = 25°C, V_{CM} = V_{SS} V_{DD} = 1.8 to 5V	80	—	—	dB
I_{SRC}	Output Source Current	V_{IN}+ = V_{DD}, V_{IN} – = V_{SS}, Output Shorted to V_{SS} V_{DD} = 1.8V, Gain = 1	3	—	—	mA
I_{SINK}	Output Sink Current	V_{IN}+ = V_{SS}, V_{IN} – = V_{DD}, Output Shorted to V_{DD} V_{DD} = 1.8V, Gain = 1	4	—	—	mA

ELECTRICAL CHARACTERISTICS: (Cont.) Typical values apply at 25°C and V_{DD} = 3.0V. Minimum and maximum values apply for T_A = –40° to +85°C and V_{DD} = 1.8V to 5.5V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Op Amps (Cont.)						
en	Input Noise Voltage	0.1 Hz to 10 Hz	—	10	—	μV_{pp}
	Input Noise Density	1KHz	—	125	—	$nV/\sqrt{Hz}$
Comparators						
R_{OUT}(SD)	Output Resistance in Shutdown	$\overline{SHDN} = V_{SS}$	20	—	—	MΩ
C_{OUT}(SD)	Output Capacitance in Shutdown	$\overline{SHDN} = V_{SS}$	—	—	5	pF
T_{SEL}	Select Time (For Valid Output)	V_{OUT} from $\overline{SHDN} = V_{IH}$ R_L =10KΩ to V_{SS}	—	20	—	µsec
T_{DESEL}	Deselect Time	V_{OUT} from $\overline{SHDN} = V_{IL}$ R_L =10KΩ to V_{SS}	—	500	—	nsec
V_{ICMR}	Common Mode Input Voltage Range		V_{SS} – 0.2	—	V_{DD} +0.2	V
V_{OS}	Input Offset Voltage	V_{DD} = 3V, V_{CM} =1.5V, T_A = 25°C T_A = –40°C to 85°C	–5 –5	—	+5 +5	mV mV
I_B	Input Bias Current	T_A = 25°C, IN+, IN– = V_{DD} to V_{SS}	—	—	±100	pA
V_{OH}	Output High Voltage	R_L = 10KΩ to V_{SS}	V_{DD} – 0.3	—	—	V
V_{OL}	Output Low Voltage	R_L = 10KΩ to V_{DD}	—	—	0.3	V
CMRR	Common Mode Rejection Ratio	T_A = 25°C, V_{DD} = 5V V_{CM} = V_{DD} to V_{SS}	66	—	—	dB
PSRR	Power Supply Rejection Ratio	T_A = 25°C, V_{CM} =1.2V V_{DD} = 1.8V to 5V	60	—	—	dB
I_{SRC}	Output Source Current	IN+ = V_{DD}, IN– = V_{SS} Output Shorted to V_{SS} V_{DD} = 1.8V	1	—	—	mA
I_{SINK}	Output Sink Current	IN+ = V_{SS}, IN– = V_{DD}, Output Shorted to V_{DD} V_{DD} = 1.8V	2	—	—	mA
t_{PD1}	Response Time	100 mV Overdrive,C_L = 100pF	—	4	—	µsec
t_{PD2}	Response Time	10mV Overdrive, C_L = 100pF	—	6	—	µsec
Voltage Reference						
V_{REF}	Reference Voltage		1.176	1.200	1.224	V
$I_{REF(SOURCE)}$	Source Current		50	—	—	µA
$I_{REF(SINK)}$	Sink Current		50	—	—	µA
$C_{L(REF)}$	Load Capacitance		—	—	100	pF
N_{VREF}	Voltage Noise	100 Hz to 100 KHz	—	20	—	μV_{RMS}
	Noise Density	1 KHz	—	1.0	—	$\mu V/\sqrt{Hz}$

DETAILED DESCRIPTION

The TC1043 is one of a series of very low power, linear building block products targeted at low voltage, single supply applications. The TC1043 minimum operating voltage is 1.8V and typical supply current is only 20μA (fully enabled). It combines two comparators, two op amps, and a voltage reference in a single package. A shutdown mode is incorporated for easy adaptation to system power management schemes. During shutdown, all but one comparator and the voltage reference are disabled (i.e. powered down and with their respective outputs at high impedance). The "still awake" comparator and voltage reference can be used as a wake-up timer, power supply monitor, LDO controller, or other continuous duty circuit function.

Comparators

The TC1043 contains two comparators. The comparators' input range extends beyond both supply voltages by 200mV and the outputs will swing to within several millivolts of the supplies depending on the load current being driven.

The comparators exhibit a propagation delay and supply current which are largely independent of supply voltage. The low input bias current and offset voltage make them suitable for high impedance precision applications.

Comparator CMPTR1 is disabled during shutdown and has a high impedance output. Comparator CMPTR2 remains active.

Operational Amplifiers

The TC1043 contains two rail-to-rail op amps. The amplifiers' input range extends beyond both supplies by 200mV and the outputs will swing to within several millivolts of the supplies depending on the load current being driven.

The amplifier design is such that large signal gain, slew rate and bandwidth are largely independent of supply voltage. The low input bias current and offset voltage of the TC1043 make it suitable for precision applications. Both op amps are disabled during shutdown and have high output impedance.

Voltage Reference

A 2.0 percent tolerance, internally biased, 1.20V bandgap voltage reference is included in the TC1043. It has a push-pull output capable of sourcing and sinking at least 50 μA. The voltage reference remains fully enabled during shutdown.

Shutdown Input

$\overline{SHDN}$ at V_{IL} disables both op amps and one comparator. The $\overline{SHDN}$ input cannot be allowed to float; when not used, connect it to V_{DD}. The disabled comparator's output and the two disabled op amps' outputs are in a high impedance state when shutdown is active. The disabled comparator's inputs and the two disabled op amps' inputs can be driven from rail-to-rail by an external voltage when the TC1043 is in shutdown. No latchup will occur when the device is driven to its enabled state when $\overline{SHDN}$ is set to V_{IH}.

TYPICAL APPLICATIONS

The TC1043 lends itself to a wide variety of applications, particularly in battery-powered systems. It typically finds application in power management, processor supervisory, and interface circuitry.

Wake-Up Timer

Many microcontrollers have a low power "sleep" mode that significantly reduces their supply current. Typically, the microcontroller is placed in this mode via a software instruction, and returns to a fully enabled state upon reception of an external signal ("wake-up"). The wake-up signal is usually supplied by a hardware timer. Most system applications demand that this timer have a long duration (typically seconds or minutes), and consume as little supply current as possible.

The circuit shown in Figure 1 is a wake-up timer made from comparator CMPTR2. (CMPTR2 is used because the wake-up timer must operate when $\overline{SHDN}$ is active.) Capacitor C1 charges through R1 until a voltage equal to V_R is reached, at which point the WAKE-UP is driven active. Upon wake-up, the microcontroller resets the timer by forcing a logic low on a dedicated, open drain I/O port pin. This discharges C1 through R4 (the value of R4 is chosen to limit the maximum current sunk by the I/O port pin). With a 3V supply, the circuit as shown consumes typically 6 μA and furnishes a nominal timer duration of 25 seconds.

Precision Battery Monitor

Figure 2 is a precision battery low/battery dead monitoring circuit. Typically, the battery low output warns the user that a battery dead condition is imminent. Battery dead typically initiates a forced shutdown to prevent operation at low internal supply voltages (which can cause unstable system operation).

The circuit of Figure 2 uses a single TC1043 (one op amp is unused) and only six external resistors. AMP 1 is a simple buffer while CMPTR1 and CMPTR2 provide precision voltage detection using V_R as a reference. Resistors R2 and R4 set the detection threshold for $\overline{BATTLOW}$ while resistors R1 and R3 set the detection threshold for $\overline{BATTFAIL}$. The component values shown assert

$\overline{\text{BATT LOW}}$ at 2.2V (typical) and $\overline{\text{BATT FAIL}}$ at 2.0V (typical). Total current consumed by this circuit is typically 22 µA at 3V. Resistors R5 and R6 provide hysteresis for comparators CMPTR1 and CMPTR2, respectively.

Dual LDO with Shutdown

Figure 3 shows a portion of a TC1043 configured as a dual low dropout regulator with shutdown. AMP1 and AMP2 are independent error amplifiers that use V_R as a reference. Resistors RA_1, RB_1, RA_2, and RB_2 set the feedback around the amplifiers and therefore determine the output voltage settings (please see equation in the figure). RA_1, RB_1, RA_2, and RB_2 can have large ohmic values (i.e. 100's of KΩ) to minimize supply current.

Using the 2N2222 output transistors as shown, these regulators exhibit low dropout operation. For example, with V_{OUT} = 3.0V, the typical dropout voltage is only 50 mV at an output current of 50 mA. The unused comparators can be used in conjunction with this circuit as power-on reset or low voltage detectors for a complete LDO solution at a very low installed cost.

External Hysteresis

Hysteresis can be set externally with two resistors using positive feedback techniques (see Figure 4). The design procedure for setting external comparator hysteresis is as follows:

1. Choose the feedback resistor R_C. Since the input bias current of the comparator is at most 100 pA, the current through R_C can be set to 100 nA (i.e. 1000 times the input bias current) and retain excellent accuracy. The current through R_C at the comparator's trip point is V_R / R_C where V_R is a stable reference voltage.

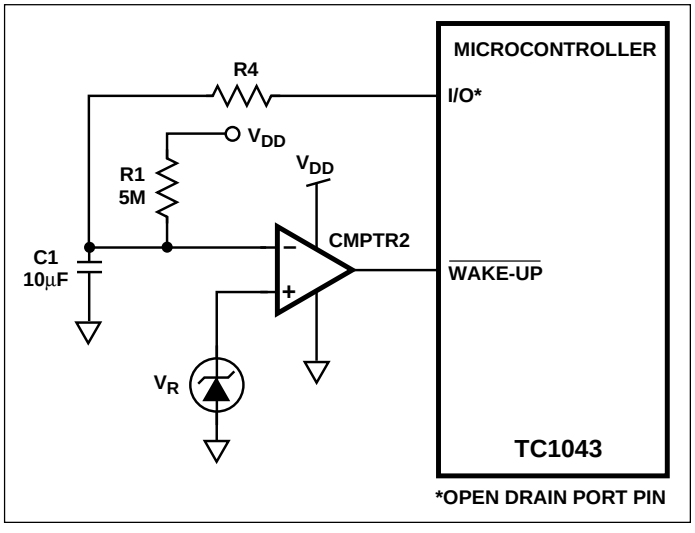


Figure 1. Wake-Up Timer

2. Determine the hysteresis voltage (V_{HY}) between the upper and lower thresholds.

3. Calculate R_A as follows.

$$R_A = R_C \left(\frac{V_{HY}}{V_{DD}}\right)$$

Equation 1.

4. Choose the rising threshold voltage for V_{SRC} (V_{THR}).

5. Calculate R_B as follows:

$$R_B = \frac{1}{\left[\left(\frac{V_{THR}}{(V_R * R_A)}\right) - \frac{1}{R_A} - \frac{1}{R_C}\right]}$$

Equation 2.

6. Verify the threshold voltages with these formulas:

V_{SRC} rising:

$$V_{THR} = (V_R)(R_A)\left[\left(\frac{1}{R_A}\right) + \left(\frac{1}{R_B}\right) + \left(\frac{1}{R_C}\right)\right]$$

Equation 3.

V_{SRC} falling:

$$V_{THF} = V_{THR} - \left[\frac{(R_A * V_{DD})}{R_C}\right]$$

Equation 4.

32.768 KHz 'Time Of Day Clock' Crystal Controlled Oscillator

A very stable oscillator driver can be designed by using a crystal resonator as the feedback element. Figure 5 shows a typical application circuit using this technique to develop a clock driver for a Time Of Day (TOD) clock chip. The value of R_A and R_B determine the DC voltage level at which the comparator trips — in this case one-half of V_{DD}. The RC time constant of R_C and C_A should be set several times greater than the crystal oscillator's period, which will ensure a 50% duty cycle by maintaining a DC voltage at the inverting comparator input equal to the absolute average of the output signal.

Non-Retriggerable One Shot Multivibrator

Using two comparators, a non-retriggerable one shot multivibrator can be designed using the circuit configuration of Figure 6. A key feature of this design is that the pulse width is independent of the magnitude of the supply voltage because the charging voltage and the intercept voltage are

a fixed percentage of V_{DD}. In addition, this one shot is capable of pulse width with as much as a 99% duty cycle and exhibits input lockout to ensure that the circuit will not re-trigger before the output pulse has completely timed out. The trigger level is the voltage required at the input to raise the voltage at node A higher than the voltage at node B, and is set by the resistive divider R4 and R10 and the impedance network composed of R1, R2, and R3. When the one shot has been triggered, the output of CMPTR2 is high, causing the reference voltage at the non-inverting input of CMPTR1 to go to V_{DD}. This prevents any additional input pulses from disturbing the circuit until the output pulse has timed out.

The value of the timing capacitor C1 must be small enough to allow CMPTR1 to discharge C1 to a diode voltage before the feedback signal from CMPTR2 (through R10) switches CMPTR1 to its high state and allows C1 to start an exponential charge through R5. Proper circuit action depends upon rapidly discharging C1 through the voltage set by R6, R9, and D2 to a final voltage of a small diode drop. Two propagation delays after the voltage on C1 drops below the level on the non-inverting input of CMPTR2, the output of CMPTR1 switches to the positive rail and begins to charge C1 through R5. The time delay which sets the output pulse width results from C1 charging to the reference voltage set by R6, R9, and D2, plus four comparator propagation delays. When the voltage across C1 charges beyond the reference, the output pulse returns to ground and the input is again ready to accept a trigger signal.

Oscillators and Pulse Width Modulators

Microchip's linear building block comparators adapt well to oscillator applications for low frequencies (less than 100 KHz). Figure 7 shows a symmetrical square wave generator using a minimum number of components. The output is set by the RC time constant of R4 and C1, and the total hysteresis of the loop is set by R1, R2, and R3. The maximum frequency of the oscillator is limited only by the large signal propagation delay of the comparator in addition to any capacitive loading at the output which degrades the slew rate.

To analyze this circuit, assume that the output is initially high. For this to occur, the voltage at the inverting input must be less than the voltage at the non-inverting input. Therefore, capacitor C1 is discharged. The voltage at the non-inverting input (V_H) is:

$$V_H = \frac{R2(V_{DD})}{[R2 + (R1 \parallel R3)]}$$

Equation 5.

where, if R1 = R2 = R3, then:

$$V_H = \frac{2\,(V_{DD})}{3}$$

Equation 6.

Capacitor C1 will charge up through R4. When the voltage at the comparator's inverting input is equal to V_H, the comparator output will switch. With the output at ground potential, the value at the non-inverting input terminal (V_L) is reduced by the hysteresis network to a value given by:

$$V_L = \frac{V_{DD}}{3}$$

Equation 7.

Using the same resistors as before, capacitor C1 must now discharge through R4 toward ground. The output will return to a high state when the voltage across the capacitor has discharged to a value equal to V_L. The period of oscillation will be twice the time it takes for the RC circuit to charge up to one half its final value. The period can be calculated from:

$$\frac{1}{FREQ} = 2\,(0.694)\,(R4)\,(C1)$$

Equation 8.

The frequency stability of this circuit should only be a function of the external component tolerances.

Figure 8 shows the circuit for a pulse width modulator circuit. It is essentially the same as in Figure 7 with the addition of an input control voltage. When the input control voltage is equal to one-half V_{DD}, operation is basically the same as described for the free-running oscillator. If the input control voltage is moved above or below one-half V_{DD}, the duty cycle of the output square wave will be altered. This is because the addition of the control voltage at the input has now altered the trip points. The equations for these trip points are shown in Figure 8 (see V_H and V_L).

Pulse width sensitivity to the input voltage variations can be increased by reducing the value of R6 from 10 KΩ and conversely, sensitivity will be reduced by increasing the value of R6. The values of R1 and C1 can be varied to produce the desired center frequency.

Voice Band Receive Filter

The majority of spectral energy for human voices is found to be in a 2.7 KHz frequency band from 300 Hz to 3 KHz. To properly recover a voice signal in applications such

as radios, cellular phones, and voice pagers a low-power bandpass filter that is matched to the human voice spectrum can be implemented using TelCom's CMOS op amps. Figure 9 shows a unity gain multi-pole Butterworth filter with ripple less than 0.15 dB in the human voice band. The lower 3 dB cut-off frequency is 70 Hz (single order response) while the upper cut-off frequency is 3.5 KHz (fourth order response).

Supervisory Audio Tone (SAT) Filter for Cellular

Supervisory Audio Tones (SAT) provide a reliable transmission path between cellular subscriber units and base stations. The SAT tone functions much like the current/voltage used in land line telephone systems to indicate that a phone is off the hook. The SAT tone may be one of three frequencies: 5970, 6000, or 6030 Hz. A loss of SAT implies that channel conditions are impaired and if SAT is interrupted for more than 5 seconds a cellular call is terminated.

Figure 10 shows a high Q (30) second order SAT detection bandpass filter using TelCom's CMOS op amp architecture. This circuit nulls all frequencies except the three SAT tones of interest.

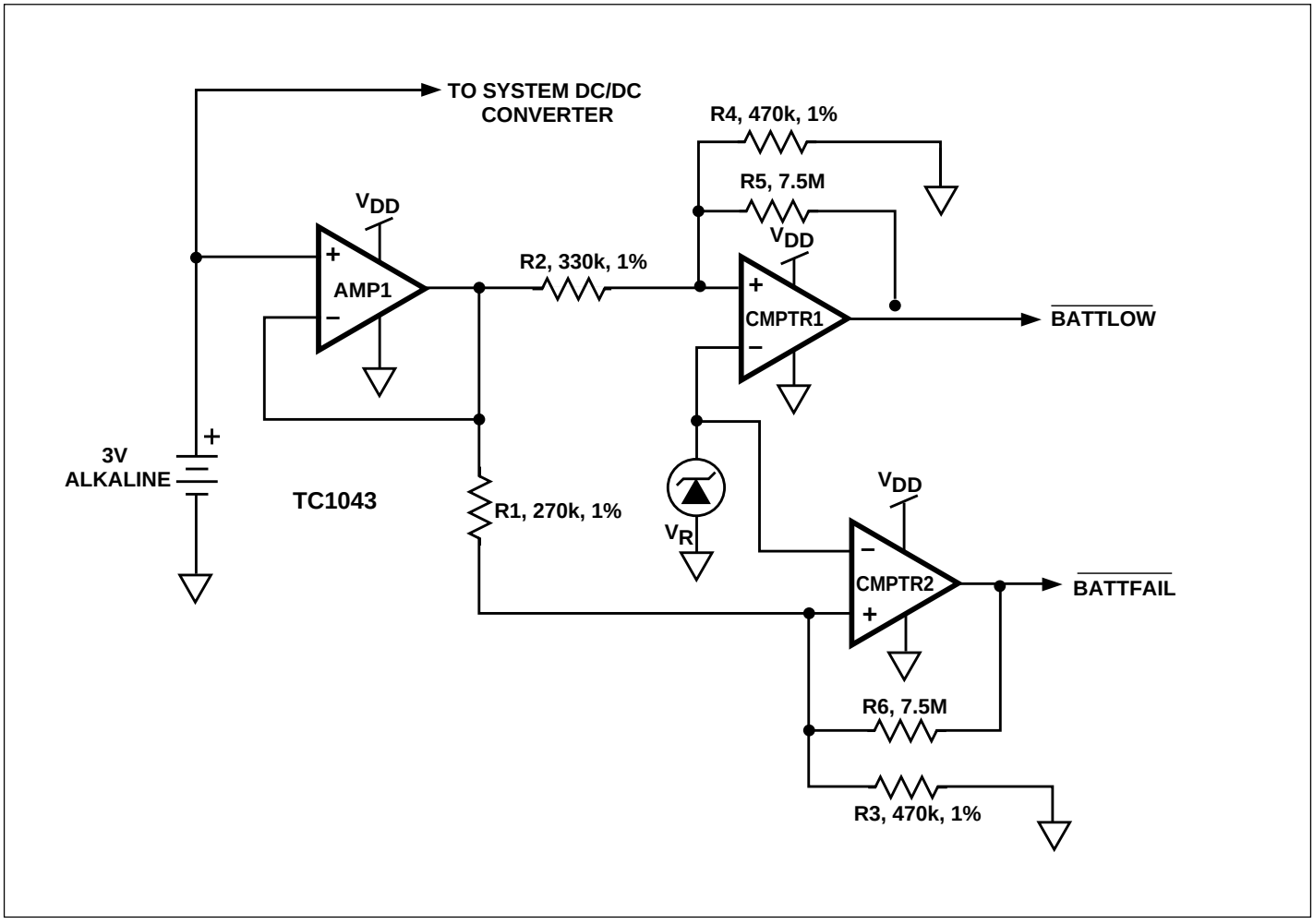


Figure 2. Precision Battery Monitor

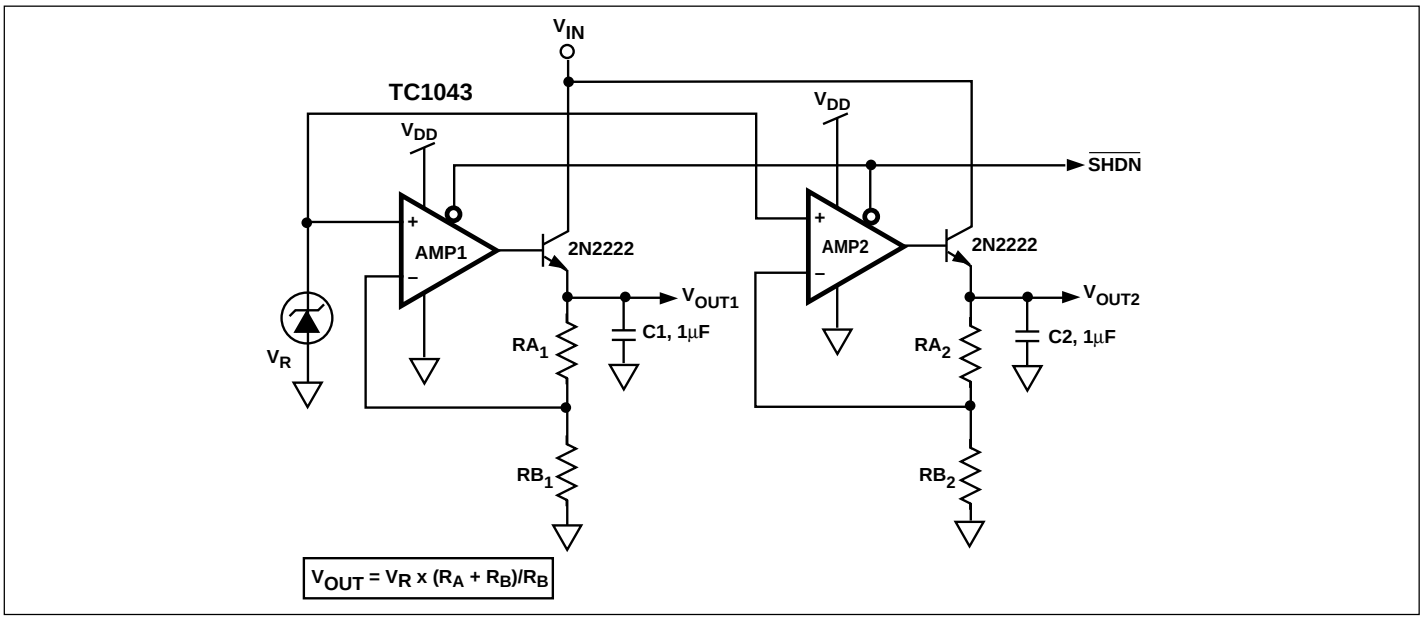


Figure 3. Dual Low Dropout Regulator

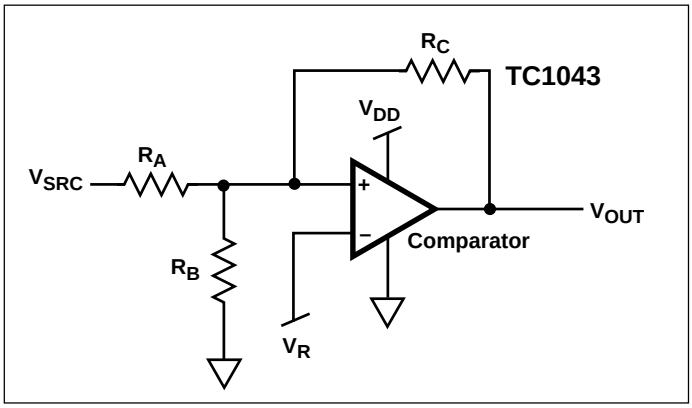


Figure 4. Comparator External Hysteresis Configuration

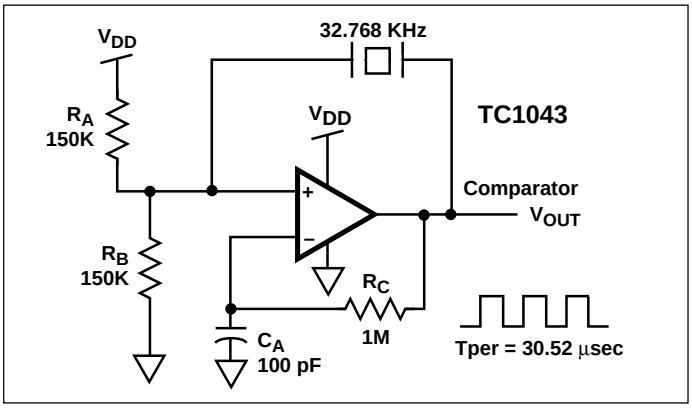


Figure 5. 32.768 KHz "Time of Day" Clock Oscillator

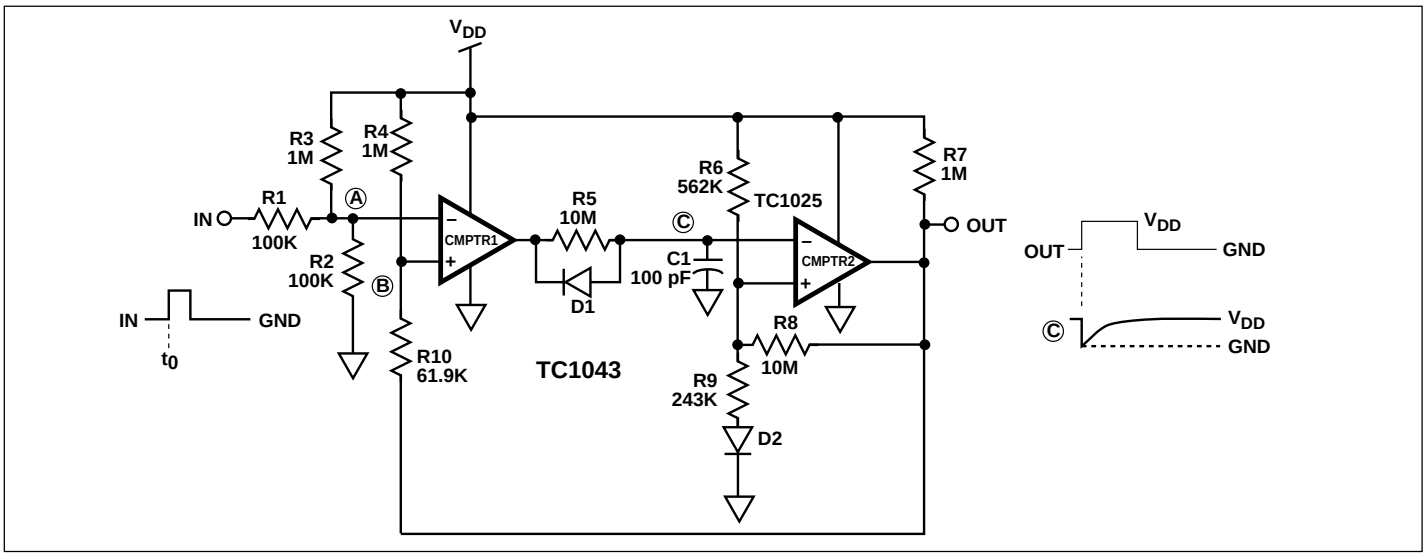


Figure 6. Non-Retriggerable Multivibrator

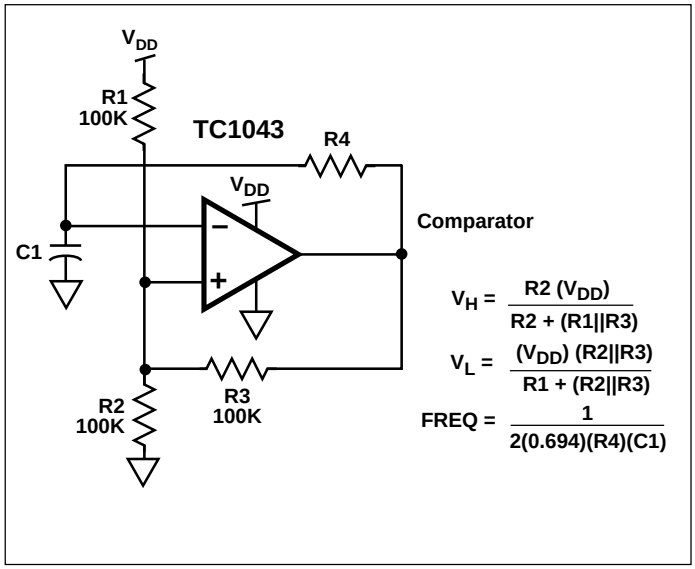


Figure 7. Square Wave Generator

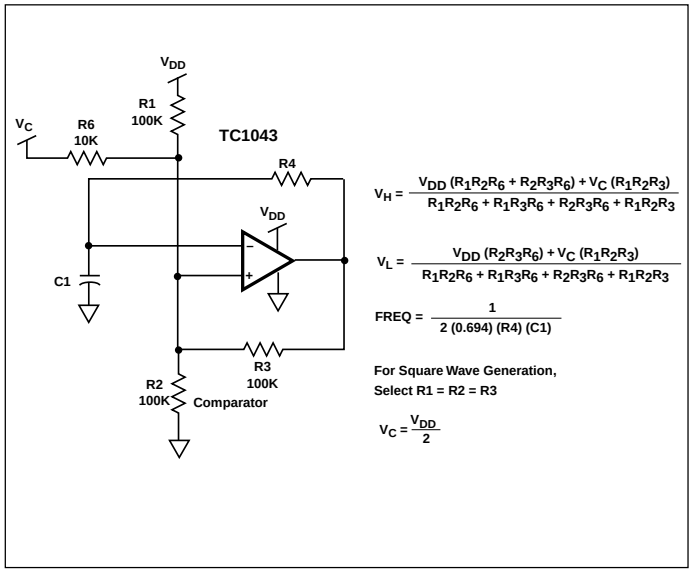


Figure 8. Pulse Width Modulator

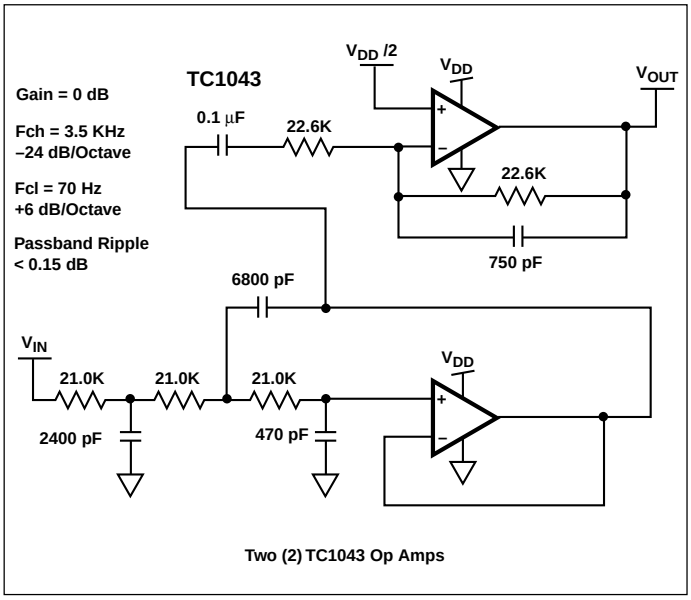


Figure 9. Multi-Pole Butterworth Voice Band Receive Filter

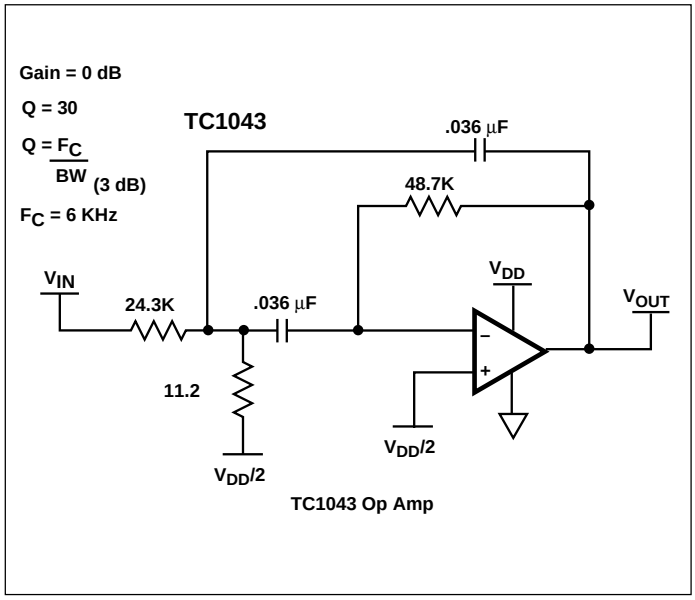


Figure 10. Second Order SAT Bandpass Filter

TC1043 DEMO CARD

The TC1043 Demo Card is a 1.25" x 1.0" card containing a TC1043 and all of the necessary external components required to develop a Dual Adjustable Low Dropout Voltage Regulator with 'Power Good' Flags and Master Shutdown Mode. This application utilizes all five internal cells (i.e. both op-amps, both comparators and the reference) of the TC1043 which allows the user to evaluate the device performance in a system level application.

The demo card is fully assembled with the required external resistors, capacitors, transistors, and potentiometers that allow the user to adjust the two regulated output voltages (V_{OUT1}, V_{OUT2}) and the two 'Power Good' Flag (V_{OUT1_GOOD}, V_{OUT2_GOOD}) threshold levels. For convenience, several test points and jumpers are available for measuring various voltages and currents on the circuit board.

Figure 11 is a schematic of the TC1043 Demo Card, and Figure 12 shows the assembly drawing and artwork for the board. Table 1 lists the voltages that are monitored by the test points and Table 2 lists the currents that can be measured as well as the various operating modes of the demo card using the jumpers on the board. **NOTE: Never operate the TC1043 Demo Card with both J2 and J3 connected simultaneously!** Table 3 lists the adjustments the user can make with the four potentiometers (VR1 through VR4).

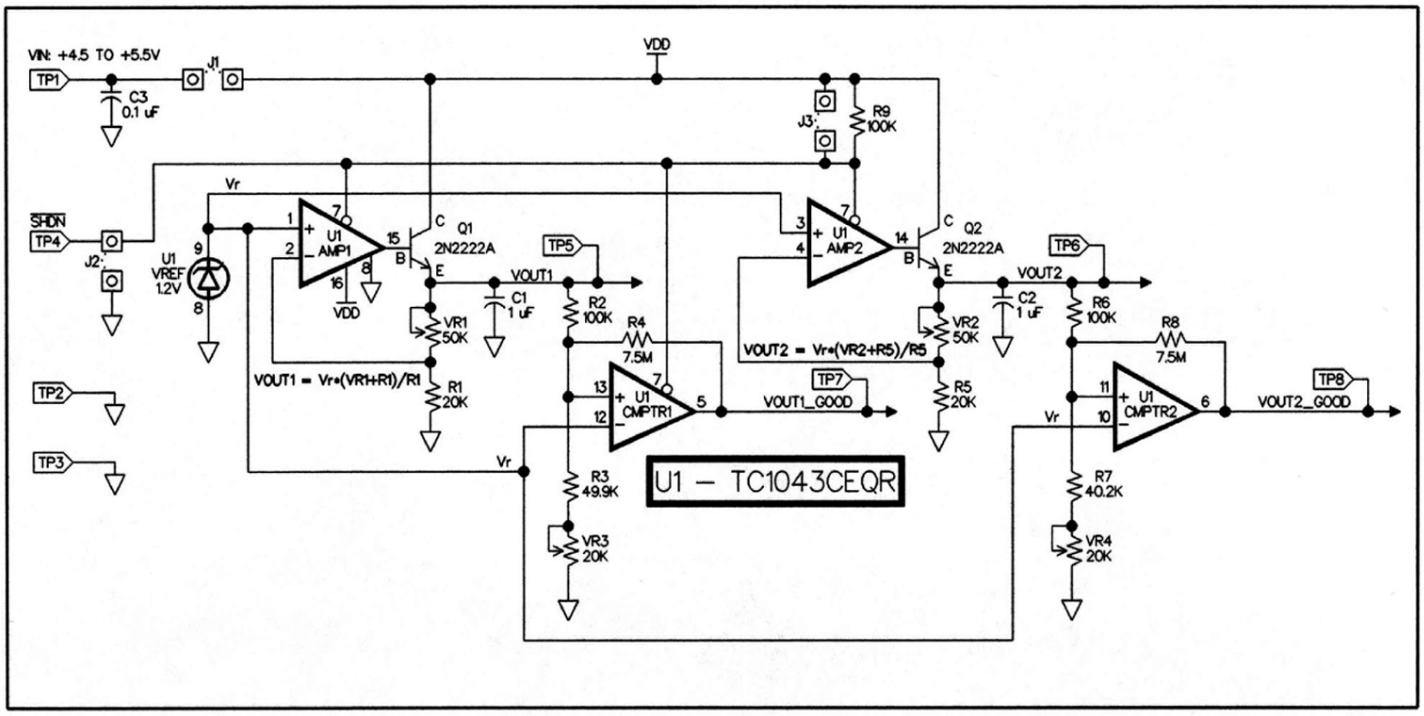


Figure 11. TC1043 Demo Card Schematic

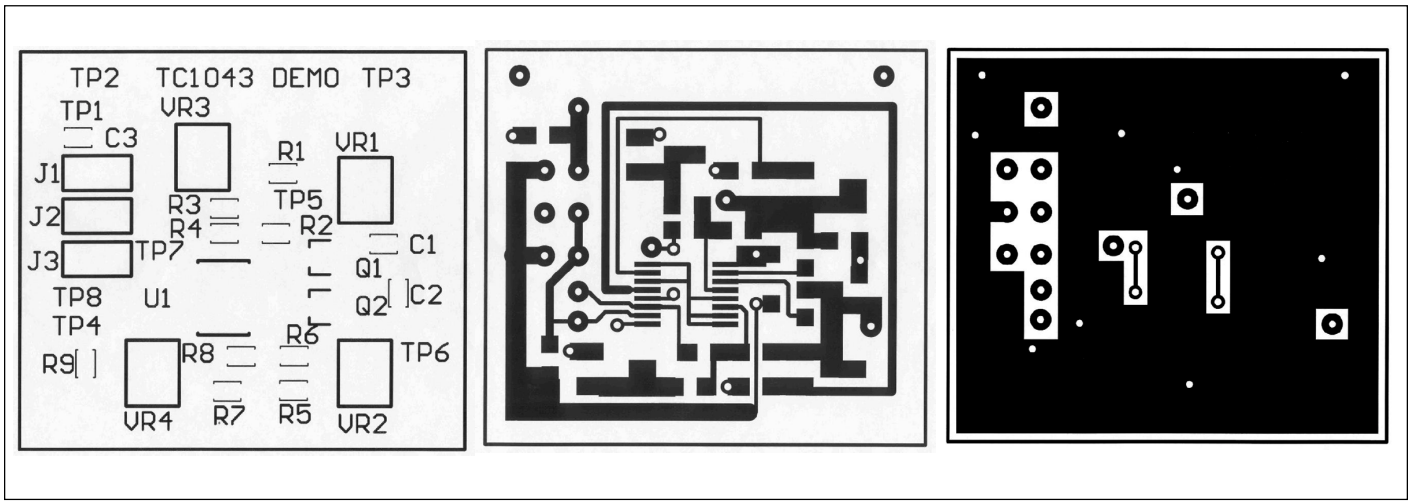


Figure 12. TC1043 Demo Card Assembly Drawing and Artwork

Table 1. TC1043 Demo Card Test Points

Test Font	Voltage Measurement
TP1	Demo Card Power Supply Input [+4.5V to +5.5V]
TP2	Ground
TP3	Ground
TP4	TC1043 /SHDN Input (Active Low)
TP5	Adjustable LDO Regulator Output Voltage #1 (V_{OUT1})
TP6	Adjustable LDO Regulator Output Voltage #2 (V_{OUT2})
TP7	Power Good Flag for LDO Regulator #1 (V_{OUT1_GOOD})
TP8	Power Good Flag for LDO Regulator #2 (V_{OUT2_GOOD})

Table 2. TC1043 Demo Card Test Points

Jumper	Current Measurement / Jumper Function
J1	TC1043 Demo Card Supply Current
J2 1,2)	TC1043 Demo Cad Shutdown (See Notes
J3	TC1043 Demo Card Enable (See Notes 1, 2)

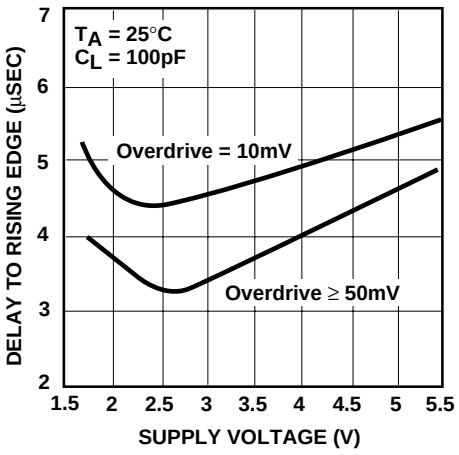
NOTES: 1. Never connect both J2 and J3 Jumpers simultaneously.
2. If jumpers J2 and J3 are ‘OPEN’, the Demo Card will default to the ‘ENABLE’ mode.

Table 3. TC1043 Demo Card Adjustments

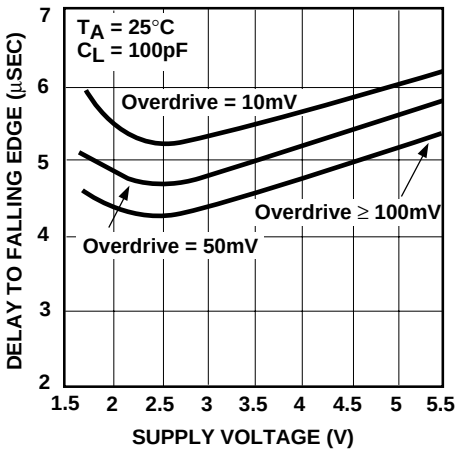
Potentiometer	Adjustments
VR1	LDO Regulator Voltage #1 (V_{OUT1})
VR2	LDO Regulator Voltage #2 (V_{OUT2})
VR3	Power Good Flag Threshold for LDO Regulator #1 (V_{OUT1_GOOD})
VR4	Power Good Flag Thresh old for LDO Regulator #2 (V_{OUT2_GOOD})

TYPICAL CHARACTERISTICS

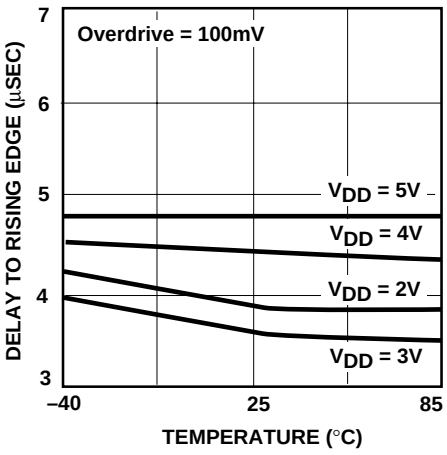
Comparator
Propagation Delay vs. Supply Voltage



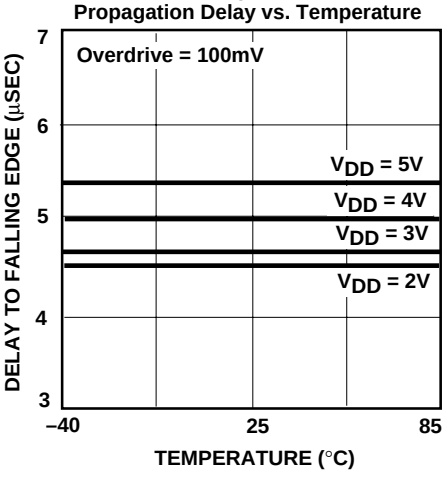
Comparator
Propagation Delay vs. Supply Voltage



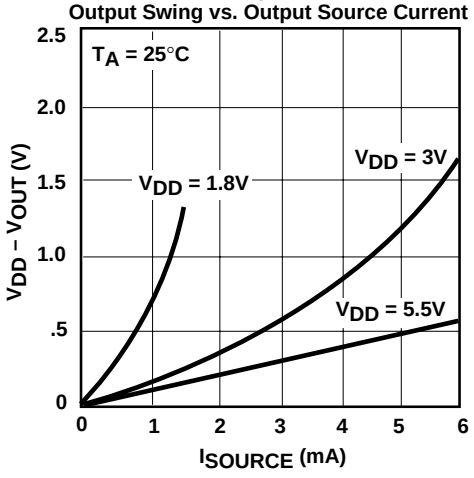
Comparator
Propagation Delay vs. Temperature



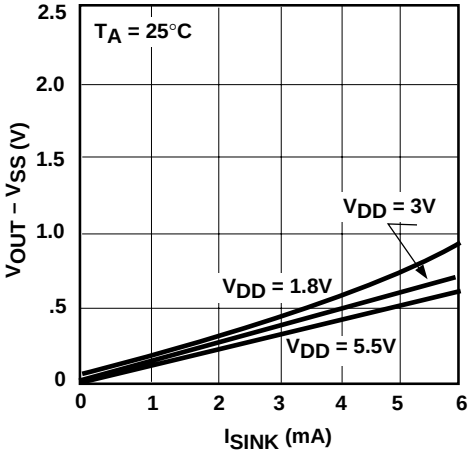
Comparator
Propagation Delay vs. Temperature



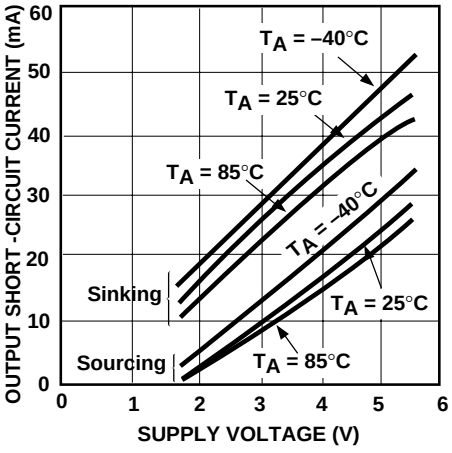
Comparator
Output Swing vs. Output Source Current



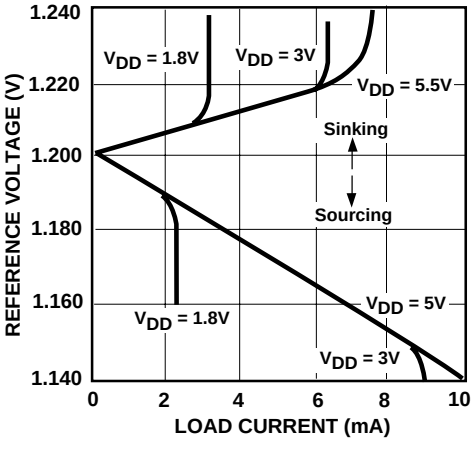
Comparator
Output Swing vs. Output Sink Current



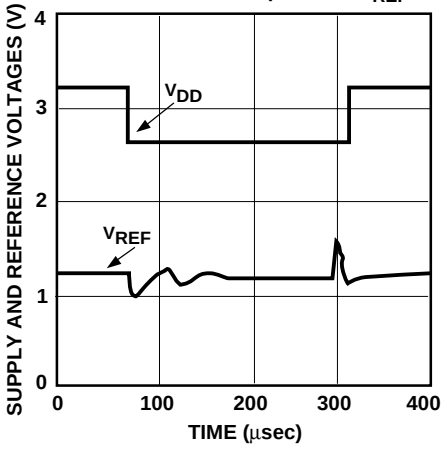
Comparator
Output Short-Circuit Current vs. Supply Voltage



Reference Voltage vs. Load Current

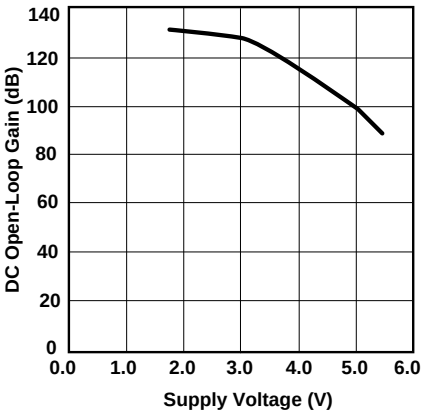


Line Transient Response of V_{REF}

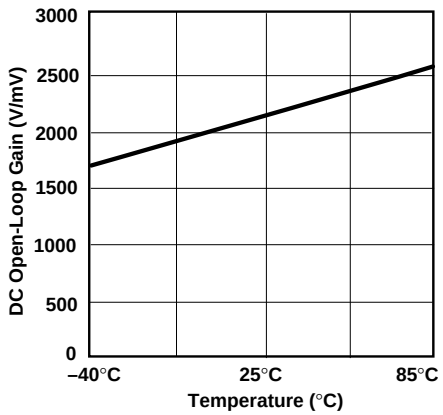


TYPICAL CHARACTERISTICS

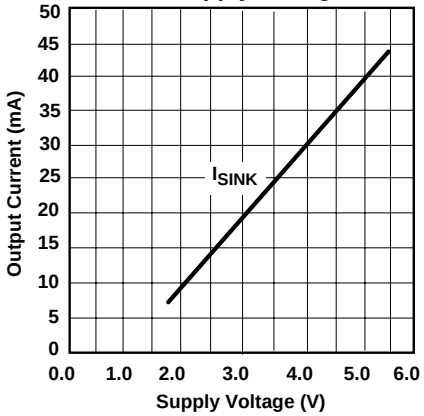
**Op Amp
DC Open-Loop Gain
vs. Temperature**



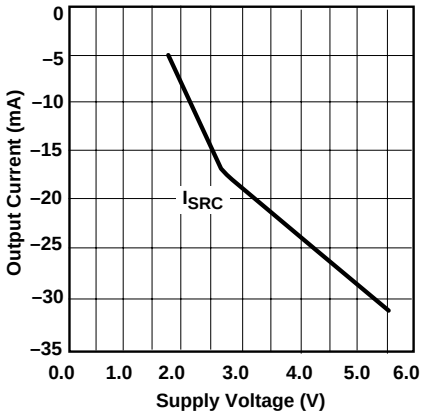
**Op Amp
DC Open-Loop Gain
vs. Temperature**



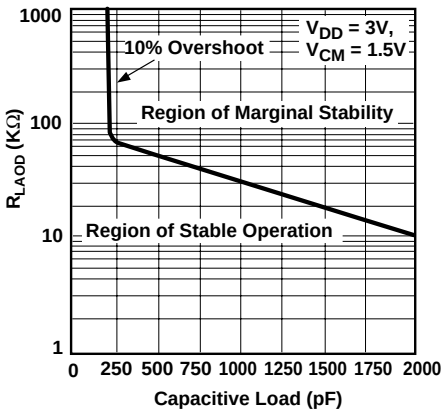
**Op Amp
Short-Circuit Current
vs. Supply Voltage**



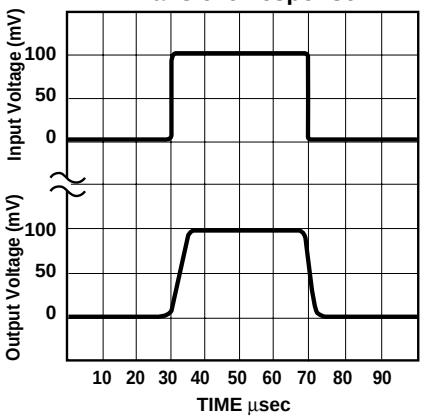
**Op Amp
Short-Circuit Current
vs. Supply Voltage**



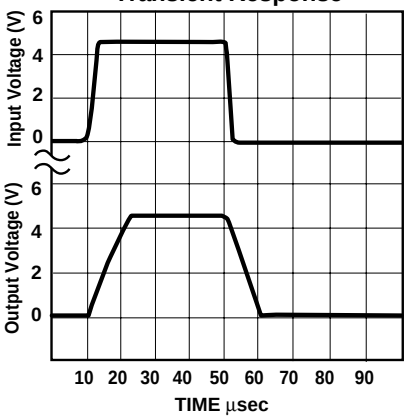
**Op Amp
Load Resistance
vs. Load Capacitance**



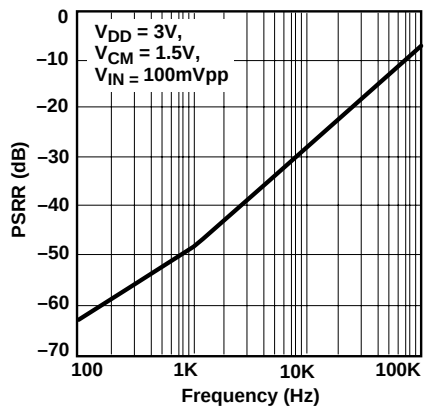
**Op-Amp Small-Signal
Transient Response**



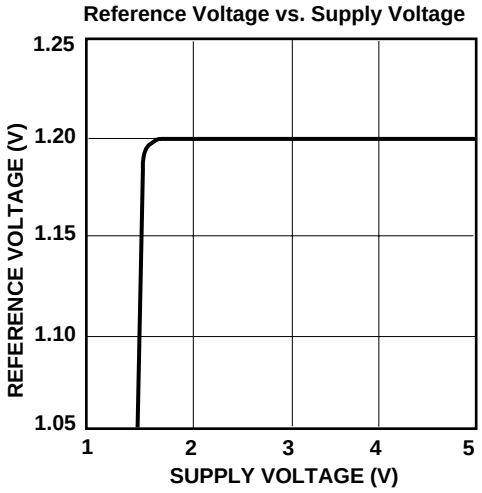
**Op-Amp Large-Signal
Transient Response**

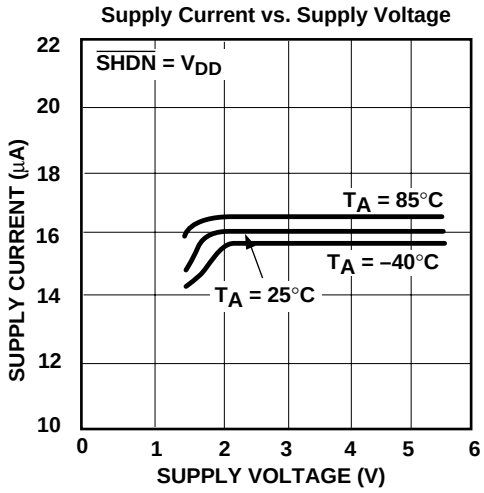


**Op Amp
Power Supply Rejection Ratio
(PSRR) vs. Frequency**



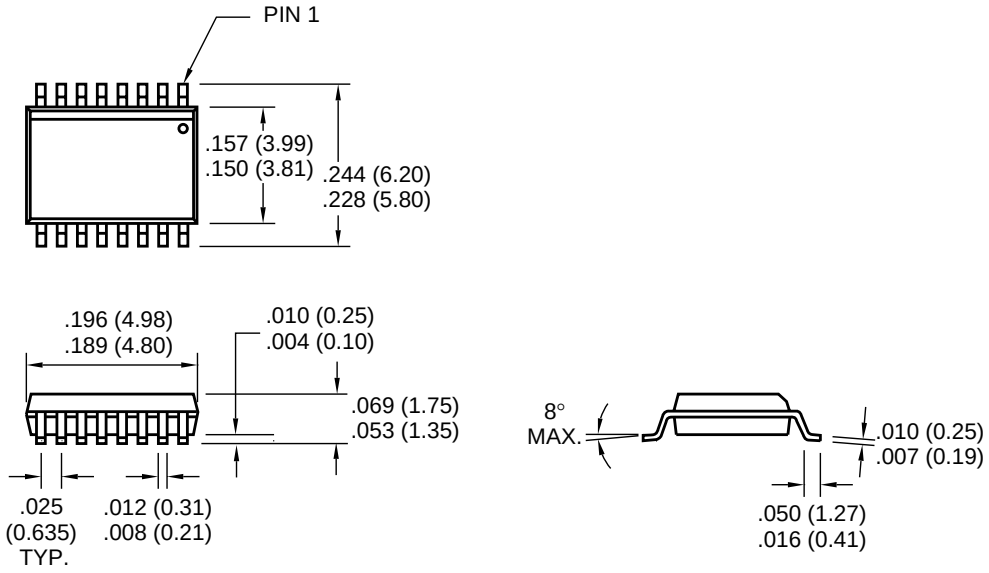
TYPICAL CHARACTERISTICS





PACKAGE DIMENSIONS

16-Pin QSOP



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