

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

# T B 6 5 2 4 F N

## DC MOTOR DUAL FULL BRIDGE DRIVER (H-SWITCH)

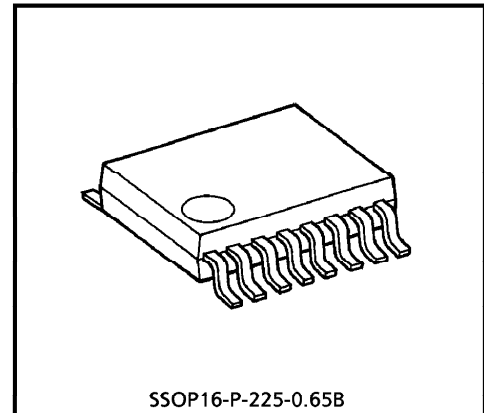
The TB6524FN is a bridge driver most suitable for switching between normal rotation and reverse rotation and can control three modes, normal rotation, reverse rotation, and stop.

The driver is capable of handling output current of 100mA.

Fixed current operation is also available as the control method.

### FEATURES

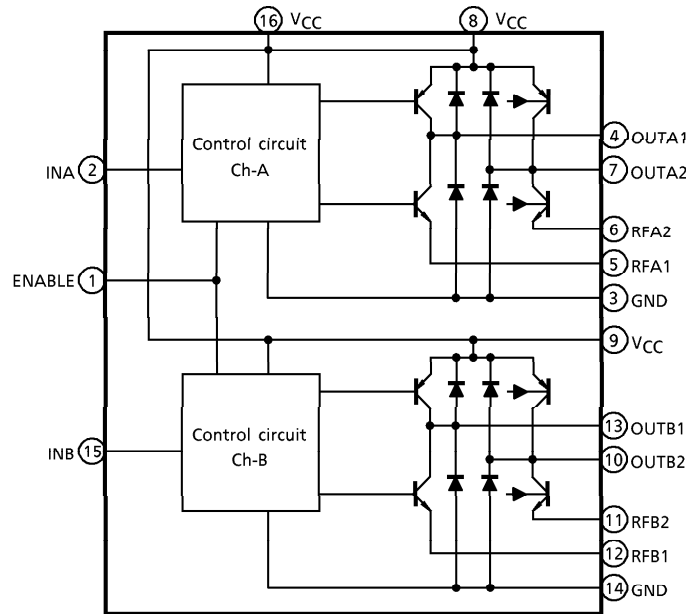
- Operating voltage range :  $V_{CC} = 1.5 \sim 7.0V$   
(normal operation)  
 $V_{CC} = 2.0 \sim 7.0V$   
(fixed current operation)
- Output current :  $I_{OUT} = 100mA$
- Built-in diode for absorbing counter electromotive force
- Built-in enable terminal



SSOP16-P-225-0.65B

Weight : 0.07g (Typ.)

### BLOCK DIAGRAM



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**PIN FUNCTION**

PIN No.	SYMBOL	DESCRIPTION
1	ENABLE	Enable signal input, Hi : Enabled, Low : All output OFF
2	INA	Channel A input signal terminal
3	GND	Ground terminal
4	OUTA1	Channel A output terminal
5	RFA1	Channel A : Output current is set by external resistance.
6	RFA2	Channel A : Output current is set by external resistance.
7	OUTA2	Channel A output terminal
8	V <sub>CC</sub>	Power supply
9	V <sub>CC</sub>	Power supply
10	OUTB2	Channel B output terminal
11	RFB2	Channel B : Output current is set by external resistance.
12	RFB1	Channel B : Output current is set by external resistance.
13	OUTB1	Channel B output terminal
14	GND	Ground terminal
15	INB	Channel B input signal terminal
16	V <sub>CC</sub>	Logic power supply

⑧ V<sub>CC</sub>, ⑨ V<sub>CC</sub>, ⑩ V<sub>CC</sub>, ③ GND and ⑭ GND must be connected to V<sub>CC</sub> or GND.

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**FUNCTION**

INPUT			OUTPUT			
INA	INB	ENABLE	OUTA1	OUTA2	OUTB1	OUTB2
H	H	H	H	L	H	L
L	L	H	L	H	L	H
H	L	H	H	L	L	H
L	H	H	L	H	H	L
H/L	H/L	L	∞	∞	∞	∞

∞ : High impedance

(Note) Before you change "Enable" to Low from High on the operating, change to Low both "INA" and "INB".

**MAXIMUM RATING (Ta = 25°C)**

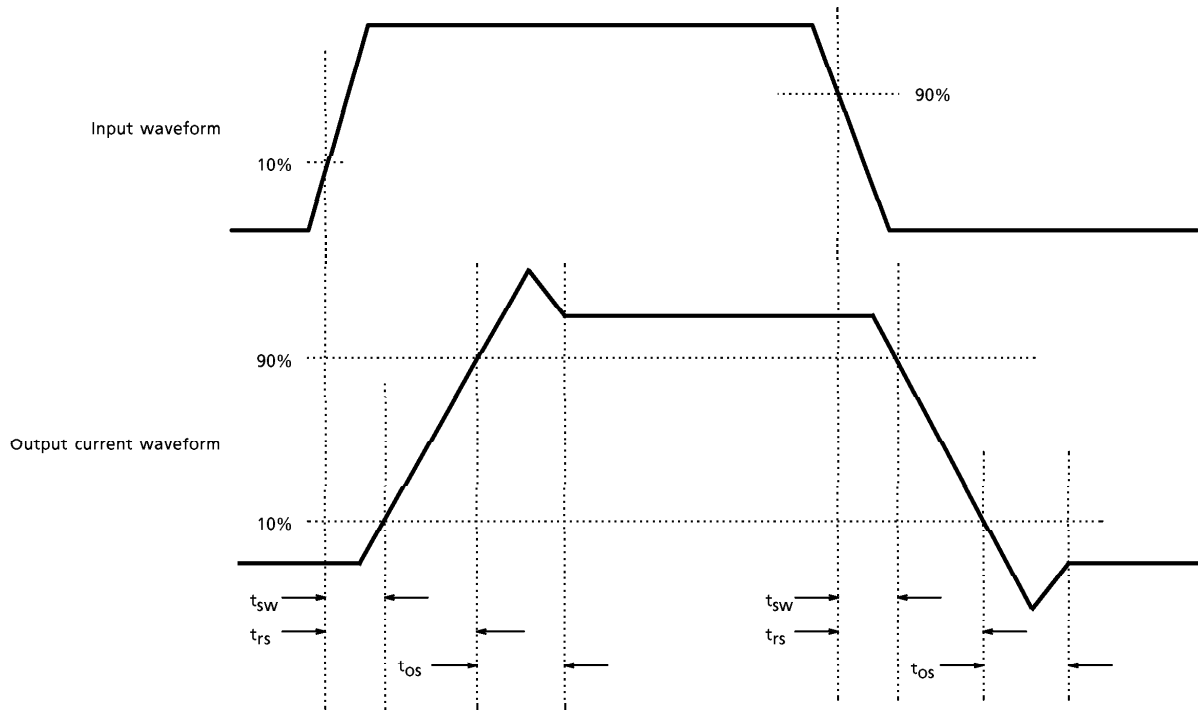
CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V <sub>CC</sub> (Max)	8	V
Output Current	I <sub>OUT</sub>	0.1	A
Power Dissipation (Tc = 25°C)	P <sub>D</sub>	0.5 (Note)	W
Operating Temperature	T <sub>opr</sub>	- 30~75	°C
Storage Temperature	T <sub>stg</sub>	- 55~150	°C

(Note) IC single unit

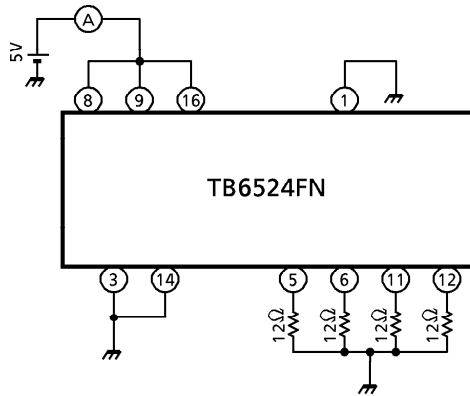
**ELECTRICAL CHARACTERISTICS** (Ta = 25°C, VCC = 5V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Current	I <sub>CC1</sub>	1	Standby (ENABLE OFF)	—	0.1	1.0	μA
	I <sub>CC2</sub>	2	Normal / reverse (for 2 channels), output OPEN	—	32	45	mA
Output Saturation Voltage	Upper V <sub>SAT</sub> U-1	3	I <sub>OUT</sub> = 100mA at normal / reverse	—	0.2	0.3	V
	Lower V <sub>SAT</sub> L-1		I <sub>OUT</sub> = 100mA at normal / reverse	—	0.2	0.3	
	Upper V <sub>SAT</sub> U-2		I <sub>OUT</sub> = 50mA at normal / reverse	—	0.1	0.25	
	Lower V <sub>SAT</sub> L-2		I <sub>OUT</sub> = 50mA at normal / reverse	—	0.1	0.25	
Setting Output Current	I <sub>OUT C</sub>	4	12Ω between RFA1, 2 / RFB1, and 2-GND Load 7.5Ω	55	65	75	mA
Output Current V <sub>CC</sub> Dependency	$\frac{\Delta I_{OUTC}}{\Delta V_{CC}}$	5	I <sub>OUT C</sub> = 10~100mA (R <sub>f</sub> : 8Ω, 80Ω) V <sub>CC</sub> = 2.0~7.0V Load 5Ω	-8		5	%
Output Current Switching Duration	t <sub>sw</sub>	—	560μH (7.5Ω) R <sub>f</sub> = 16Ω	—	1.0	—	μs
	t <sub>rs</sub>			—	6.0	—	
Overshoot Duration	t <sub>os</sub>			—	2.0	—	
Input Voltage	V <sub>IH</sub>	6	INA, INB, ENABLE	1.5	—	V <sub>CC</sub>	V
	V <sub>IL</sub>			0	—	0.3	
Input Current	I <sub>in</sub>	7	Sync V <sub>IN</sub> = 5.0V Input terminal 4.7kΩ	—	430	550	μA
Output Transistor Leak Current	Upper I <sub>LU</sub>	8	V <sub>L</sub> = 7V	—	—	30	μA
	Lower I <sub>LL</sub>			—	—	30	

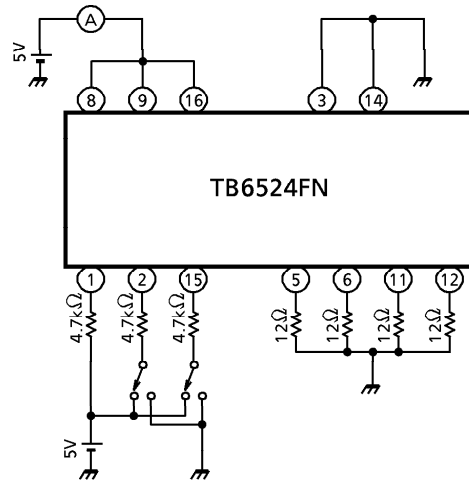
$t_{sw}$ ,  $t_{rs}$ ,  $t_{os}$



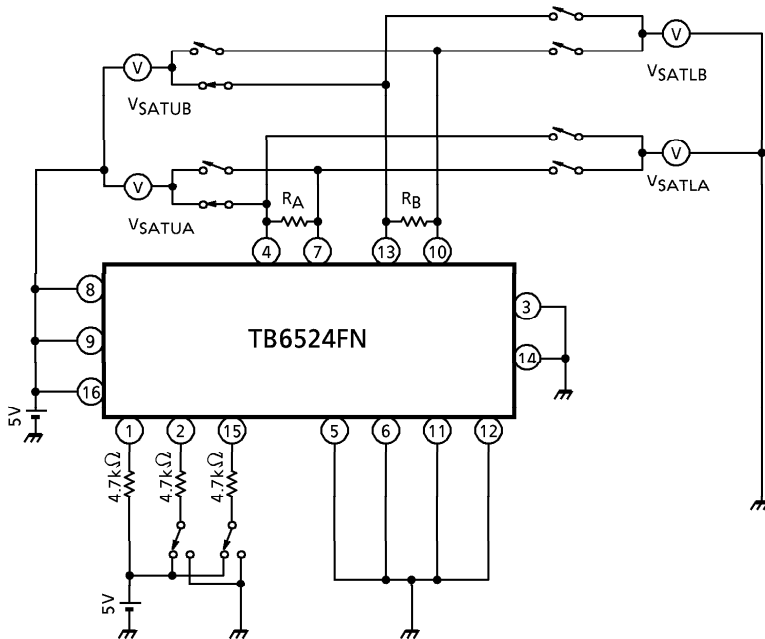
TEST CIRCUIT 1  $I_{CC1}$



TEST CIRCUIT 2  $I_{CC2}$

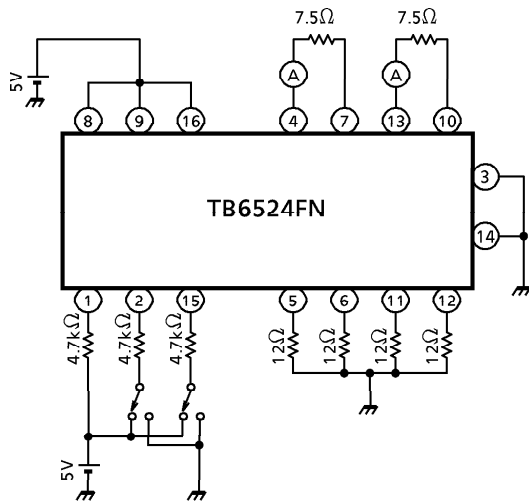


TEST CIRCUIT 3  $V_{SATU-1, 2}/V_{SATL1, 2}$

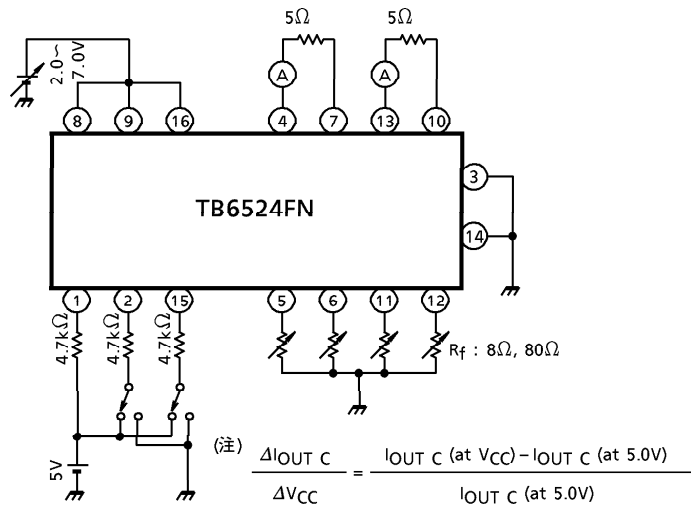


(Note) Set  $R_A$  and  $R_B$  so that  $I_{OUT} = 50mA$  and  $100mA$  is satisfied.

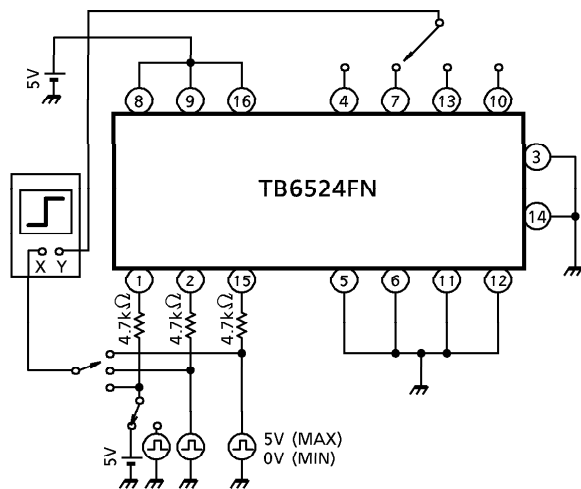
TEST CIRCUIT 4  $I_{OUT C}$



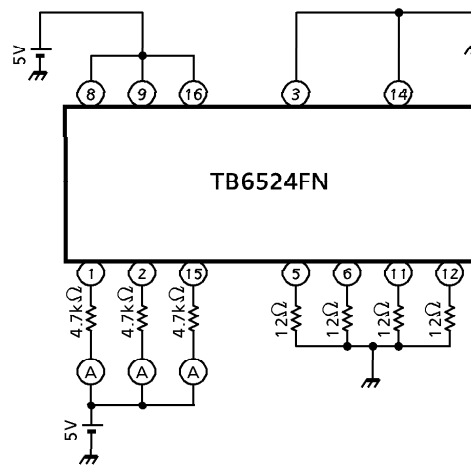
TEST CIRCUIT 5  $\Delta I_{OUT C}$



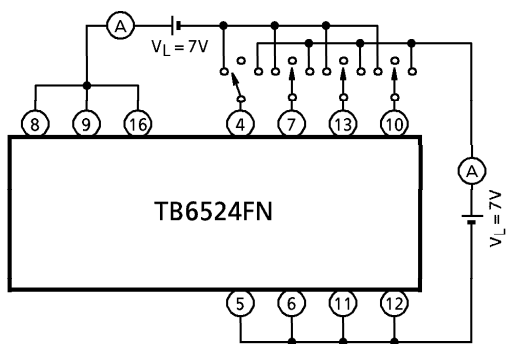
TEST CIRCUIT 6  $V_{IH}/V_{IL}$

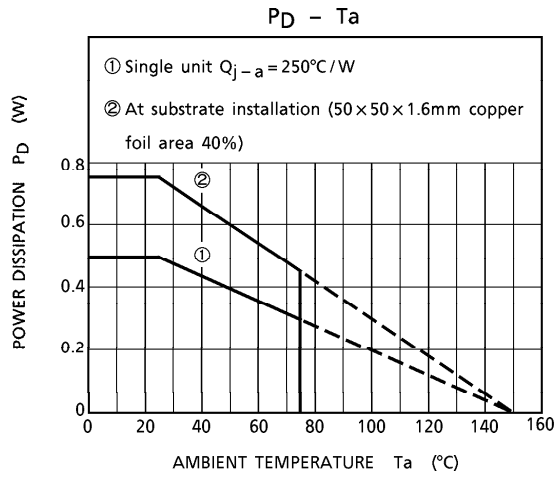


TEST CIRCUIT 7  $I_{in}$



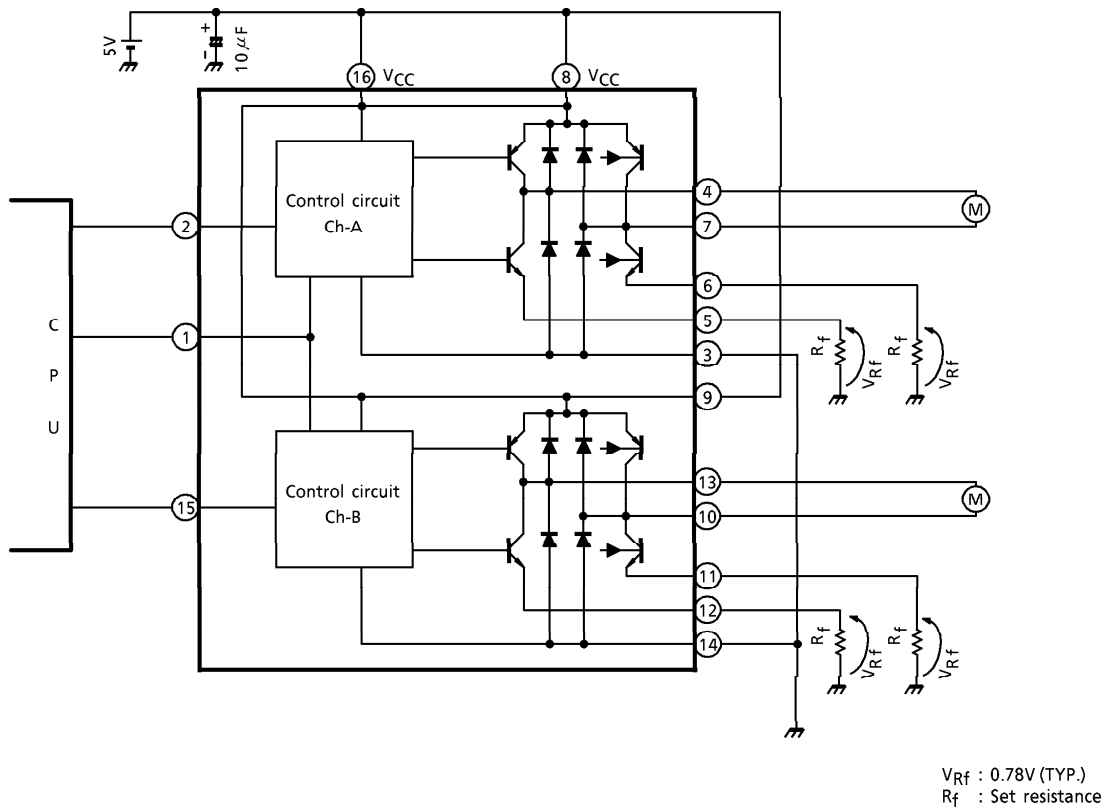
TEST CIRCUIT 8  $I_{LU}/I_{LL}$







APPLICATION CIRCUIT

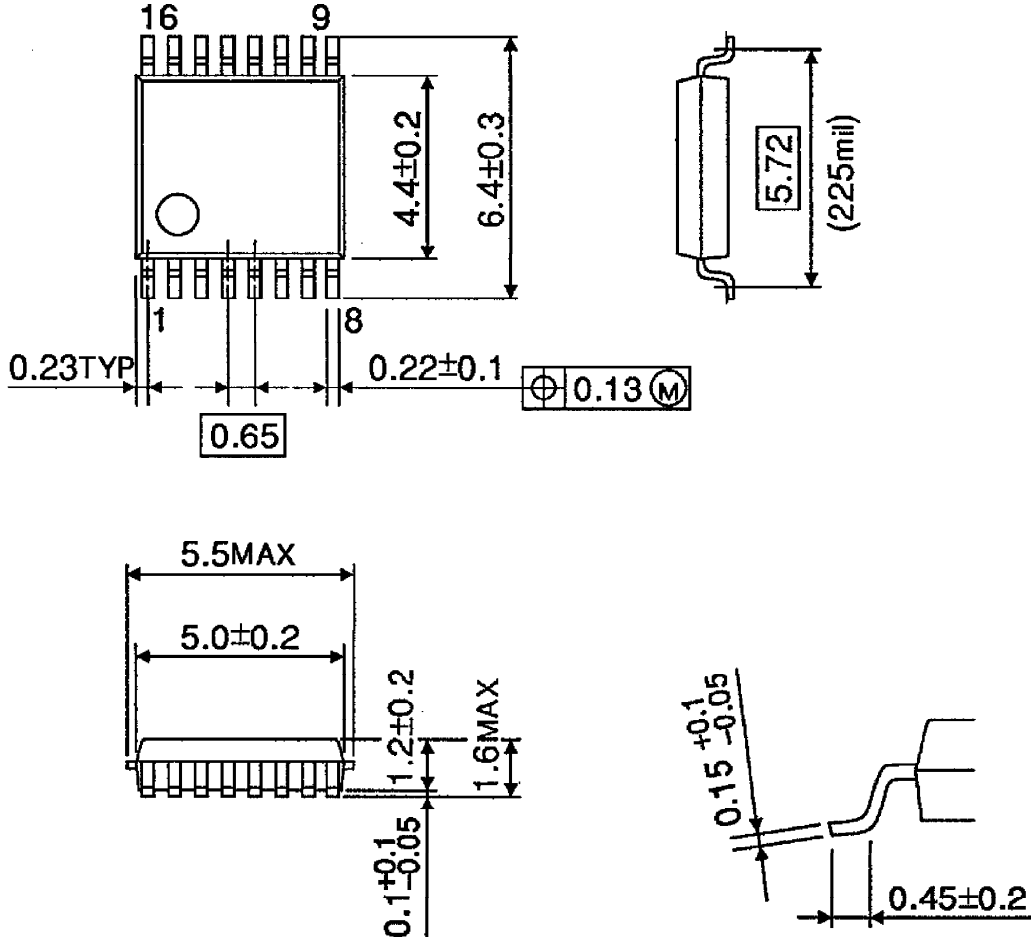


(Note) Utmost care is necessary in the design of the output line,  $V_{CC}$  and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

OUTLINE DRAWING

SSOP16-P-225-0.65B

Unit : mm



Weight : 0.07g (Typ.)