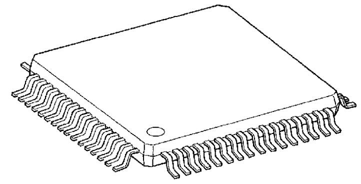
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB6519AF

VIDEO CAMERA CYLINDER MOTOR CONTROLLERS AND CAPSTAN MOTOR CONTROLLERS

The TB6519AF is a single-chip IC for video camera cylinder motor controllers and capstan motor controllers. The cylinder section is a soft-switching pre-driver based on a 3-phase full-wave sensorless driver and 180° trapezoidal wave commutation control. The capstan section is a soft-switching pre-driver based on 3-phase full-wave drive and pseudo-sine wave commutation control.



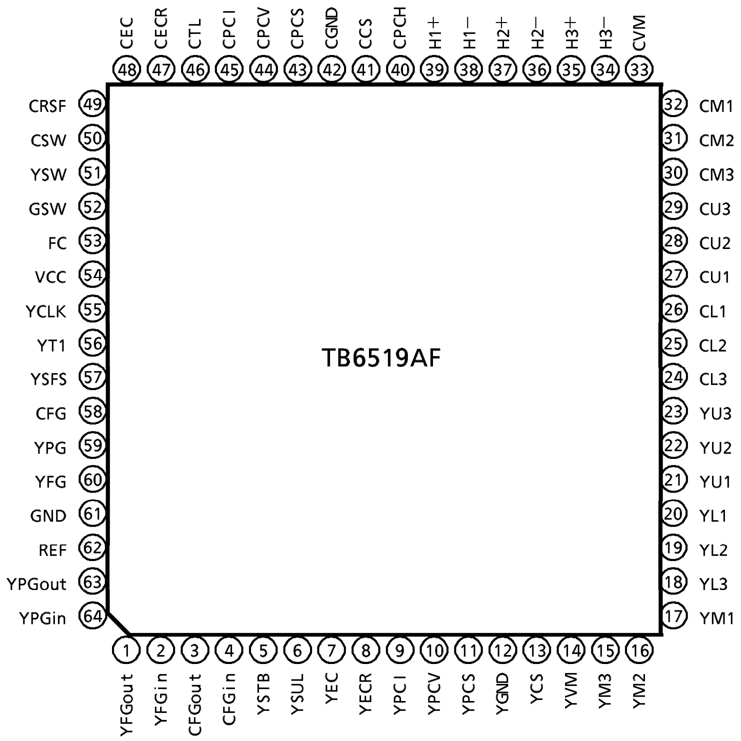
LQFP64-P-1010-0.50A

Weight : 0.34g (Typ.)

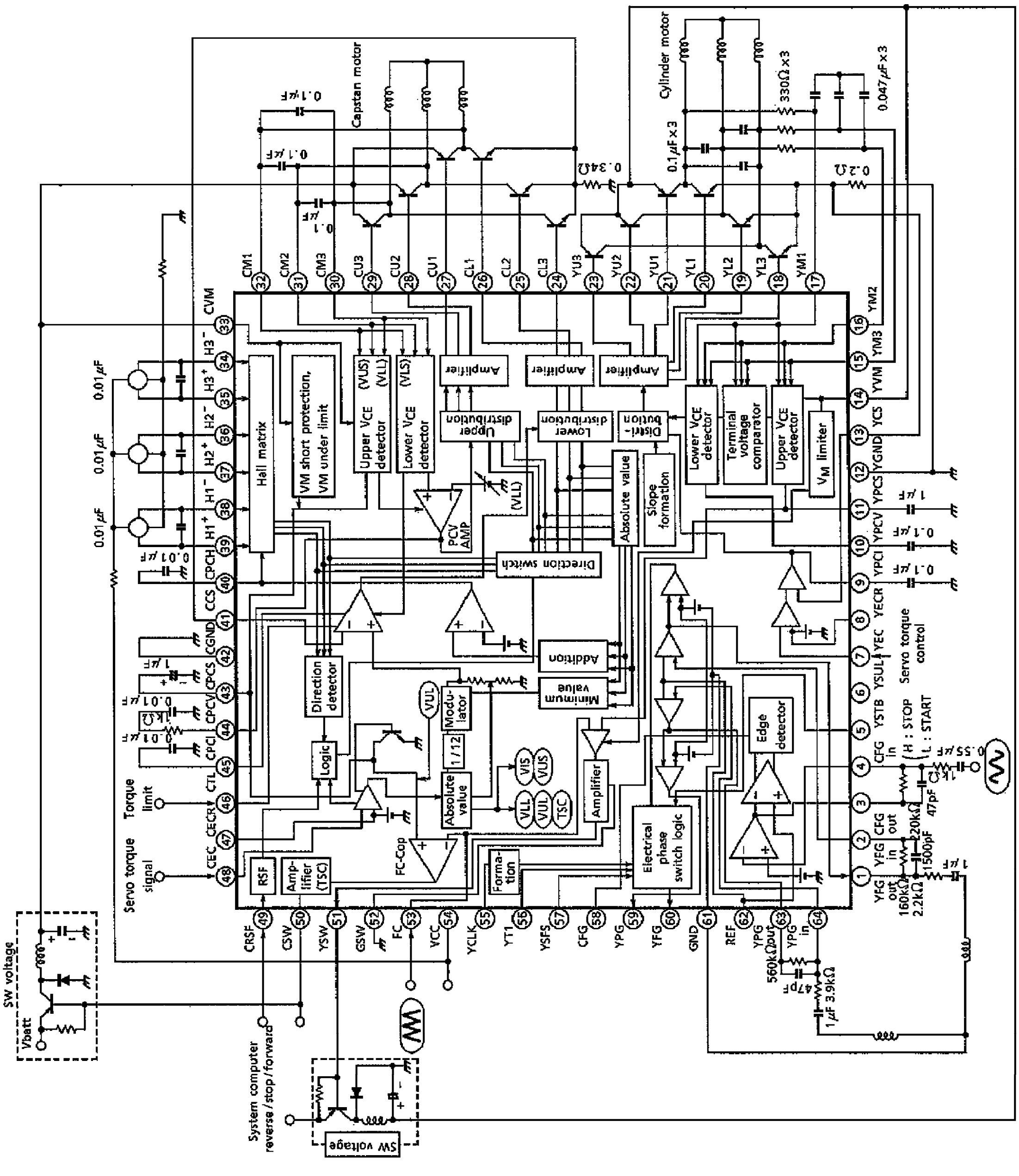
FEATURES

- Output current : 10mA (MIN.) (At $V_{CC} = 3.5V$)
- Operating voltage : $V_{CC} = 2.8\sim5.5V$
- Motor voltage : $V_M = 3.0\sim12V$

PIN CONNECTION



BLOCK DIAGRAM



TB6519AF – 3

PIN FUNCTION

PIN No.	SYMBOL	FUNCTION DESCRIPTION
1	YFGout	Cylinder part FG amplifier output terminal
2	YFGin	Cylinder part FG input terminal
3	CFGout	Capstan part FG amplifier output terminal
4	CFGin	Capstan part FG input terminal
5	YSTB	Cylinder part stand-by switch input terminal
6	YSUL	Cylinder part sloop voltage terminal
7	YEC	Cylinder part torque control input terminal
8	YECR	Cylinder part torque control reference input terminal
9	YPCI	Cylinder part current feedback phase compensation
10	YPCV	Cylinder part voltage feedback phase compensation
11	YPCS	Cylinder part switching voltage control output terminal
12	YGND	Cylinder part ground terminal
13	YCS	Cylinder part current detection input terminal
14	YVM	Cylinder motor power voltage terminal
15	YM3	Cylinder motor coil terminal
16	YM2	〃
17	YM1	〃
18	YL3	Cylinder motor lower side pre-drive output terminal
19	YL2	〃
20	YL1	〃
21	YU1	Cylinder motor upper side pre-drive output terminal
22	YU2	〃
23	YU3	〃
24	CL3	Capstan motor low side pre-driver output terminal
25	CL2	〃
26	CL1	〃
27	CU1	Capstan motor upper side pre-driver output terminal
28	CU2	〃
29	CU3	〃
30	CM3	Capstan motor coil terminal
31	CM2	〃
32	CM1	〃
33	CVM	Capstan motor mains power terminal

PIN No.	SYMBOL	FUNCTION DESCRIPTION
34	H3−	Capstan motor hall element input terminal
35	H3+	〃
36	H2−	〃
37	H2+	〃
38	H1−	Capstan motor hall element input terminal
39	H1+	〃
40	CPCH	Capstan part hall amplifier phase compensation
41	CCS	Capstan part current detection input terminal
42	CGND	Capstan part ground terminal
43	CPCS	Capstan part switching voltage control output
44	CPCV	Capstan part voltage feedback phase compensation
45	CPCI	Capstan part current feedback phase compensation
46	CTL	Capstan part torque limit
47	CECR	Capstan part torque control reference voltage
48	CEC	Capstan part torque control input terminal
49	CRSF	Capstan part direction control input terminal
50	CSW	Capstan part switching pre-driver output terminal
51	YSW	Cylinder part switching pre-driver output terminal
52	GSW	Switching voltage part ground terminal
53	FC	Switching comparator triangular-wave Input terminal
54	VCC	Capstan part ground terminal
55	YCLK	Cylinder part clock input terminal
56	YT1	Cylinder part test mode switch input terminal
57	YSFS	Cylinder part start-up frequency switch input
58	CFG	Capstan part FG wave output terminal
59	YPG	Cylinder part PG wave output terminal
60	YFG	Cylinder part FG wave output terminal
61	GND	FG and PG part ground terminal
62	REF	FG and PG part reference voltage terminal
63	YPGout	Cylinder part PG amplifier output terminal
64	YPGin	Cylinder part PG input terminal

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	6	V
Motor Supply Voltage (Note 1)	V_M	14	V
Supply I / O Voltage (Note 2)	V_{SWB}	14	V
Output Terminal Voltage (Note 3)	V_N	14	V
Input Terminal Voltage (Note 4)	V_I	$-0.3\sim V_{CC}+0.3$	V
Power Dissipation	P_D	0.95 (Note 5)	W
Operating Temperature	T_{opr}	−20~75	°C
Storage Temperature	T_{stg}	−55~125	°C

(Note 1) Pin No. = 14, 33
(Note 2) Pin No. = 50, 51
(Note 3) Pin No. = 15, 16, 17, 21, 22, 23, 27, 28, 29, 30, 31, 32
(Note 4) Pin No. = 2, 4, 5, 7, 8, 13, 41, 46, 47, 48, 49, 53, 55, 56, 57, 62, 64
(Note 5) Element

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{CC} = 3.5V)
Cylinder part

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
1	Supply Current (1)	$I_{CC\,(1)}$	1	Shared use of the cylinder area and capstan area during operations	—	17.9	30	mA
2	Supply Current (2)	$I_{CC\,(2)}$	1	During STB, during STOP (CAP)	—	10.6	20	mA
3	ECR Voltage	V_{ECR}	1		2.14	2.24	2.54	V
4	Torque Control Input Current	YI_{EC}	1	YEC = 0V	−5	−0.5	—	μA
5	Torque Control Input Offset Voltage	ΔEC	2		−100	−15	100	mV
6	I / O Gain	YGio	2		0.13	0.15	0.17	
7	Maximum Output Voltage	YCSmax	2	R_{YCS} = 0.27Ω	145	160	183	mV
8	Lower Side Output Voltage (1)	$V_{L\,(1)}$	3	YCS = 54mV	0.2	0.39	0.6	V
9	Lower Side Output Voltage (2)	$V_{L\,(2)}$	3	YECR = 2.24V, YEC = 0V	0.45	0.66	0.85	V
10	Upper Side Drive Current	I_U	4		—	—	−10	mA
11	Lower Side Drive Current	I_L	4		10	—	—	mA
12	PCS Operating Point (1)	$V_{PCS\,(1)}$	5	YEC = YECR = 2.24V V_{PCS} = 1.75V	0.36	0.47	0.58	V

Cylinder part

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
13	PCS Operating Point (2)	V_{PCS} (2)	5	YEC = 0V, YECR = 2.24V V_{PCS} = 1.75V	0.60	0.79	0.98	V
14	PCS Gain	YG_{PCS}	5		4.5	6.5	8.5	
15	SW Reg Drive Current (1)	I_{SW} (1)	5	VM1 = 6V, YEC = YECR = 2.24V	3	4.5	—	mA
16	SW Reg Drive Current (2)	I_{SW} (2)	5	VM1 = 6V YEC = 0V, YECR = 2.24V	11	16.6	—	mA
17	SW Reg Comparator Offset Voltage	ΔV_{FC}	5		−5	15	25	mV
18	FG Amplifier Gain	G_{FG}	6	V_{p-p} = 1.5mV, f = 1kHz	45	—	—	dB
19	YFG High Level	YFG (H)	7	I_{YFG} = −100μA	2.0	3.4	—	V
20	YFG Low Level	YFG (L)	7	I_{YFG} = 100μA	—	0.1	1.5	V
21	PG Amplifier Open Loop Gain	G_{PG}	—		—	70	—	dB
22	PG Amplifier Offset Voltage	ΔPGin	7		0.45	0.5	0.6	V
23	YPG High Level	YPG (H)	7	I_{YPG} = −10μA	2.0	3.0	—	V
24	YPG Low Level	YPG (L)	7	I_{YPG} = 100μA	—	0.03	1.0	V
25	Stand-By Voltage	STB_{on}	8		2.15	—	—	V
26	Stand-By Release Voltage	STB_{off}	8		—	—	1.0	V
27	Stand-By Input Current	I_{STB}	8	V_{STB} = 0V	−100	−35	—	μA
28	Start-Up Phase Switch Frequency 7.5Hz Setting Input	SFS (L)	9		—	—	1.05	V
29	Start-Up Phase Switch Frequency 15Hz Setting Input	SFS (H)	9		2.45	—	—	V
30	YVM Under Limit	YVML	5		1.87	2.5	3.13	V
31	YVM Short Protection	YVMS	5		0.26	0.76	1.00	V
32	Current Leak When Mains Power Off	I_{ML}	10	YVM = 6V	—	3	10	μA
33	Output Idle Voltage	YCSidle	2	R_{YCS} = 0.27Ω	—	0	5	mV

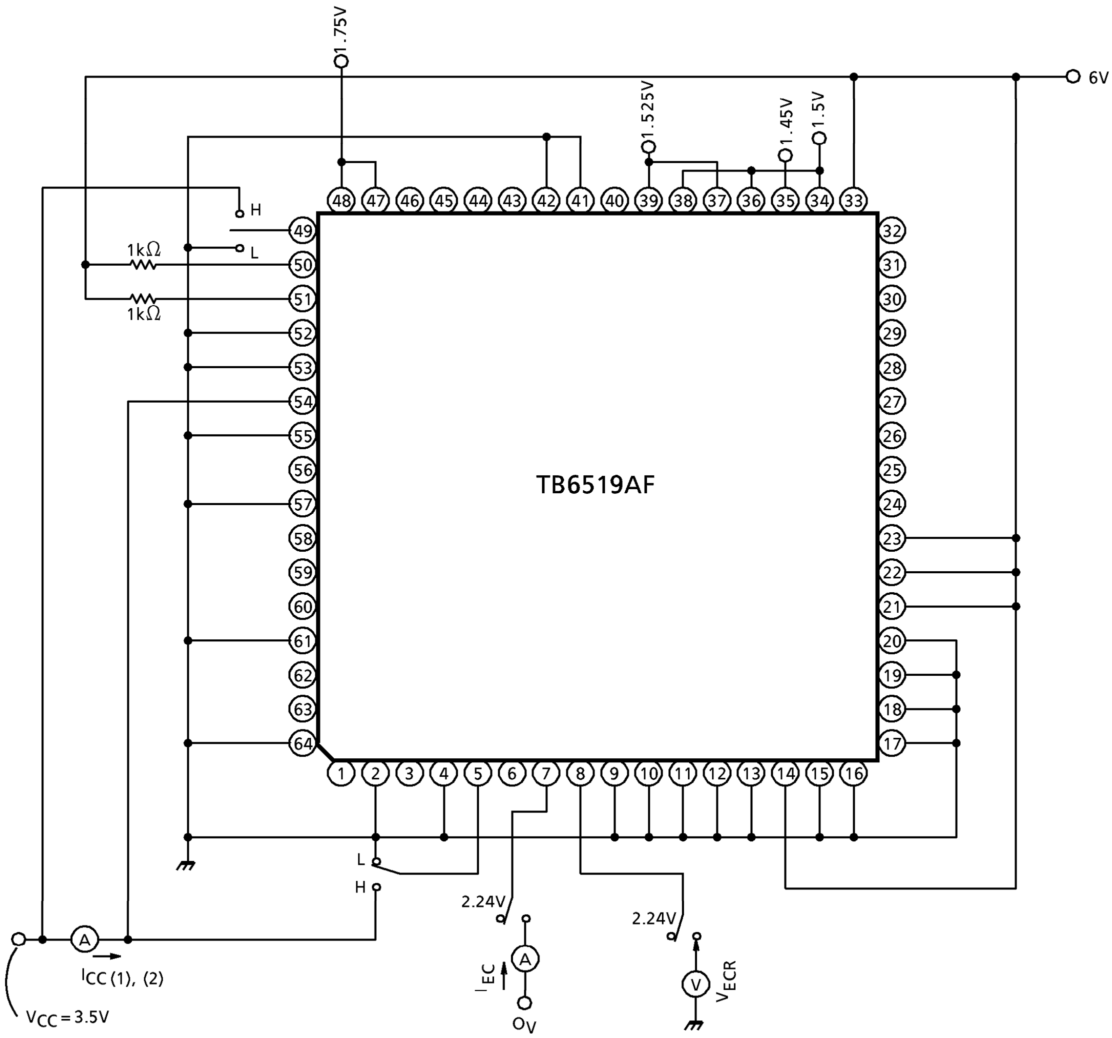
Capstan area

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
34	Torque Control Input Current	CI_{EC}	11	CEC = CECR = 1.75V	−2	−1	—	μA
35	Torque Control Reference Voltage	CE_{CR}	11		1.55	1.73	1.95	V
36	Torque Control Input Voltage	CE_{C}	12		0.5	—	3.0	V
37	Output Maximum Voltage	CCSmax	12	R_{CCS} = 0.34Ω	0.19	0.23	—	V
38	Torque Control I/O Gain	CGio	12		0.21	0.24	0.27	

Capstan area

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
39	Output Idle Voltage	CCSidle	12		—	0	4	mV
40	Torque Control Input Offset	CECofs	12		– 100	15	100	mV
41	Torque Control Dead Zone	CECdz	12		30	77	130	mV
42	Low Side V_{CE} Voltage (1)	CVLL (1)	13	CCS = 60mV	0.22	0.28	0.50	V
43	Low Side V_{CE} Voltage (2)	CVLL (2)	13	CEC = 0V, CTL = 1.0V	0.40	0.50	0.80	V
44	Hall Element Permissible Input Voltage	Hin	14		1.2	—	2.0	V
45	Hall Element Input Conversion Offset	Hofs	15		– 8	– 1	8	mV
46	TL-CS Offset	TLofs	16	CTL = 20mV	6	9.5	14	mV
47	Forward Rotation Control Voltage	Vf	17		—	—	0.87	V
48	Stop Control Voltage	Vs	17		1.27	—	2.23	V
49	Reverse Rotation Control Voltage	Vr	17		2.90	—	—	V
50	Ripple Cancel Rates	R	18	CCS = 60mV	8	13	18	%
51	Upper Side Drive MAX Current	CI_U	19		10	24	—	mA
52	Low Side Drive MAX Current	CI_L	19		—	– 16	– 10	mA
53	SW Power Voltage Input Offset	CSWofs	21		– 20	11	20	mV
54	SW Power Voltage Control Output Gain	CG_{PCS}	20		6	8	10	
55	SW Power Voltage Control Output Voltage (1)	VUD (1)	20	CEC = CECR, CPCS = 1.7V	0.3	0.40	0.65	V
56	SW Power Voltage Control Output Voltage (2)	VUD (2)	20	CEC = 0V, CTL = 0.2V CPCS = 1.7V	0.47	0.62	1.10	V
57	SW Power Voltage Output MAX Current	CI_{SWB}	20	CEC = 0V, CTL = 0.2V	15	22	—	mA
58	FG Amplifier Standard Voltage	CFG_{ref}	11		1.7	2.0	2.3	V
59	FG Amplifier Loop Gain	CG_{FG}	22	External 1kΩ, 220kΩ Input $3mV_{p-p}$, 1kHz	45	50	—	dB
60	FG Amplifier Output Voltage High Level	CFG_H	22		3	3.5	—	V
61	FG Amplifier Output Voltage Low Level	CFG_L	22		—	0.01	0.5	V
62	V_M Under Limit	CV_{ML}	23		1.13	1.52	1.88	V
63	V_M Short Protection	CV_{MS}	23		0.26	0.45	1.00	V

TEST CIRCUIT 1. $I_{CC\,(1)}$, $I_{CC\,(2)}$, V_{ECR}, YI_{EC}



No. 1 $I_{CC\,(1)}$

Set YSTB = 0V, YEC = 2.24V, YECR = 0V and CRSF = 0V and then measure the current flowing into the V_{CC} terminal.

No. 2 $I_{CC\,(2)}$

Set YSTB = 3.5V, YEC = YECR = 2.24V and CRSF = OPEN and then measure the current flowing into the V_{CC} terminal.

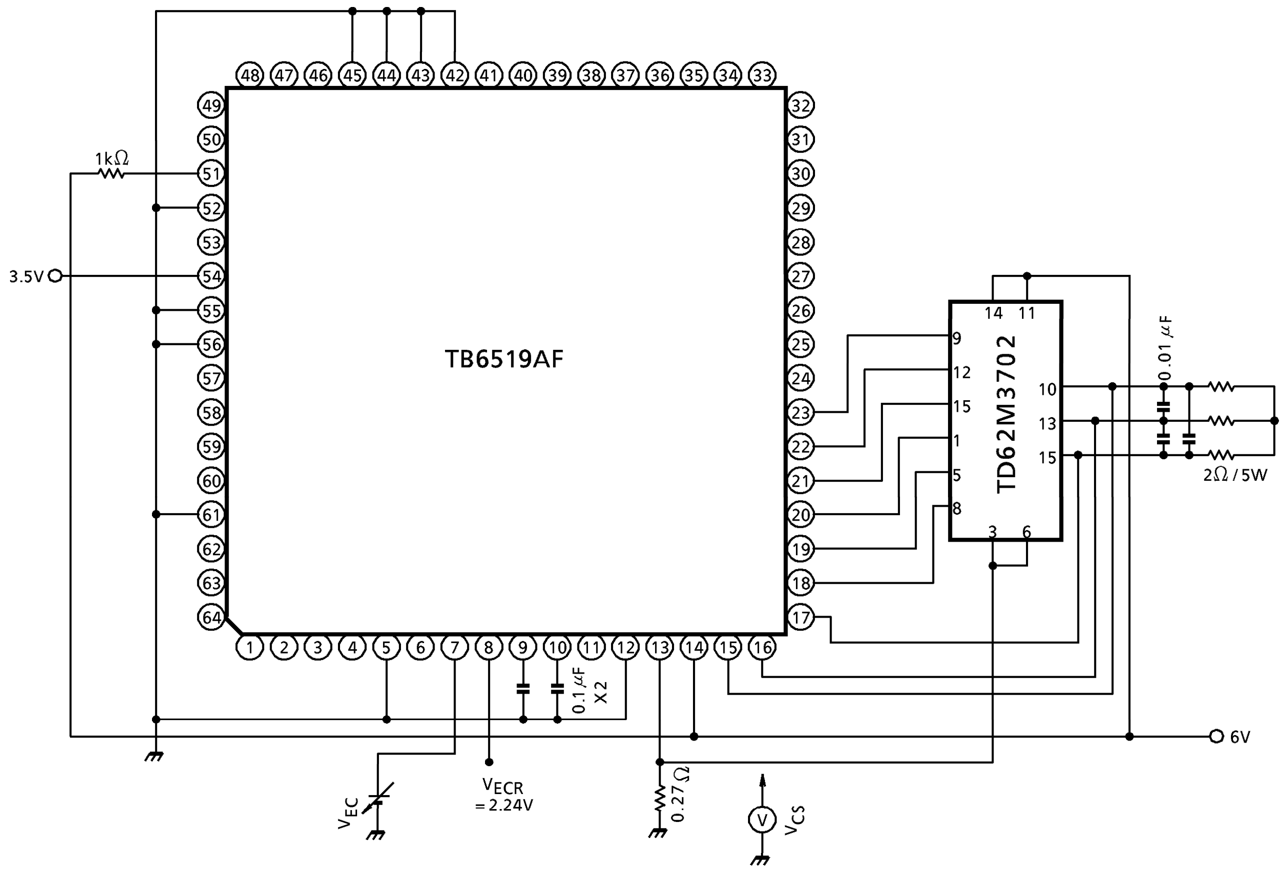
No. 3 V_{ECR}

Measure the potential of pin ⑧.

No. 4 YI_{EC}

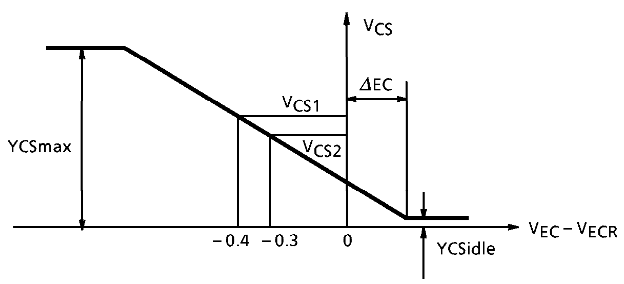
Measure the current flowing into pin ⑦ when YEC = 0V and YECR = 2.24V.

TEST CIRCUIT 2. ΔEC, YGio, YCSmax, YCSidle



No. 5 ΔEC, No. 6 YGio, No. 7 YCSmax, No. 33 YCSidle

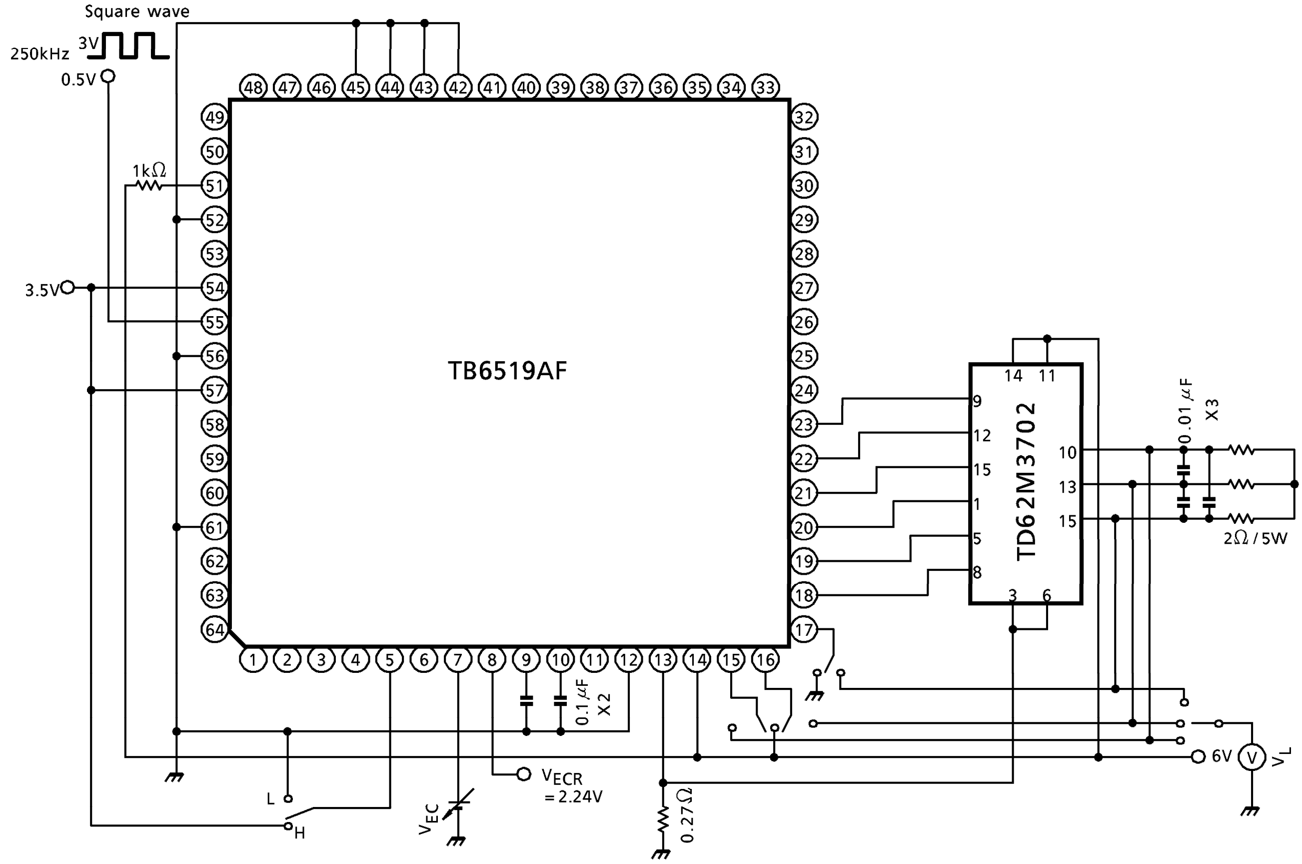
Set YECR = 2.24V, change YEC from 0V to 3V and then measure the potential of pin ⑬.



$$\Delta EC = V_{EC} - V_{ECR} \quad (V_{CS} \approx 0V)$$

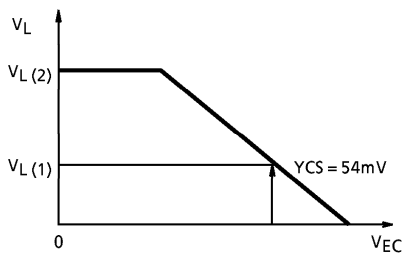
$$YGio = \frac{V_{CS1} - V_{CS2}}{0.1V}$$

TEST CIRCUIT 3. $V_{L\,(1)}$, $V_{L\,(2)}$



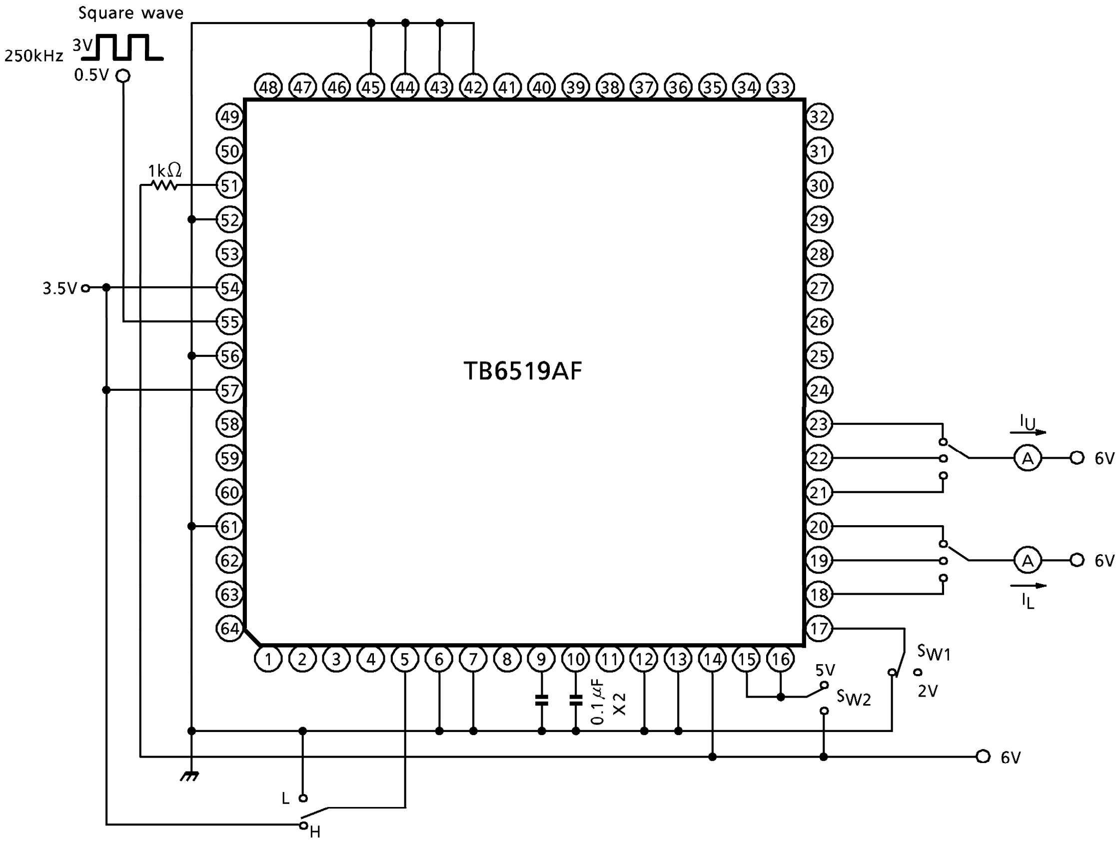
No. 8 $V_{L\,(1)}$, No. 9 $V_{L\,(2)}$

Change the YSTB terminal from H to L with YMI = 0V, YM2 = 6V and YM3 = 6V and then enter the following clock counts into the YCLK terminal in order to set the drive angle.
Connect the YM1, YM2 and YM3 terminals to PWTR after setting the drive angle and then carry out the measurement.



CLOCK	80	150	270
Terminal	YM3	YM1	YM2

TEST CIRCUIT 4. I_U, I_L

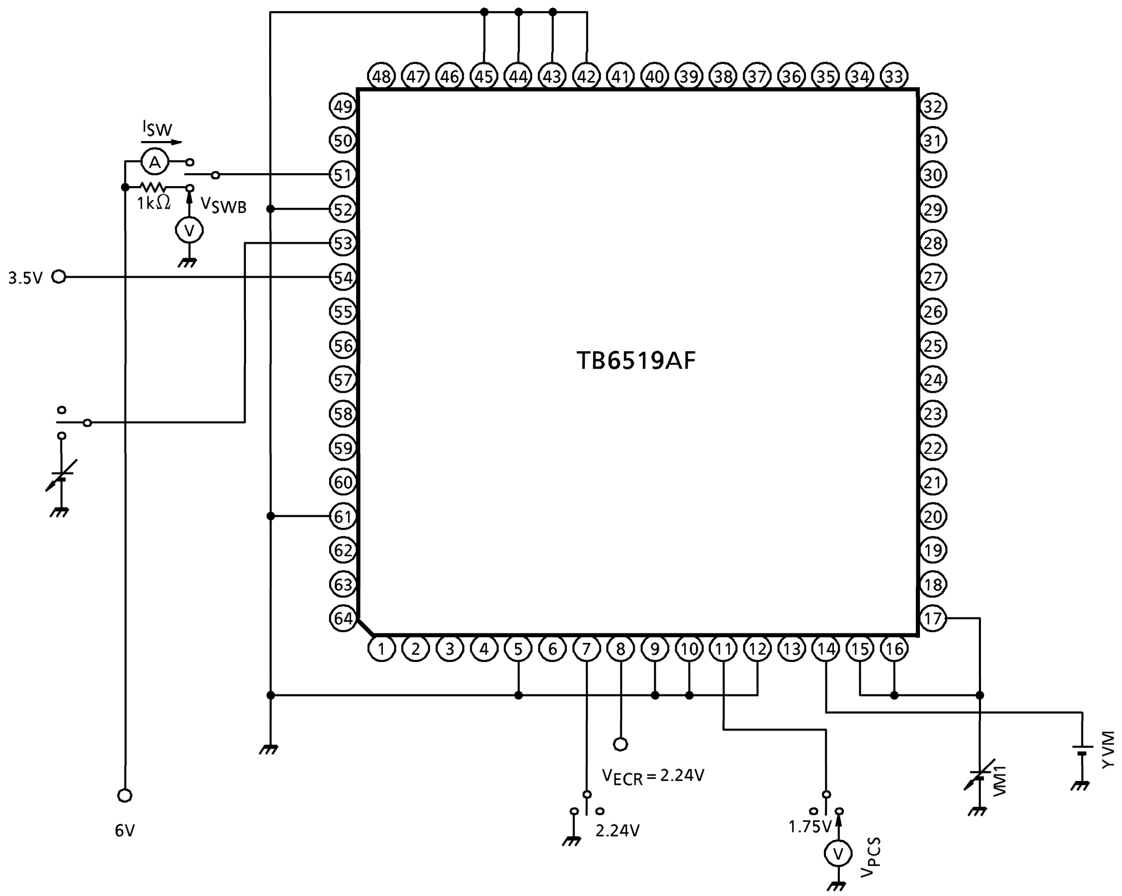


No. 10 I_U, No. 11 I_L

Change the YSTB terminal from H to L and then enter the following clock counts into the YCLK terminal in order to set the drive angle.

CLOCK	50		150		280	
Terminal	YU1	YL3	YU2	YL1	YU3	YL2
S_{W1}	0V	2V	0V	2V	0V	2V
S_{W2}	5V	6V	5V	6V	5V	6V

TEST CIRCUIT 5. $V_{PCS\,(1)}$, $V_{PCS\,(2)}$, YG_{PCS}, $I_{SW\,(1)}$, $I_{SW\,(2)}$, ΔV_{FC}, YVML, YVMS



No. 12 $V_{PCS\,(1)}$

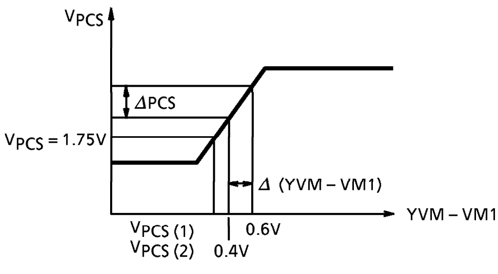
Set YVM = 6V and YEC = 2.24V and then measure the VM1 for which V_{PCS} = 1.75V.

No. 13 $V_{PCS\,(2)}$

Set YVM = 6V and YEC = 0V and then measure the VM1 for which V_{PCS} = 1.75V.

No. 14 YG_{PCS}

Set YVM = 6V and YEC = 2.24V and then acquire YG_{PCS} from the amount of V_{PCS} voltage change when (YVM − VM1) is changed from 0.4V to 0.6V.



$$YG_{PCS} = \frac{\Delta PCS}{\Delta\,(YVM - VM1)}$$

No. 15 I_{SW} (1)

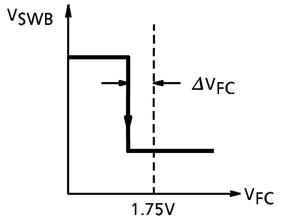
Set FC = 3V and YEC = 2.24V and then measure the current flowing into the YSW terminal. (YVM = VM1 = 6V)

No. 16 I_{SW} (2)

Set FC = 3V and YEC = 0V and then measure the current flowing into the YSW terminal. (YVM = VM1 = 6V)

No. 17 ΔV_{FC}

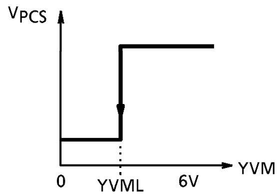
Set YPCS = 1.75V, change FC from 0V and then measure the difference in V_{FC} and V_{PCS} when V_{SWB} changes from H to L.



$$\Delta V_{FC} = V_{PCS} - V_{FC}$$

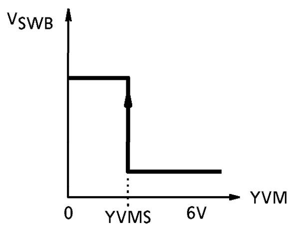
No. 30 YVML

Set FC = 3V, YEC = 2.24V and VM1 = YVM-1V, change YVM from 6V and then set YVML when V_{PCS} changes from H to L.

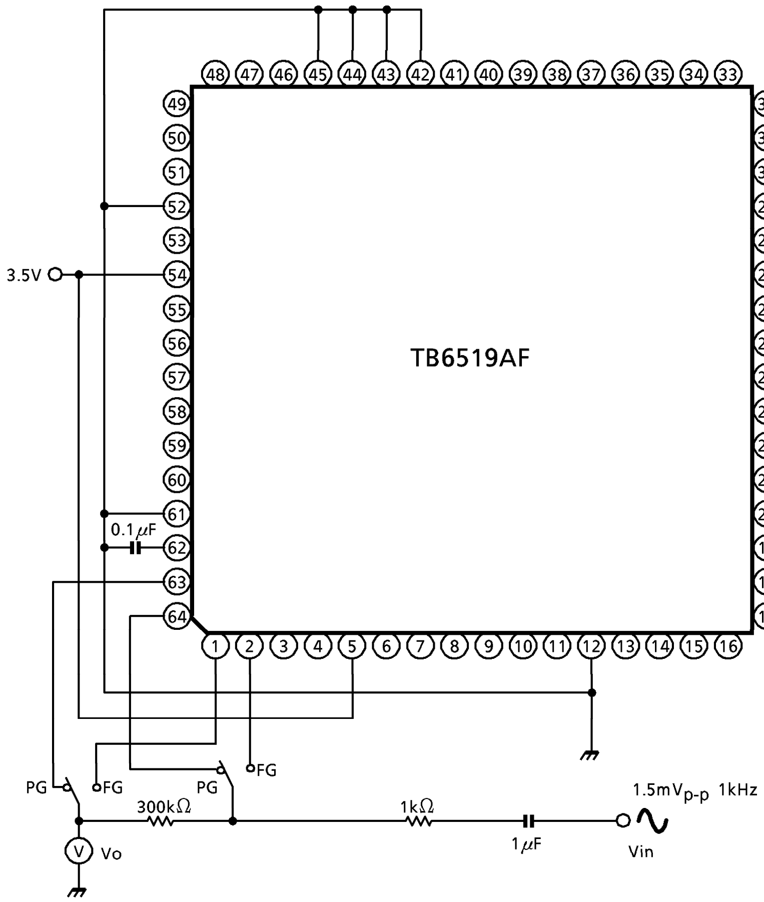


No. 31 YVMS

Set FC = 3V, YEC = 0V and VM1 = 6V, change YVM from 6V and then set YVMS when V_{SWB} changes from H to L.



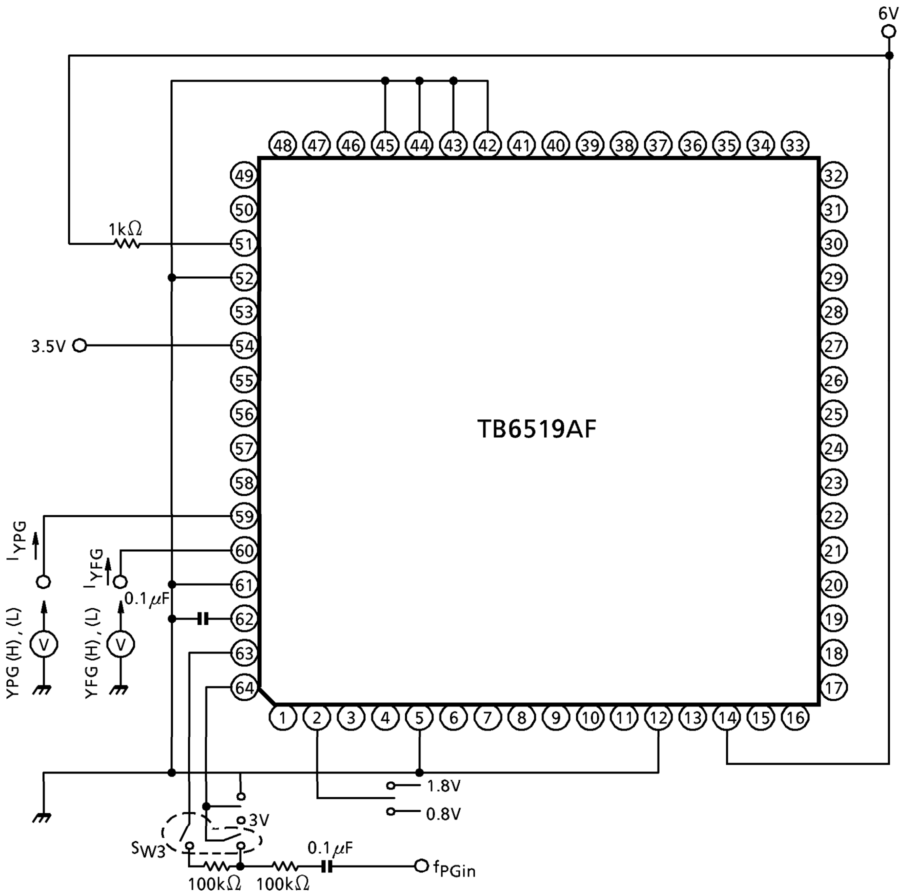
TEST CIRCUIT 6. G_{FG}, G_{PG}



No. 18 G_{FG}

Set the SW to FG, measure Vo when Vin = 1.5mV$_{p-p}$ at 1kHz and acquire $G_{FG} = 20\ell og\ (Vo / Vin)$.

TEST CIRCUIT 7. YFG (H), YFG (L), ΔPGin, YPG (H), YPG (L)



No. 19 YFG (H)

Measure the potential of YFG when a current of $I_{YFG} = -100\mu A$ is flowing after 1.8V has been applied to YFGin and YFG has been set at H.

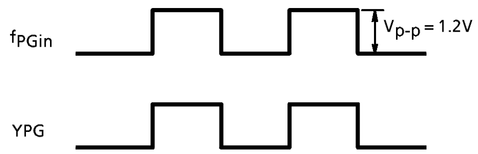
No. 20 YFG (L)

Measure the potential of YFG when a current of $I_{YFG} = 100\mu A$ is flowing after 0.8V has been applied to YFGin and YFG has been set at L.

No. 22 ΔPGin

Set SW3 on, input a 10kHz square wave from f_{PGin}, set the f_{PGin} V_{p-p} to 1.2V (ΔPGin = 0.6V) and confirm that the pin 59 is operating.

Also, set V_{p-p} to 0.9V (ΔPGin = 0.45V) and confirm that the YPG terminal is not operating.



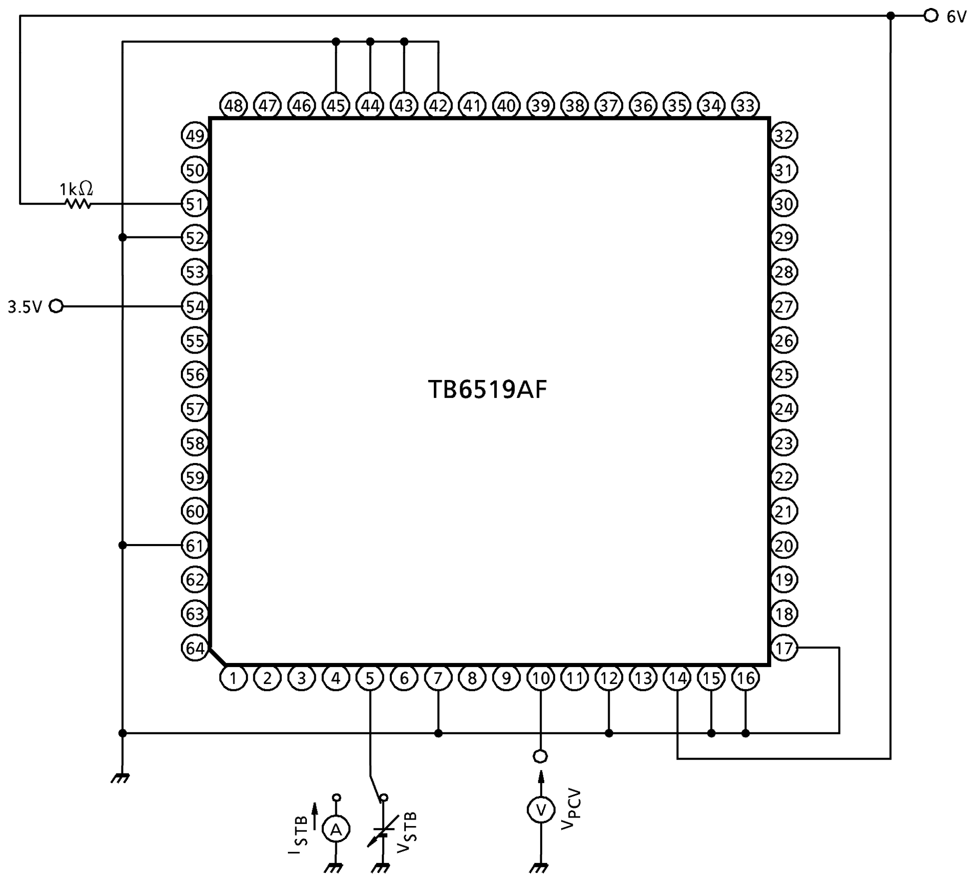
No. 23 YPG (H)

Measure the potential of YPG when a current of $I_{YPG} = -100\mu A$ is flowing after 3V has been applied to YPGin and YPG has been set at H.

No. 24 YPG (L)

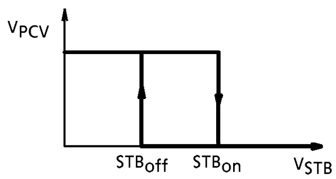
Measure the potential of YPG when a current of $I_{YPG} = 100\mu A$ is flowing after 0V has been applied to YPGin and YPG has been set at L.

TEST CIRCUIT 8. STB_{on}, STB_{off}, I_{STB}



No. 25 STB_{on}, No. 26 STB_{off}

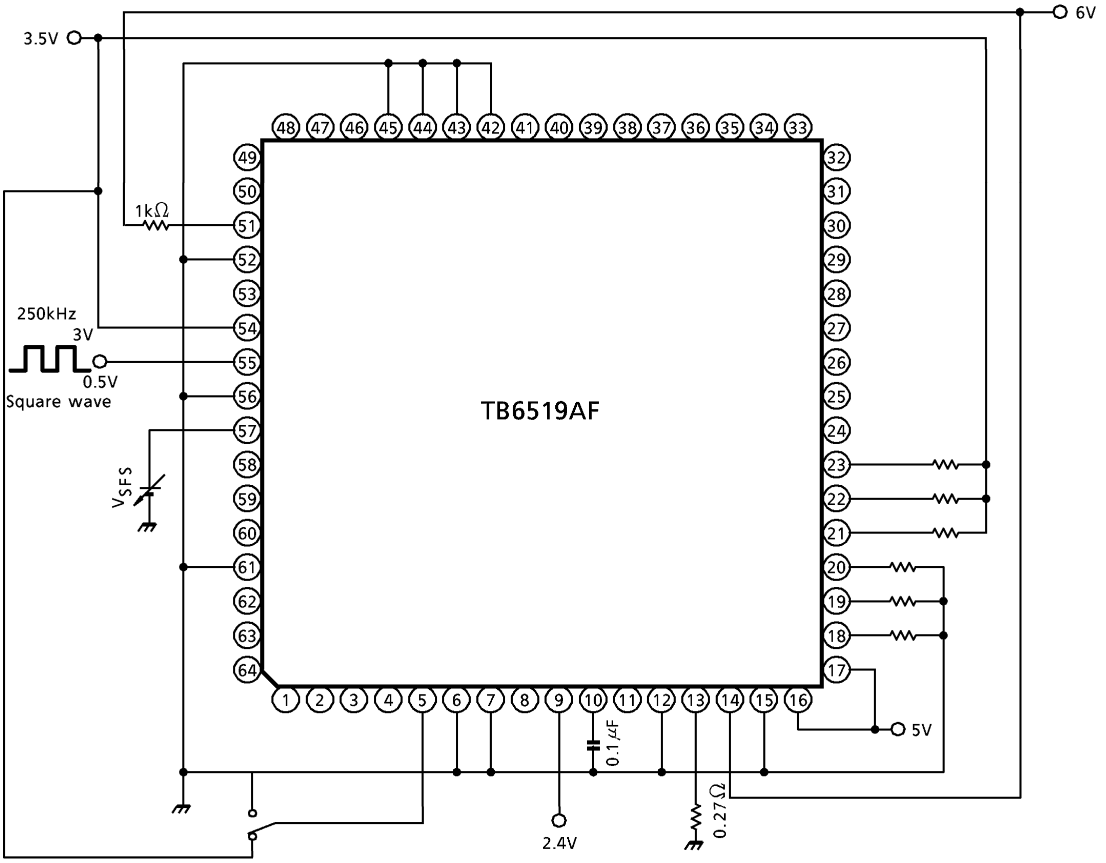
Change V_{STB} from 0V to 3.5V, and then from 3.5V to 0V, and measure V_{PCV}.
V_{STB} becomes STB_{on} when V_{PCV} changes from H to L, and becomes STB_{off} when V_{PCV} changes from L to H.



No. 27 I_{STB}

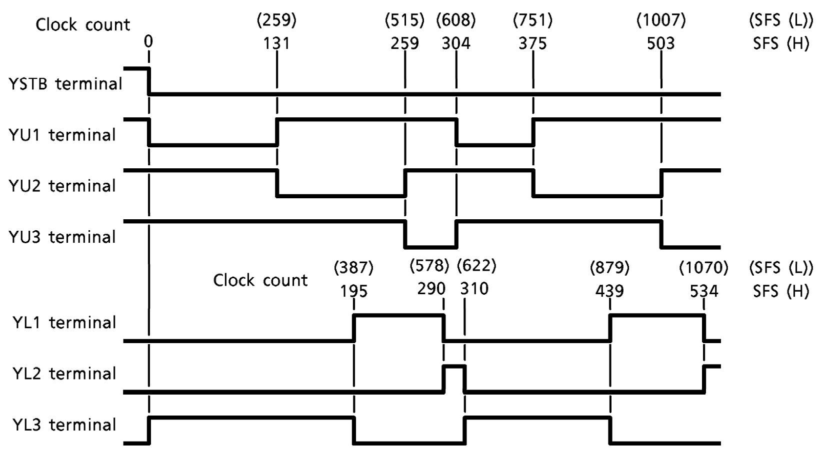
Measure I_{STB} when $V_{STB} = 0V$.

TEST CIRCUIT 9. SFS (L), SFS (H)

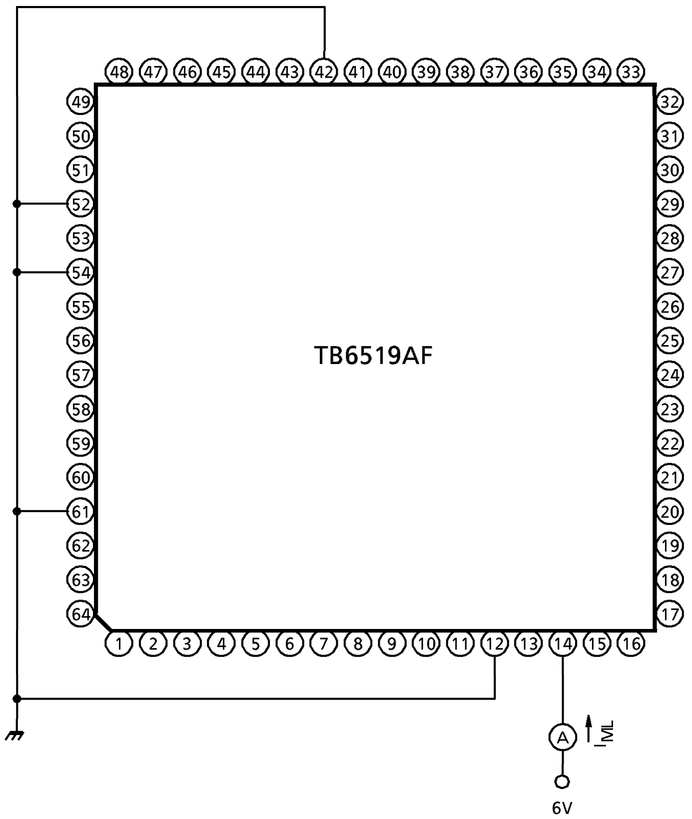


No. 28 SFS (L), No. 29 SFS (H)

Change V_{SFS} from 0V to 3.5V and measure the potential of YU1~3 and YL1~3.



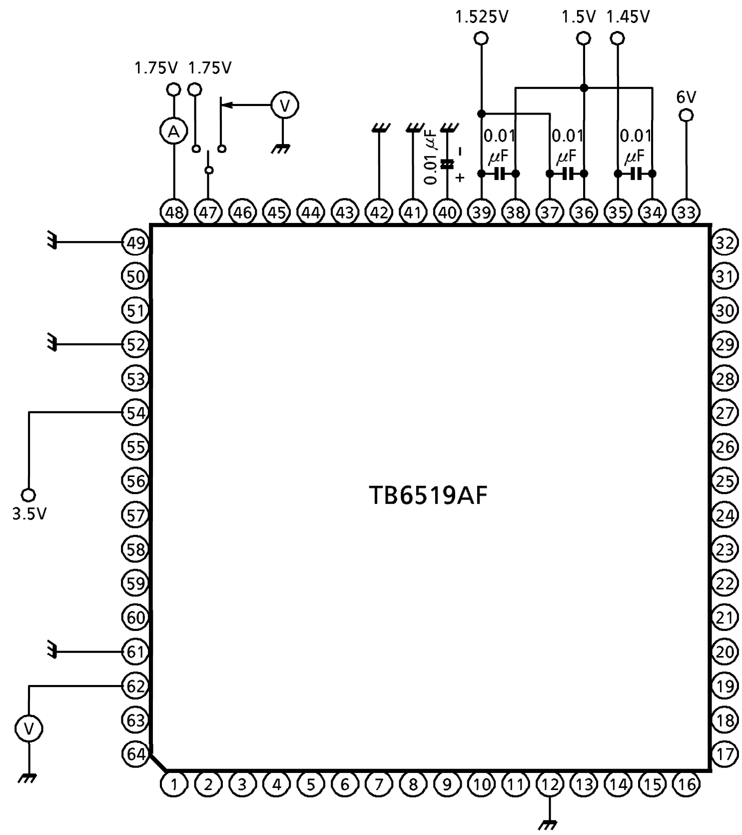
TEST CIRCUIT 10. I_{ML}



No. 32 I_{ML}

Measure the current that flows into pin ⑭ when YVM = 6V.

TEST CIRCUIT 11. CI_{EC}, CE_{CR}, CFG_{ref}



No. 34 CI_{EC}

Measure the current that flows into the CEC terminal with CEC = 1.75V and CECR = 1.75V.

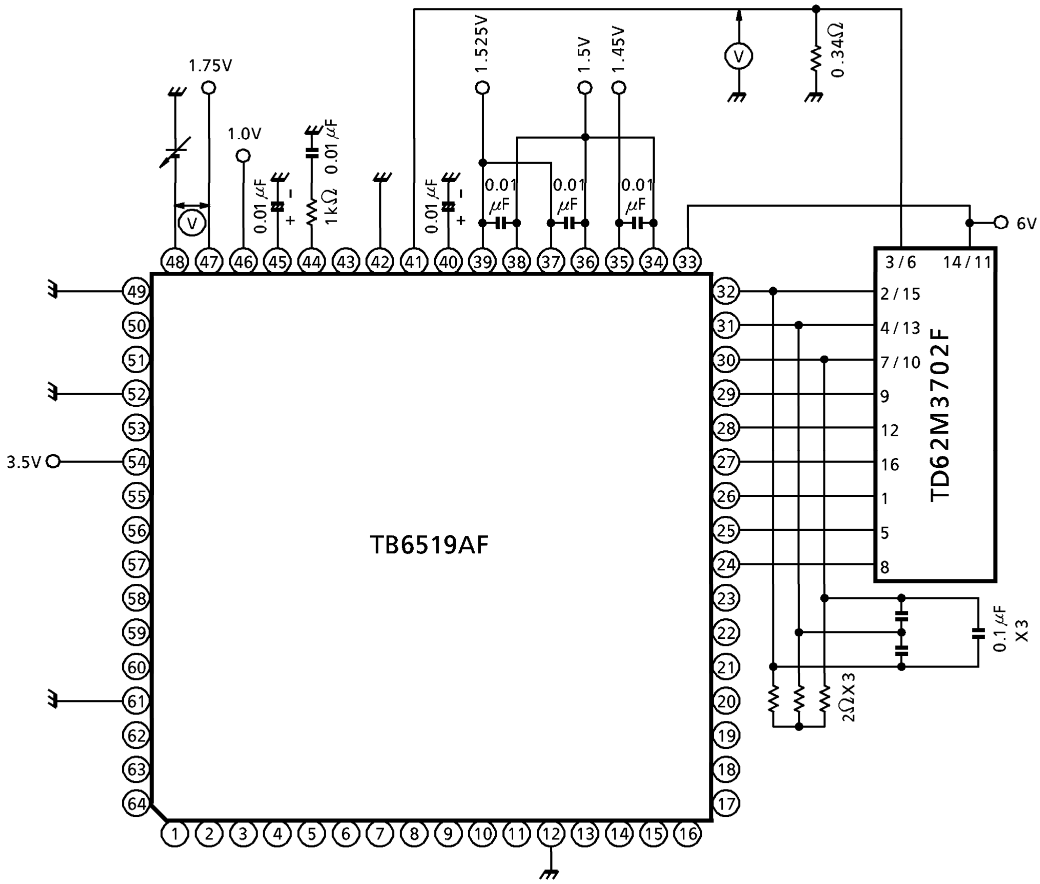
No. 35 CE_{CR}

Measure the voltage of the CECR terminal.

No. 58 CFG_{ref}

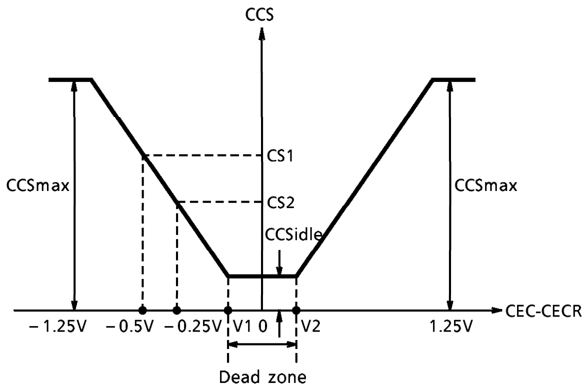
Measure the voltage of the REF terminal.

TEST CIRCUIT 12. CECm, CCSmaxm, CGiom, CCSidlem, CECofsm, CECdz



No. 36 No. 37 No. 38 No. 39 No. 40 No. 41

Set CTL = 1.0V and CECR = 1.75V, change CEC from 0V to 3.5V, measure the potential of the CCS terminal and confirm the V characteristics.



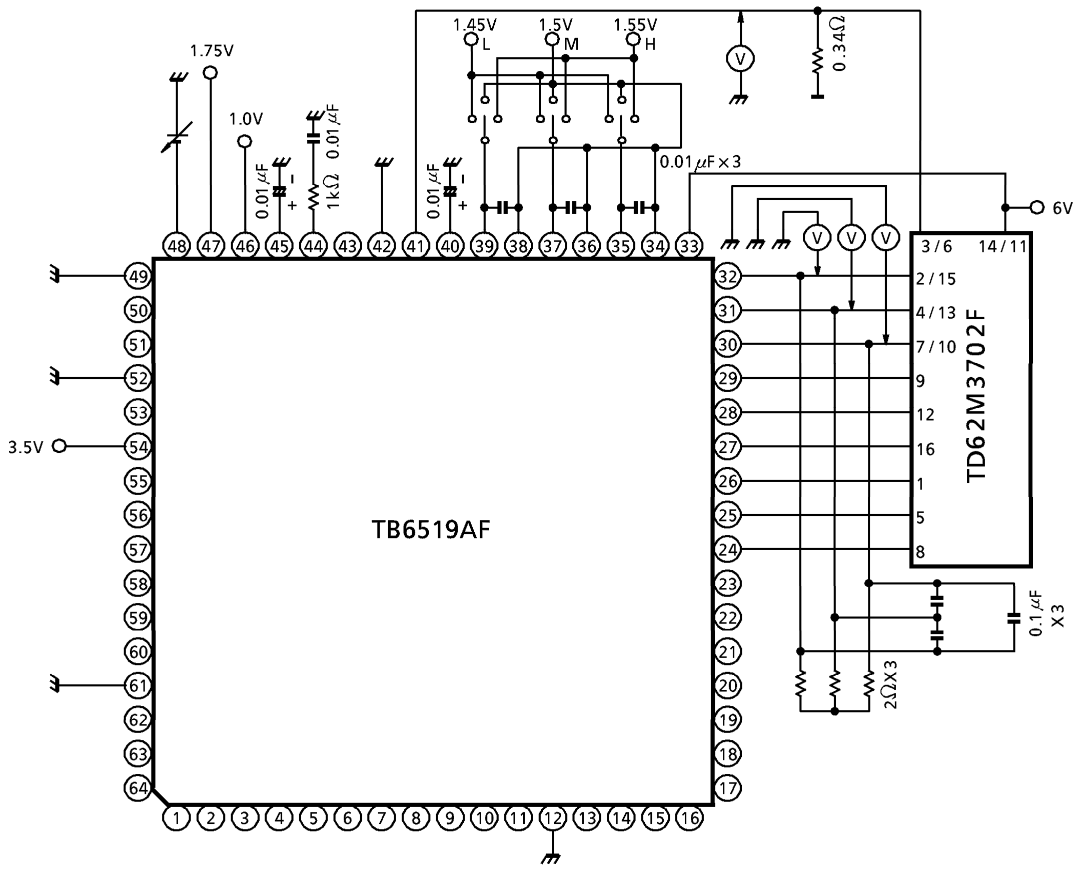
$$CGio = \frac{CS1 - CS2}{0.25V}$$

CCSidle : The CS potential within the dead zone

$$CECofs = \frac{V1 + V2}{2}$$

$$CECdz = V2 - V1$$

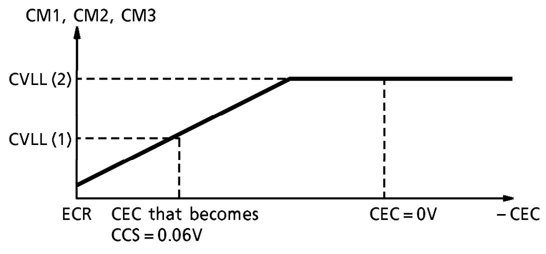
TEST CIRCUIT 13. CVLL (1), CVLL (2)



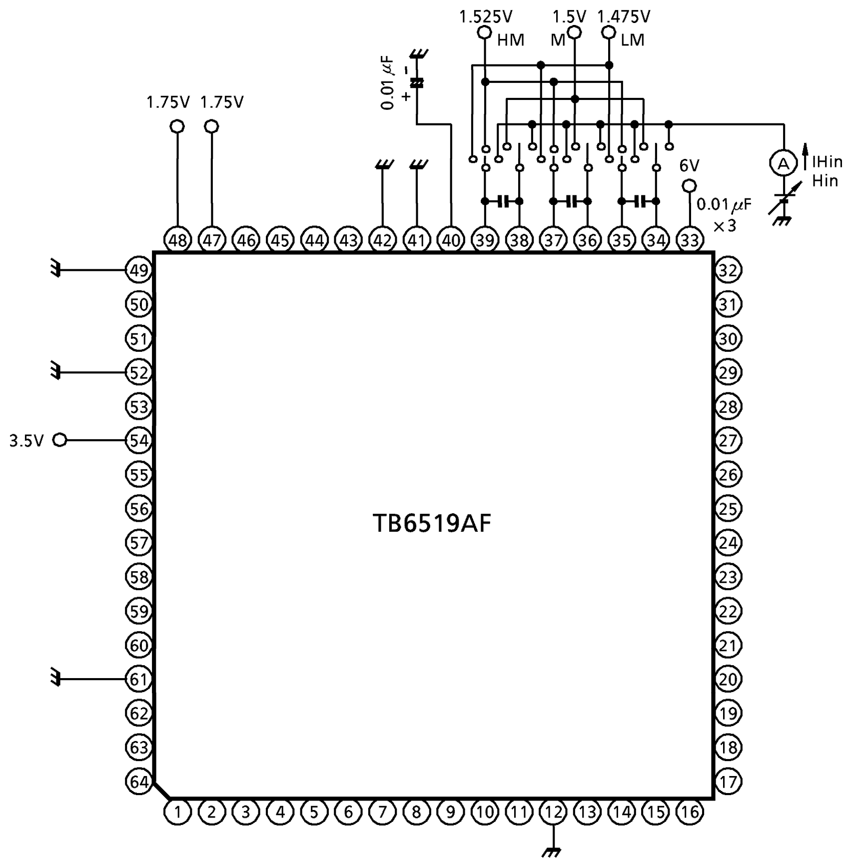
No. 42 CVLL (1), No. 43 CVLL (2)

Perform the settings laid out in the table below and measure the potential of the CM1, CM2 and CM3 terminals when the CEC voltage is adjusted to CCS = 0.06V and when CEC = 0V.

	H1 +	H2 +	H3 +	TEST TERMINAL
Setting 1	H	L	M	CM1
Setting 2	M	H	L	CM2
Setting 3	L	M	H	CM3



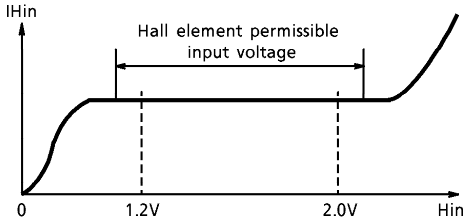
TEST CIRCUIT 14. Hin



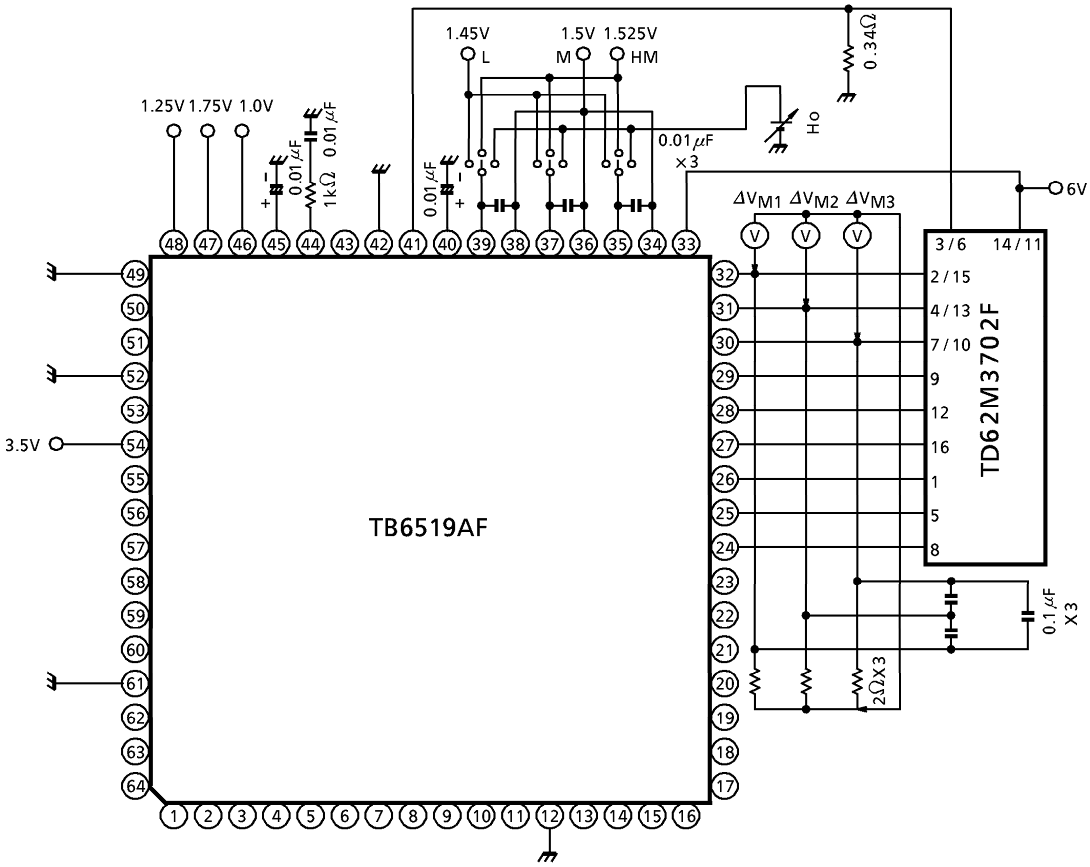
No. 44 Hin

Perform the settings laid out in the table below and then measure the voltage range of the IHin that does change rapidly in accordance with changes in the Hin.

	H1 +	H1 −	H2 +	H2 −	H3 +	H3 −
Setting 1	Hin	Hin	HM	M	LM	M
Setting 2	LM	M	Hin	Hin	HM	M
Setting 3	HM	M	LM	M	Hin	Hin



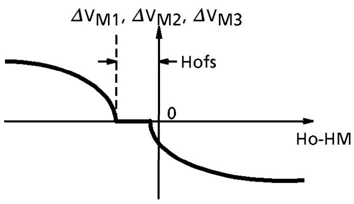
TEST CIRCUIT 15. Hofs



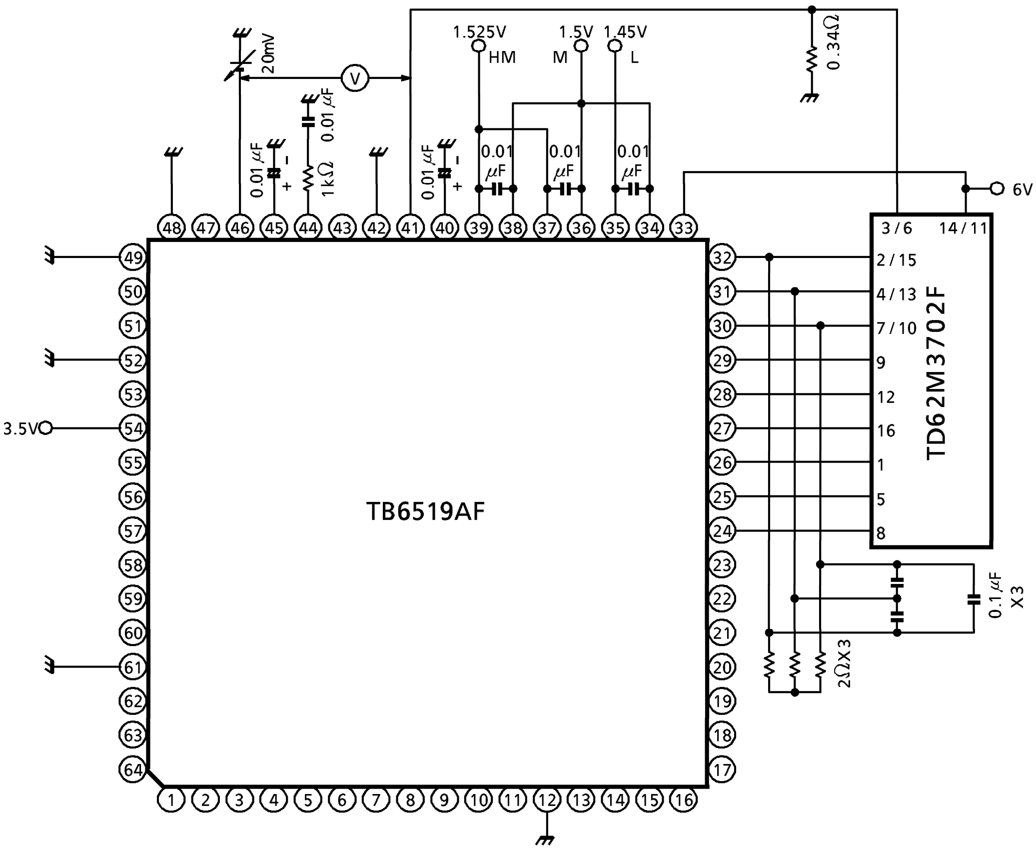
No. 45 Hofs

Perform the settings laid out in the table below and then measure the hall element input conversion offset.

	H1 +	H2 +	H3 +	OFFSET MEASUREMENT
Setting 1	Ho	HM	L	$\Delta V_{M1} = 0$ difference between H1 + and H2 +
Setting 2	L	Ho	HM	$\Delta V_{M2} = 0$ difference between H2 + and H3 +
Setting 3	HM	L	Ho	$\Delta V_{M3} = 0$ difference between H3 + and H1 +

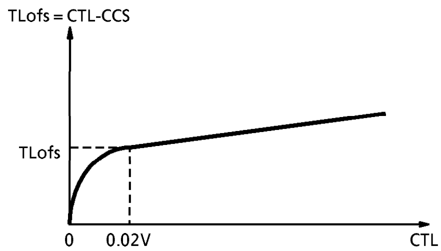


TEST CIRCUIT 16. TLofs

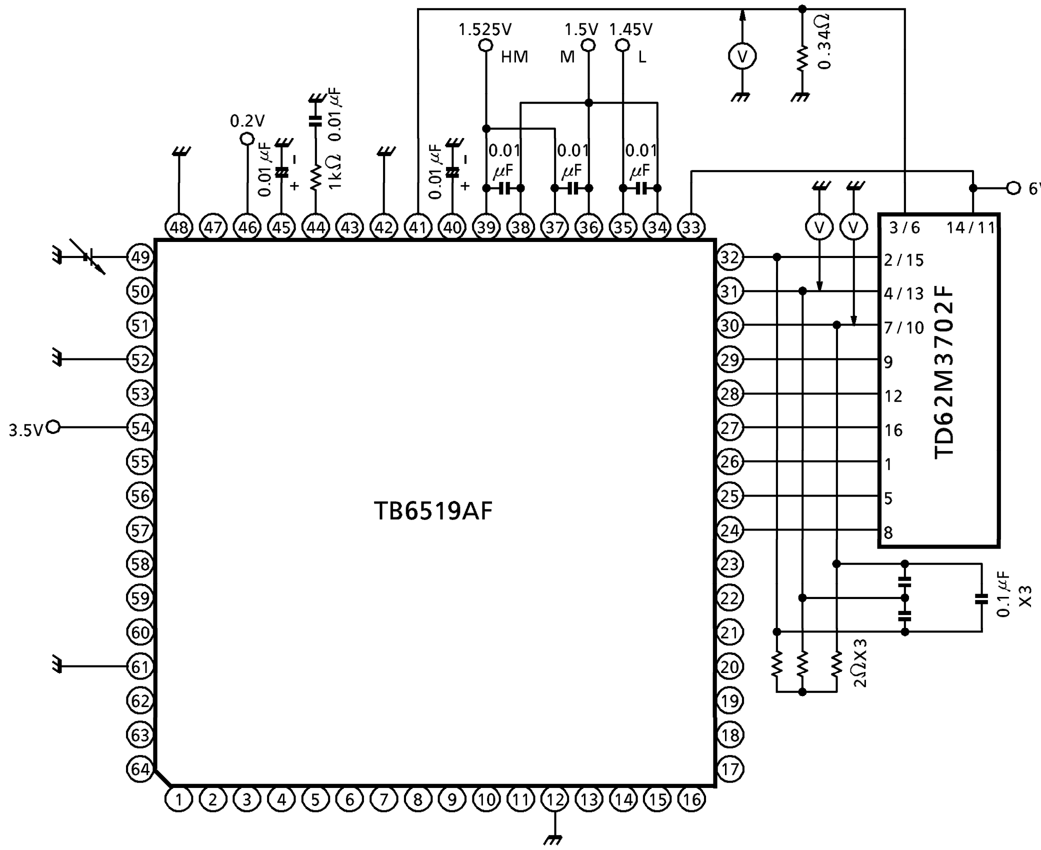


No. 46 TLofs

Measure the potential differential (CTL-CCS) of the CTL and CCS terminals when CTL = 0.02V.

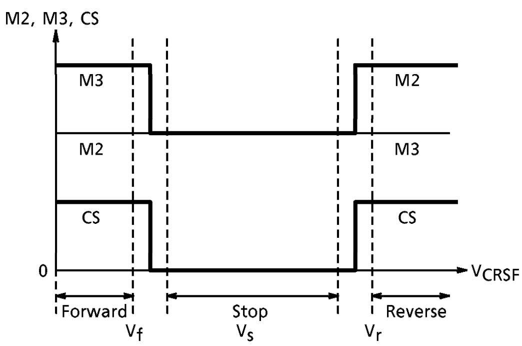


TEST CIRCUIT 17. Vf, Vs, Vr

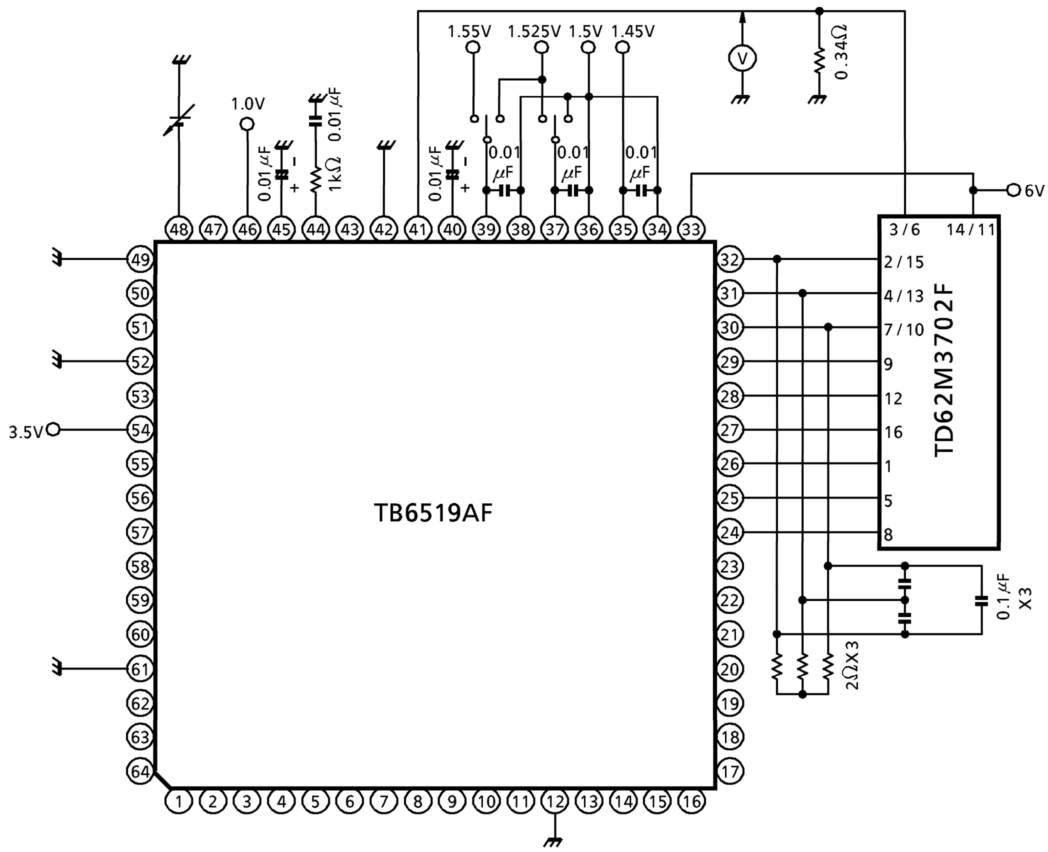


No. 47 Vf, No. 48 Vs, No. 49 Vr

Change CRSF from 0V to 3.5V, acquire the characteristics indicated in the following diagram and measure the threshold voltage.



TEST CIRCUIT 18. R

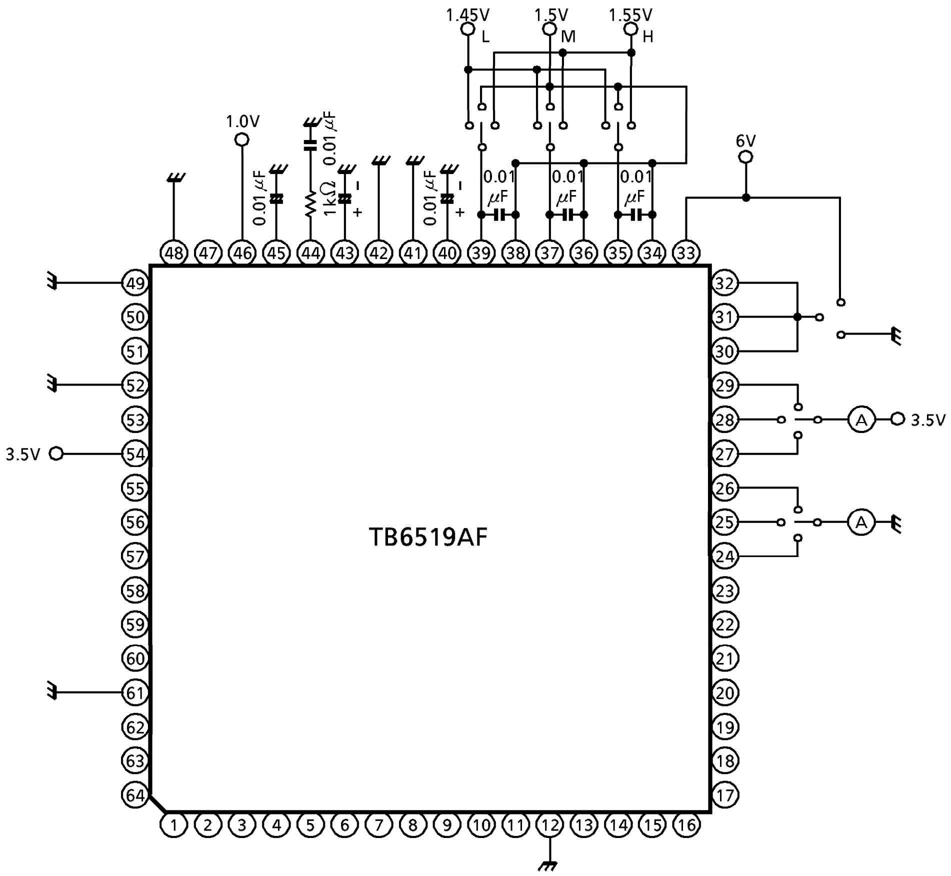


No. 50 R

Adjust the CEC voltage so that CCS becomes 0.06V with H1+ = 1.525V and H2+ = 1.525V, and then measure CCS (CS_L) when H1+ = 1.525V and H2+ = 1.525V and CCS (CS_H) when H1+ = 1.55V and H2+ = 1.5V.

Then acquire : $R = \frac{CS_H - CS_L}{CS_L}$

TEST CIRCUIT 19. CI_U, CI_L

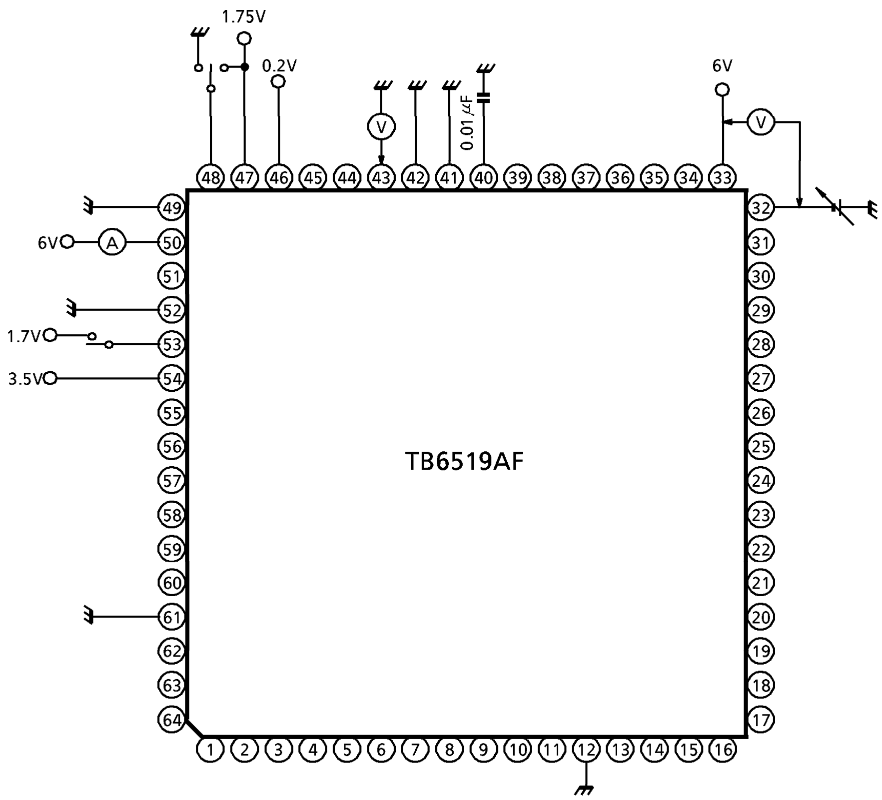


No. 51 CI_U, No. 52 CI_L

Perform the settings laid out in the table below and then measure the current that flows into the CU1, CU2 and CU3 terminals, and the CL1, CL2 and CL3 terminals.

	H1 +	H2 +	H3 +	M1, M2, M3	TEST TERMINAL
Setting 1	L	H	M	GND	CU1
Setting 2	M	L	H	GND	CU2
Setting 3	H	M	L	GND	CU3
Setting 4	H	L	M	V_M	CL1
Setting 5	M	H	L	V_M	CL2
Setting 6	L	M	H	V_M	CL3

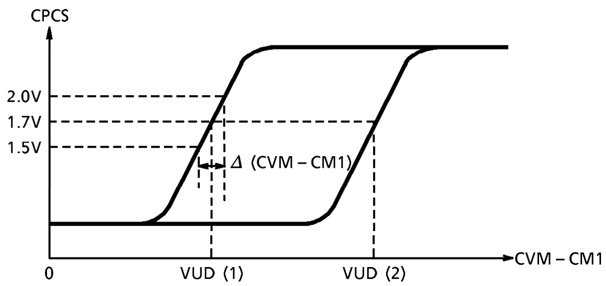
TEST CIRCUIT 20. CG_{PCS}, VUD (1), VUD (2), CI_{SWB}



No. 54 CG_{PCS}, No. 55 VUD (1), No. 56 VUD (2)

Set CEC = 0V, change CM1 from 6V to 5V and measure the potential difference (CVM − CM1) of the CVM terminal and the CM1 terminal when the potential of the CPCS terminal becomes 1.7V.

Set CEC = CECR = 1.75V, perform the same measurements as outlined below and acquire the characteristics indicated in the diagram below.

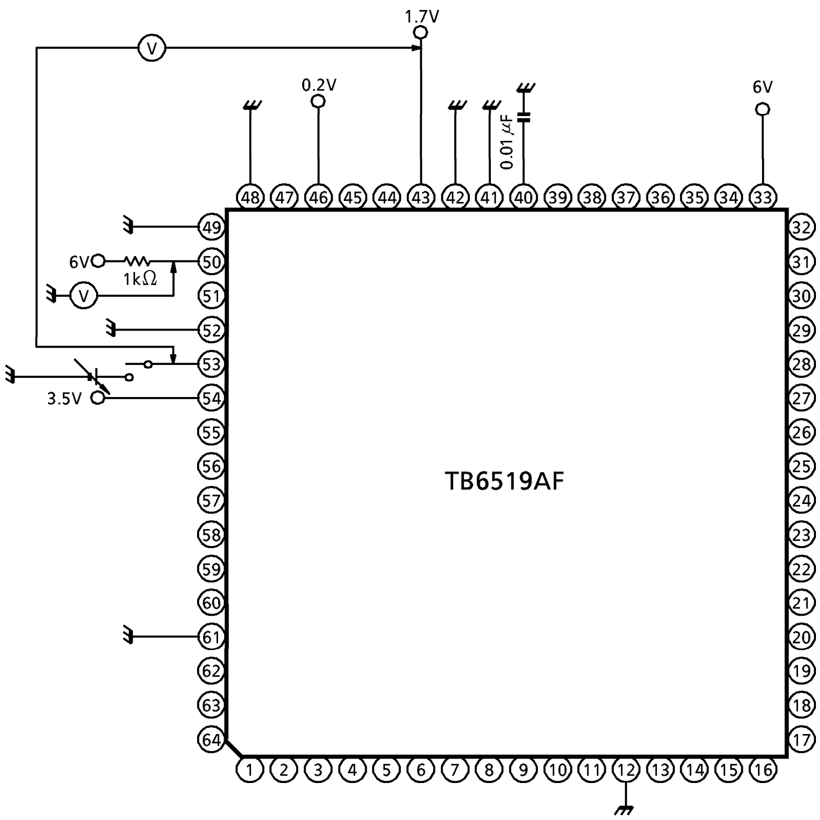


$$CG_{PCS} = \frac{2.0V - 1.5V}{\Delta\ (CVM - CM1)}$$

No. 57 CI_{SWB}

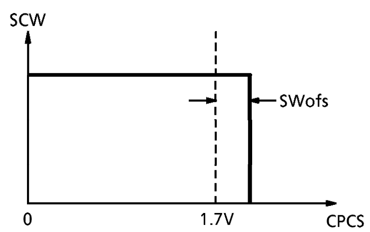
Set FC = 1.7V, CEC = 0V and CM1 = 6V and measure the current that flows into the SCW terminal.

TEST CIRCUIT 21. CSWofs

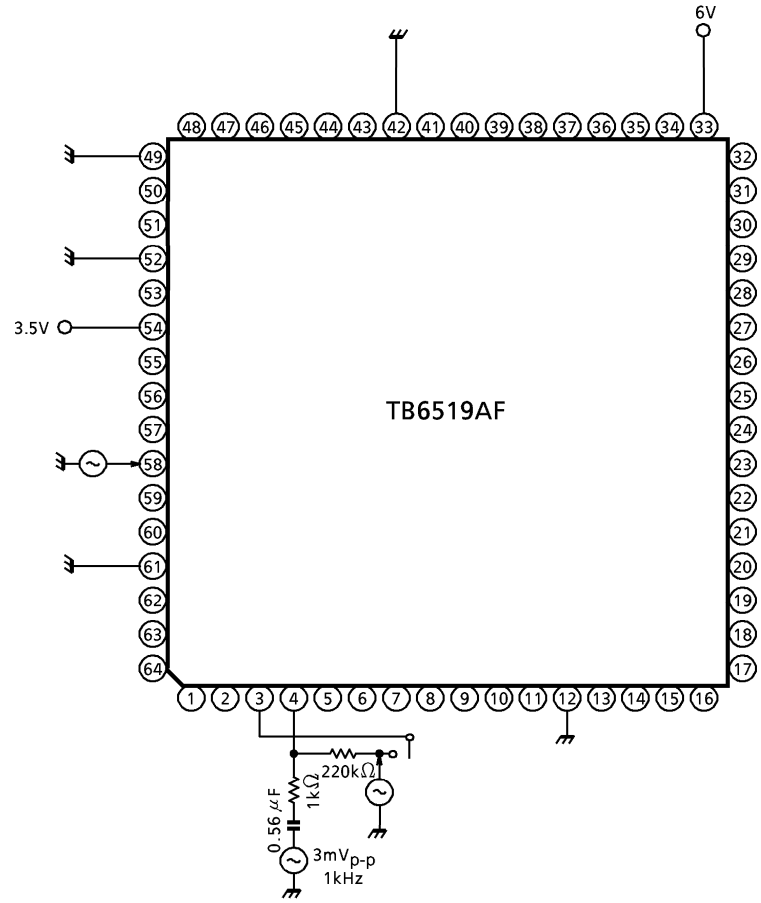


No. 53 CSWofs

Set SPCS = 1.7V, change FC from 0V to 3.5V and measure the potential difference (FC – CPCS) of the FC terminal and the CPCS terminal when SCW changes from high to low.



TEST CIRCUIT 22. CG_{FG}, CFG_H, CFG_L

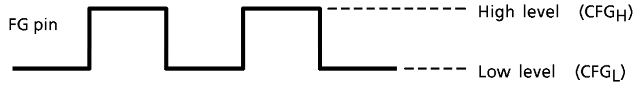


No. 59 CG_{FG} No. 60 CFG_H No. 61 CFG_L

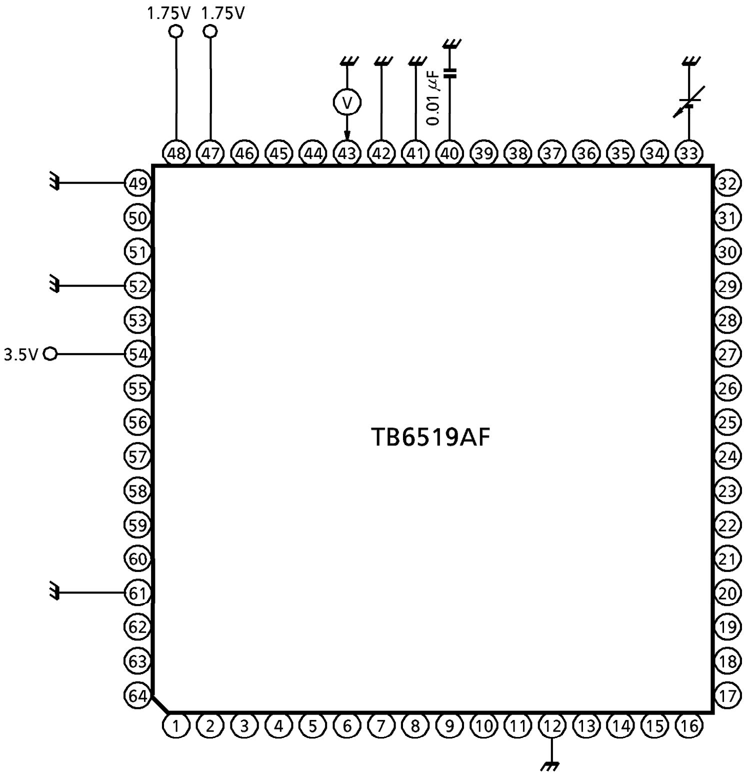
Set CFGout = Vo and measure Vo when Vin = 3mV$_{p\text{-}p}$ at 1kHz.

Then acquire : $CG_{FG} = 20\ell og \frac{Vo}{Vin}$

Also, acquire the characteristics indicated in the diagram below and then measure the high level potential and low level potential of the CFG terminal's output wave form.

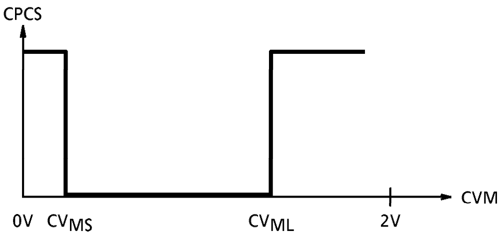


TEST CIRCUIT 23. CV_{ML}, CV_{MS}



No. 62 CV_{ML} No. 63 CV_{MS}

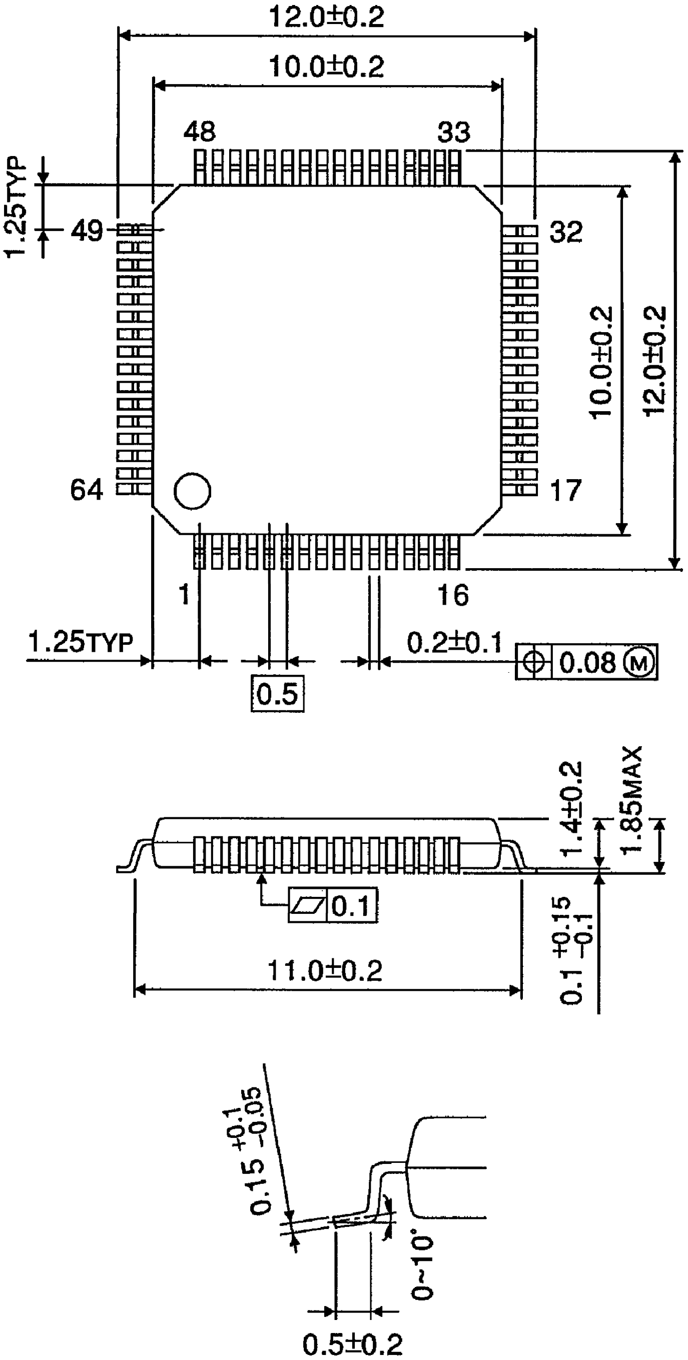
Change CVM from 2V to 0V, acquire the characteristics indicated in the following diagram and measure the threshold voltage.



OUTLINE DIAGRAM

LQFP64-P-1010-0.50A

Unit: mm



Weight: 0.34g (Typ.)