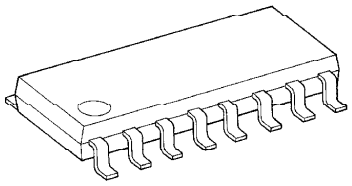
TENTATIVE TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB1232F, TB1232FN

1.3GHZ 3-WIRE BUS CONTROL FREQUENCY SYNTHESIZER FOR TV / CABLE TV

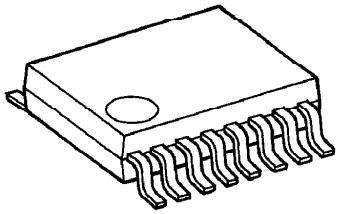
The TB1232F and TB1232FN are single-chip frequency synthesizer ICs that can be combined with a μCPU to configure an advanced-function frequency synthesizer system.
TB1232F or TB1232FN is a Bi-CMOS frequency synthesizer in which CMOS is used for the PLL and BIPOLAR for the prescaler.

TB1232F



SOP16-P-225-1.27

TB1232FN



SSOP16-P-225-0.65B

Weight
SOP16-P-225-1.27 : 0.16g (Typ.)
SSOP16-P-225-0.65B : 0.07g (Typ.)

FEATURES

- Low phase noise achieved by FET amp
- Built-in tuning amp (high voltage : 33V)
- Built-in four-band drive transistor (voltage range : 8.1 to 13.2V)
- Two bands can be operated simultaneously (total load : 50mA max.)
- 1 / 8 prescaler from 80 to 1300MHz
- Built-in phase lock detector
- Built-in 18- / 19-bit automatic identifier circuit
- Frequency steps : 31.25 and 62.5kHz
- Built-in power-on reset circuit
- Pin layout similar to that of TB1220 and 1233, which use I^2C bus
- Compact flat package : TB1232F : 16-pin SOP (1.27-mm pitch)
  TB1232FN : 16-pin SSOP (0.65-mm pitch)

(Note) These devices are easy to be damaged by high static voltage or electric fields. In regards to this, please handle with care.

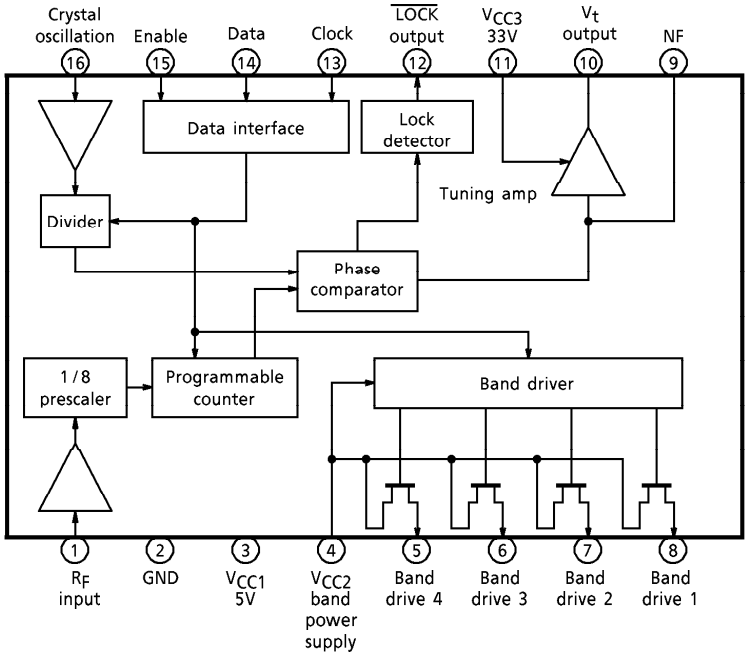
FUNCTION LIST

PRODUCT NAME	BUS METHOD	BAND VOLTAGE RANGE
TB1234F / FN	3-WIRE	4.5~9.9V
TB1220F / FN	I^2C	4.5~9.9V
TB1232F / FN	3-WIRE	8.1~13.2V
TB1233F / FN	I^2C	8.1~13.2V

- Status at power-on reset operation

  Band drives 1 to 4 : OFF
  Tuning amp : ON
  Reference frequency divider ratio : 1 / 1024
  Counter data : All 『0』

BLOCK DIAGRAM



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage 1	V_{CC1}	6.0	V
Supply Voltage 2	V_{CC2}	14	V
Supply Voltage 3	V_{CC3}	36	V
Power Dissipation	P_D	(Note 1)	mW
Operating Temperature Range	T_{opr}	−20~85	°C
Storage Temperature Range	T_{stg}	−55~150	°C

(Note 1) TB1232F : 540mW TB1232FN : 560mW
(Note 2) When using the device at above Ta = 25°C, decrease the power dissipation F-type by 4.3mW and FN-type by 4.5mW for each increase of 1°C.
(Note 3) These devices are easy to be damaged by high static voltage or electric fields. In regards to this, please handle with care.

RECOMMENDED SUPPLY VOLTAGE

PIN No.	PIN NAME	MIN.	TYP.	MAX.	UNIT
3	V_{CC1} : PLL power supply.	4.5	5.0	5.5	V
4	V_{CC2} : Band power supply.	8.1	12.0	13.2	V
11	V_{CC3} : Tuning amp power supply.	27	33	35	V

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, V_{CC1} = 5V, V_{CC2} = 9V, V_{CC3} = 33V, Ta = 25°C)
AC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current 1	I_{CC1}	1	Band switch : OFF, V_t : OFF	—	30	—	mA
Supply Current 2	I_{CC2}	1	Band switch : OFF	—	1.5	—	mA
Supply Current 3	I_{CC3}	1	V_t : OFF	—	0.5	—	mA
Band Driver Drive Current	I_{BD}	3	—	—	40	50	mA
Band Driver Drive Voltage Drop	V_{BD} Sat	3	I_{BD} = 40mA	—	0.25	0.40	V
Tuning Amp Output Low-Level Voltage	V_t MIN	1	V_{CC3} = 33 [V]	—	0.25	0.33	V
Tuning Amp Output Voltage (Close Loop)	V_t OUT	1	V_{CC3} = 33 [V]	0.33	—	32.8	V
Charge Pump Output Current	I_{cp}	—	—	—	180	—	μA
Prescaler Input Sensitivity	V_{in1}	2	f = 80~150MHz	−20	—	+3	dBmW
	V_{in2}	2	f = 150~1000MHz	−30	—	+3	
	V_{in3}	2	f = 1.0~1.3GHz	−20	—	+3	
Lock Output Low Voltage	V_{LkL}	—		—	—	0.4	V
Lock Output High Voltage	V_{LkH}	—		4.6	—	—	V
Logic Input Low Voltage	V_{BsL}	—	Pins 13 to 15	—	—	0.8	V
Logic Input High Voltage	V_{BsH}	—	Pins 13 to 15	3.0	—	—	V
Logic Input Current (when Low)	I_{BsL0}	1	Pins 13 to 15 V_{CC1} = 0 [V]	—	—	1	μA
Logic input current (when Low)	I_{BsL5}	1	Pins 13 to 15 V_{CC1} = 5 [V]	—	—	1	
Logic Input Current (when High)	I_{BsH0}	1	Pins 13 to 15 V_{CC1} = 0 [V]	—	—	1	
Logic Input Current (when High)	I_{BsH5}	1	Pins 13 to 15 V_{CC1} = 5 [V]	—	—	1	
Setup Time	T_S	—	See data timing chart.	2	—	—	μs
Enable Hold Time	T_{sL}			2	—	—	
Next Enable Disable Time	T_{NE}			6	—	—	
Next Clock Disable Time	T_{NC}			6	—	—	
Clock Width	T_C			2	—	—	
Enable Setup Time	T_L			10	—	—	
Data Hold Time	T_H			2	—	—	

HOW TO CALCULATE LOCK FREQUENCY

Calculate the lock frequency using the following formula :

$$f_{OSC} = fr \times 8 \times (32M + S)$$

Here,

f_{OSC} : Oscillation frequency of VCO (prescaler input frequency)

fr : Reference frequency. $1/2^9$ ($1/2^{10}$) of oscillation frequency of the crystal oscillator. Data length is automatically set by the identifier circuit. When transferring 18bits, $1/2^9$; transferring 19bits, $1/2^{10}$.

M : Main counter preset value. Corresponds to ten (nine) bits starting from the MSB to MSB-9 (MSB-8) of the data.
Input data in binary in the range $32 \leqq M \leqq 1023$ (511).

S : Swallow counter preset value. Corresponds to five bits from MSB-10 (MSB-9) to LSB.
Input data in binary in the range $0 \leqq S \leqq 31$.

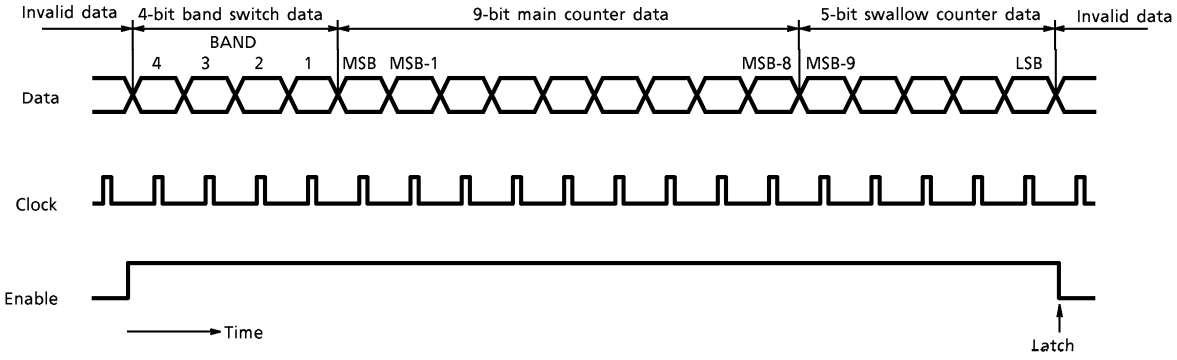


Fig.1 Normal data format (when transferring 18bits)

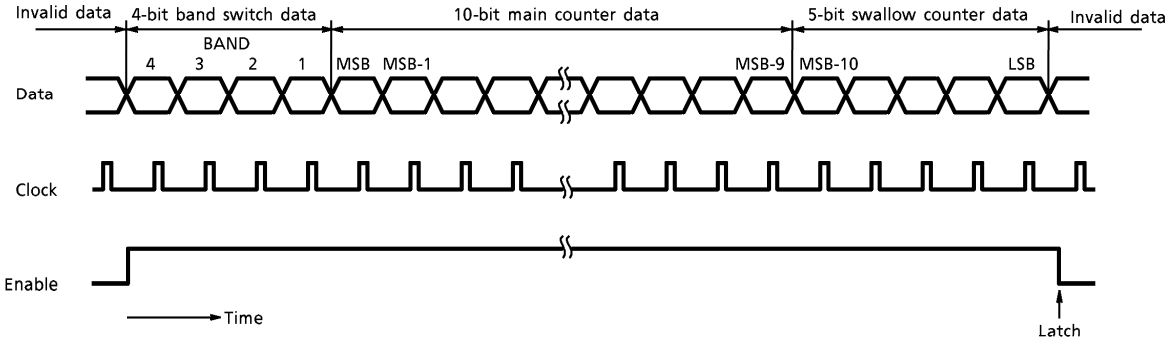


Fig.2 Normal data format (when transferring 19bits)

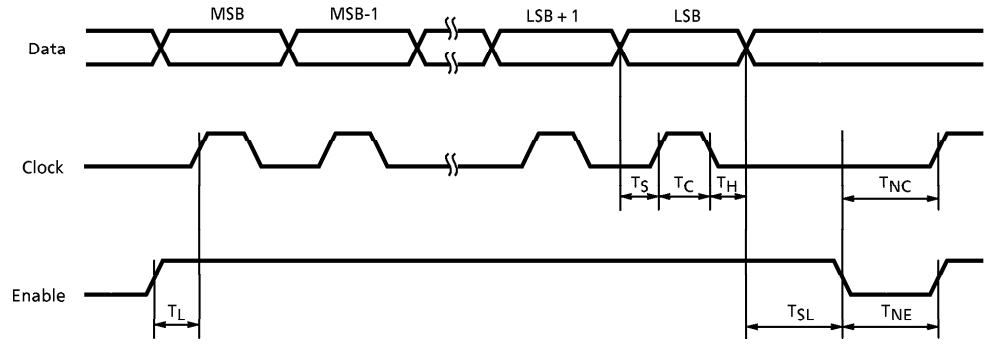


Fig.3 Data timing chart (fall timing)

- When transferring 18-bit data :

  Data read timing : When the enable signal is high, data are loaded into an internal register on the fall of the clock signal.

  Data latch condition : The number of clocks while the enable signal is high must be 18, one for each bit. (The number of clock rises during enable is 18.)
  Data are latched on the fall of the enable signal and transferred.

- When transferring 19-bit data :

  Data read timing : When the enable signal is high, data are loaded into an internal register on the fall of the clock signal.

  Data latch condition : The number of clocks while enable signal is high must be 19, one for each bit. (The number of clock rises during enable is 19.)
  Data are latched on the fall of the enable signal and transferred.

TEST MODE

Entering test mode enables the user to change settings and to check functions.
To change from normal mode to test mode, set the number of clocks during enable to 34 and transfer 34-bit clock data for three times. Since only the last data transferred are valid, any data can be transferred the first two times.
Once test mode is entered, all data transferred are valid.

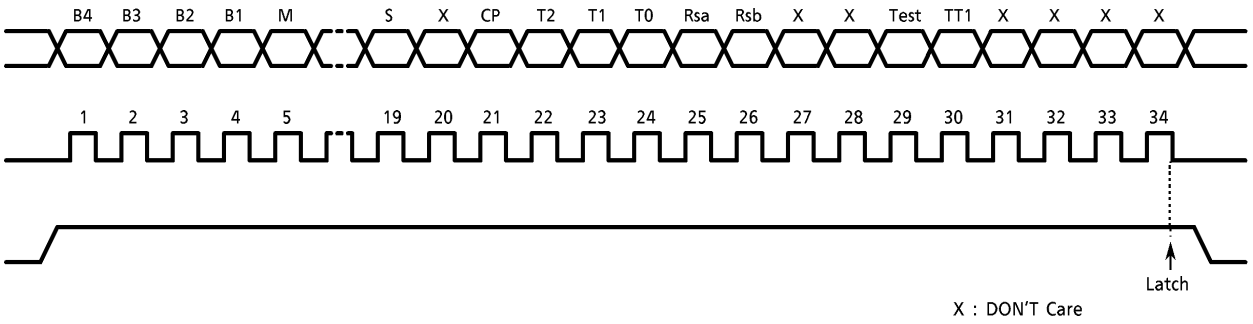


Fig.4 Test data format

DETAILS OF TEST DATA

- B4 to 1 : Band drive data
- M, S : Main, swallow counter data
- T2, T1, T0 : Test bit settings
- CP : Charge pump output resistance setting
  『0』: 2kΩ
  『1』: 10kΩ
- Rsa, Rsb : Phase comparator reference frequency divider ratio settings
- Test : 1/8 prescaler ON/OFF setting
- TT1 : Phase comparator test setting
- X : Don't care

TT1, T2, T1, T0 : Test bit settings

TT1	T2	T1	T0	TEST ITEM	OUTPUT PIN
1	0	0	1	Normal operation	
1	0	1	X	OFF	Pin 9 : NF
	1	1	0	Charge pump Sink	
	1	1	1	Source	
1	1	0	0	Reference frequency output	Pin 13 : Clock
				Counter divider output	Pin 14 : Data
X	1	0	1	Prescaler output	Pin 12 : Lock
0	0	0	0	Phase comparator output	Pin 9 : NF

X : DON'T Care

(*) To test the counter divider output, input the main and swallow counter data.

RSa, RSb : Phase comparator reference fequenc settings

RSa	RSb	DIVIDER RATIO SETTING VALUE
1	1	1/512
0	1	1/1024
X	0	1/640

X : DON'T Care

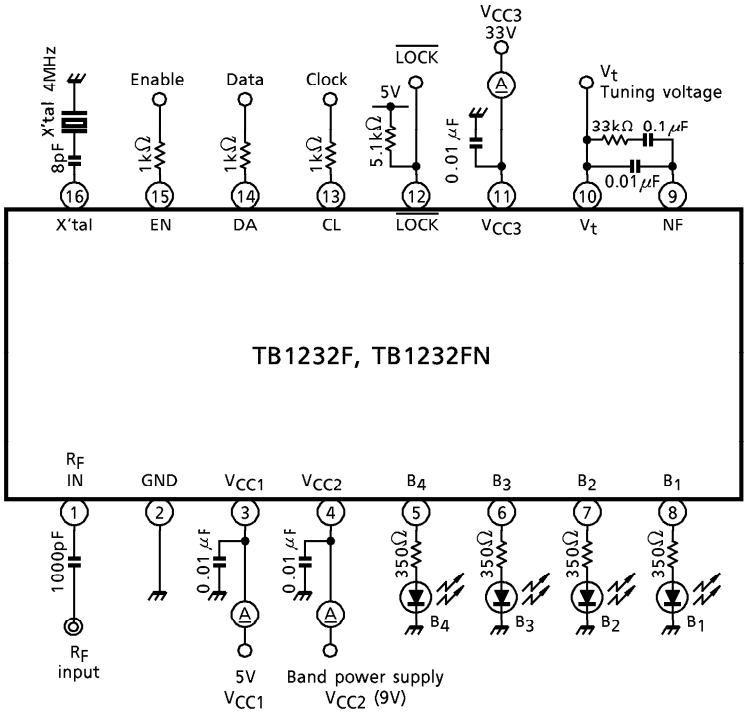
Test : 1/8 prescaler ON/OFF

『0』 : 1/8 prescaler ON

『1』 : 1/8 prescaler OFF

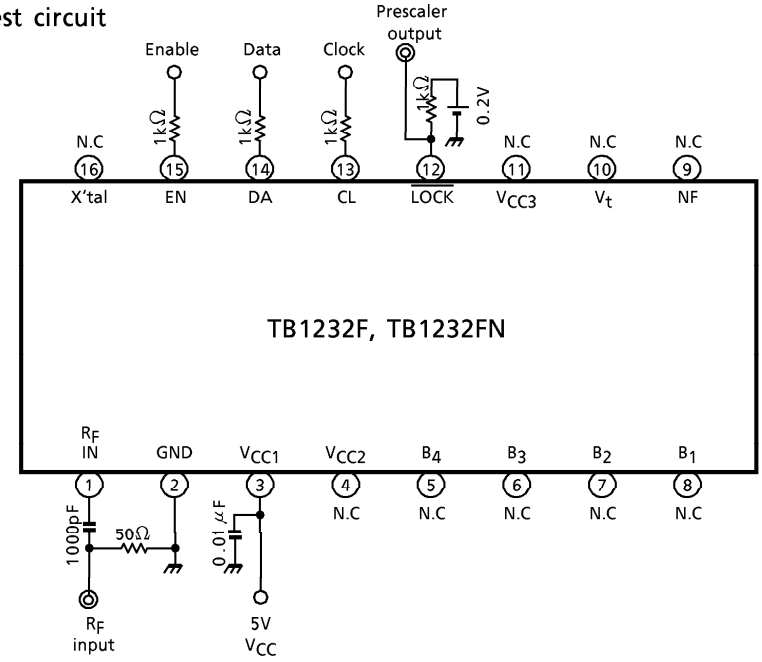
TEST CIRCUIT 1

Evaluation board circuit



TEST CIRCUIT 2

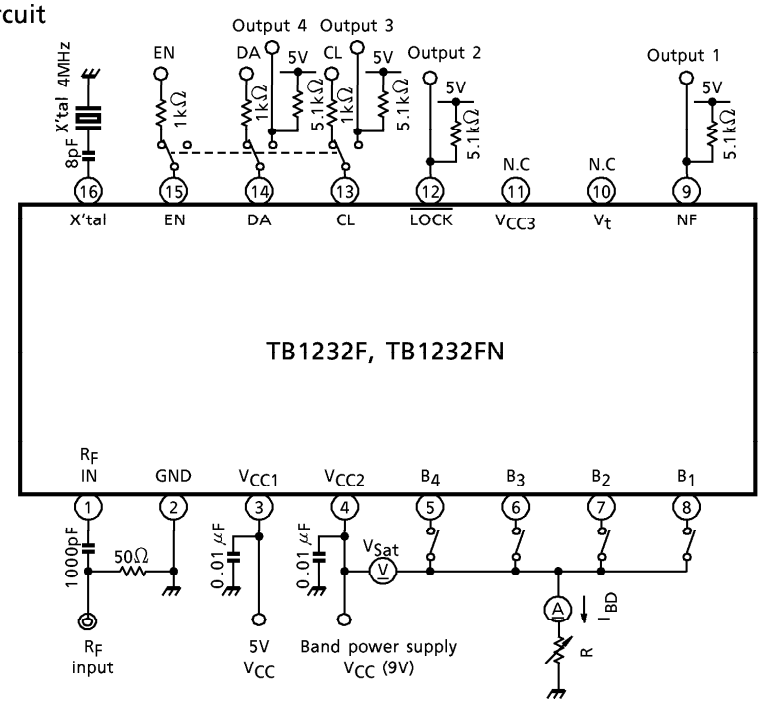
Input sensitivity test circuit



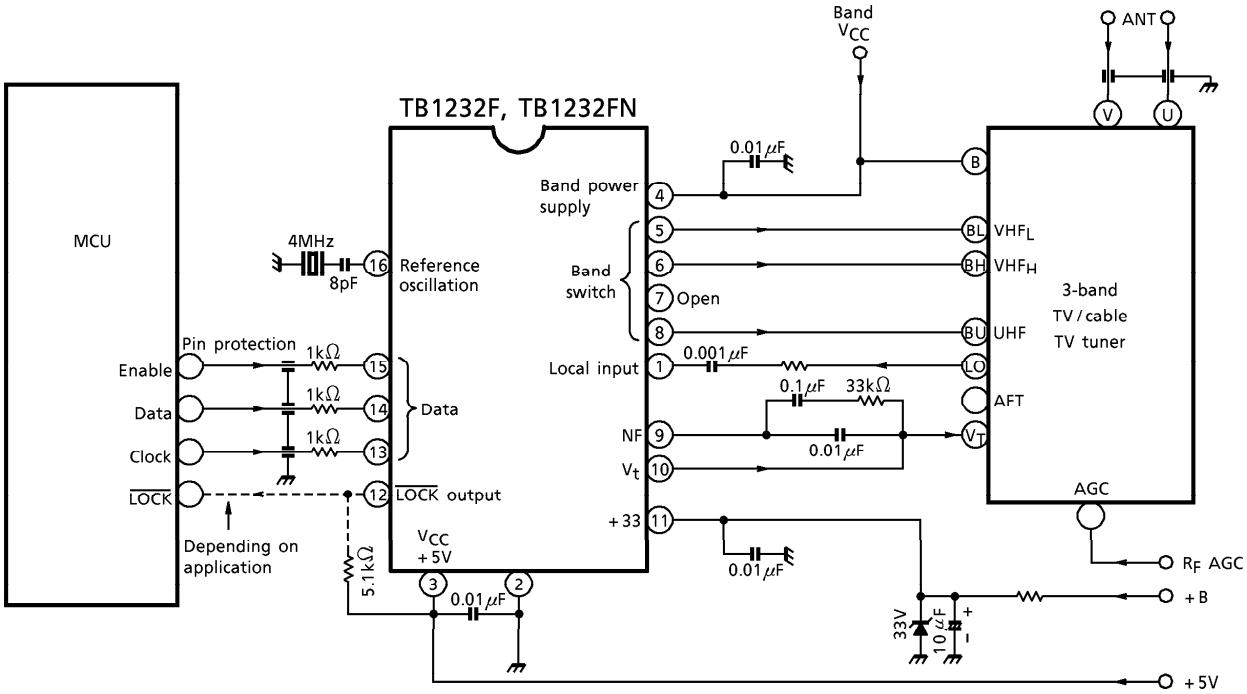
TEST CIRCUIT 3

Band drive test circuit

Test mode circuit

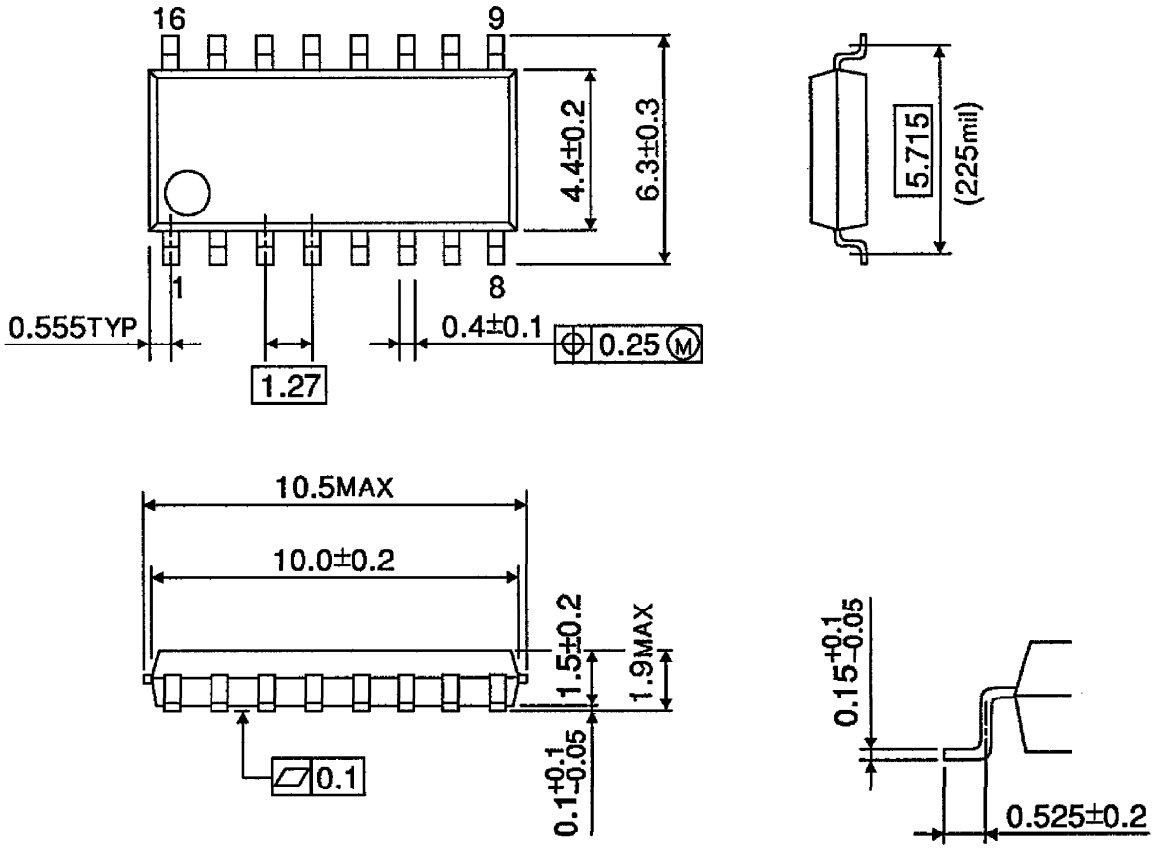


SYSTEM APPLICATION DIAGRAM



OUTLINE DRAWING

SOP16-P-225-1.27 Unit : mm

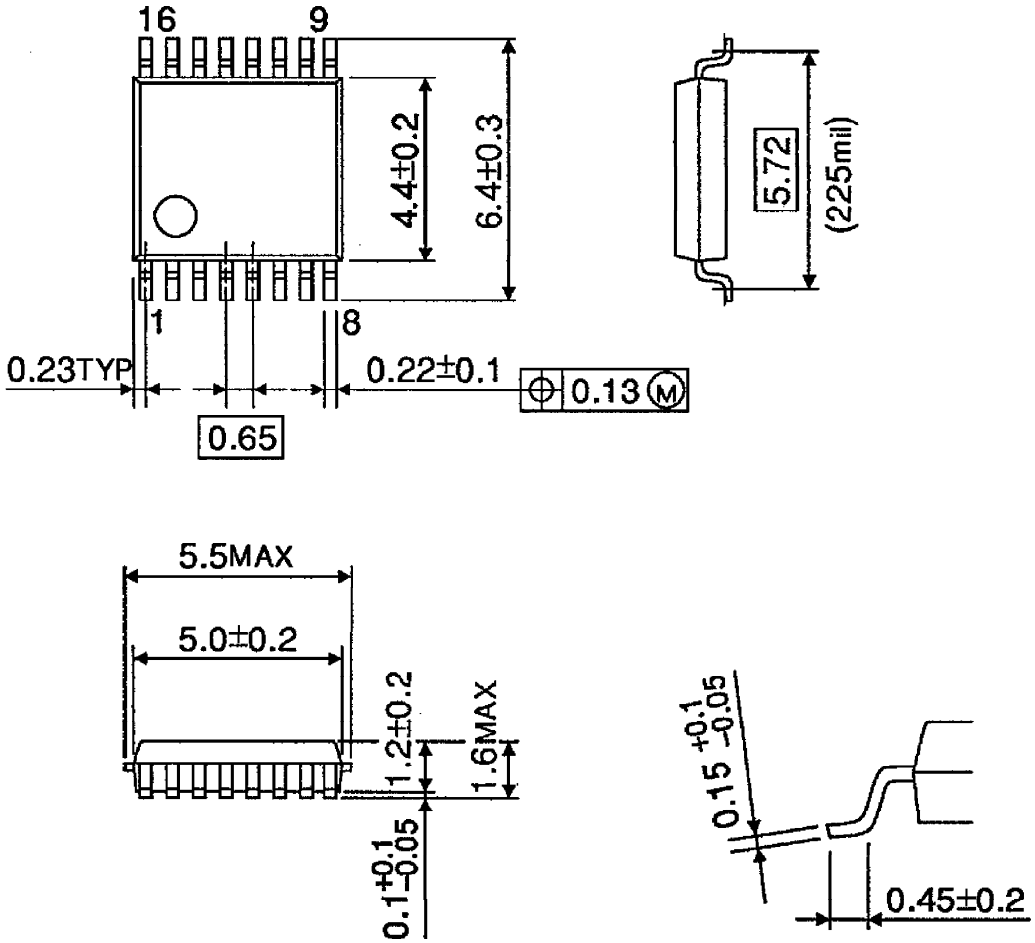


Weight : 0.16g (Typ.)

OUTLINE DRAWING

SSOP16-P-225-0.65B

Unit : mm



Weight : 0.07g (Typ.)