

## 20-W STEREO DIGITAL AUDIO POWER AMPLIFIER

Check for Samples: [TAS5701](#)

### FEATURES

- **Audio Input/Output**
  - 20-W Into an 8- $\Omega$  Load From an 18-V Supply
  - Wide PVDD Range (0 V to 21 V)
  - Efficient Class-D Operation Eliminates Need for Heat Sinks
  - Two Serial Audio Inputs (3 Audio channels)
  - Supports 32-kHz to 192-kHz Sample Rates (LJ/RJ/I<sup>2</sup>S)
  - Line-Level Subwoofer PWM Outputs
- **Audio/PWM Processing**
  - **BD (Filter-free) Modulation Supporting Bridge-Tied Loads ONLY**
  - **4-Step Volume Control (0 dB, 6 dB, 12 dB, 18 dB)**
    - All Channels Share Same Control
  - **Soft Mute (50% Duty Cycle)**
  - **DC Blocking Filters**
  - **Fixed Maximum Modulation Limit At 97.7%**
  - **$\geq 100$ -dB SNR – Measured at Maximum Output With THD+N = 1%, 1 kHz, A-Weighted Noise, Gain = 0 dB**
  - **THD < 0.1% at 1/2 Rated Power**

- **General Features**

- **5-V Tolerant Inputs (See pin list for details on which inputs are 5-V tolerant)**
- **Shutdown Mode for Low Power Consumption**
- **Thermal and Short-Circuit Protection**
- **Autodetect: Automatically Detect Sample-Rate Changes – No Need for External Microprocessor Intervention**

### DESCRIPTION

The TAS5701 is a 20-W efficient, digital audio power amplifier for driving stereo bridge-tied speakers. Two serial data inputs support up to 3 discrete audio channels. The SDIN1 input is routed to the internal left and right outputs. The SDIN2 input is dedicated to the SUB\_PWM $\pm$  outputs.

The TAS5701 is a clock slave-only device receiving clocks from external sources. The TAS5701 operates at a 384-kHz switching rate for 32-, 48-, 96-, and 192-kHz data and 352.8-kHz switching rate 44.1-, 88.2-, and 176.4-kHz data. The 8 $\times$  oversampling combined with the fourth-order noise shaper provides a flat noise floor and excellent dynamic range from 20 Hz to 20 kHz.

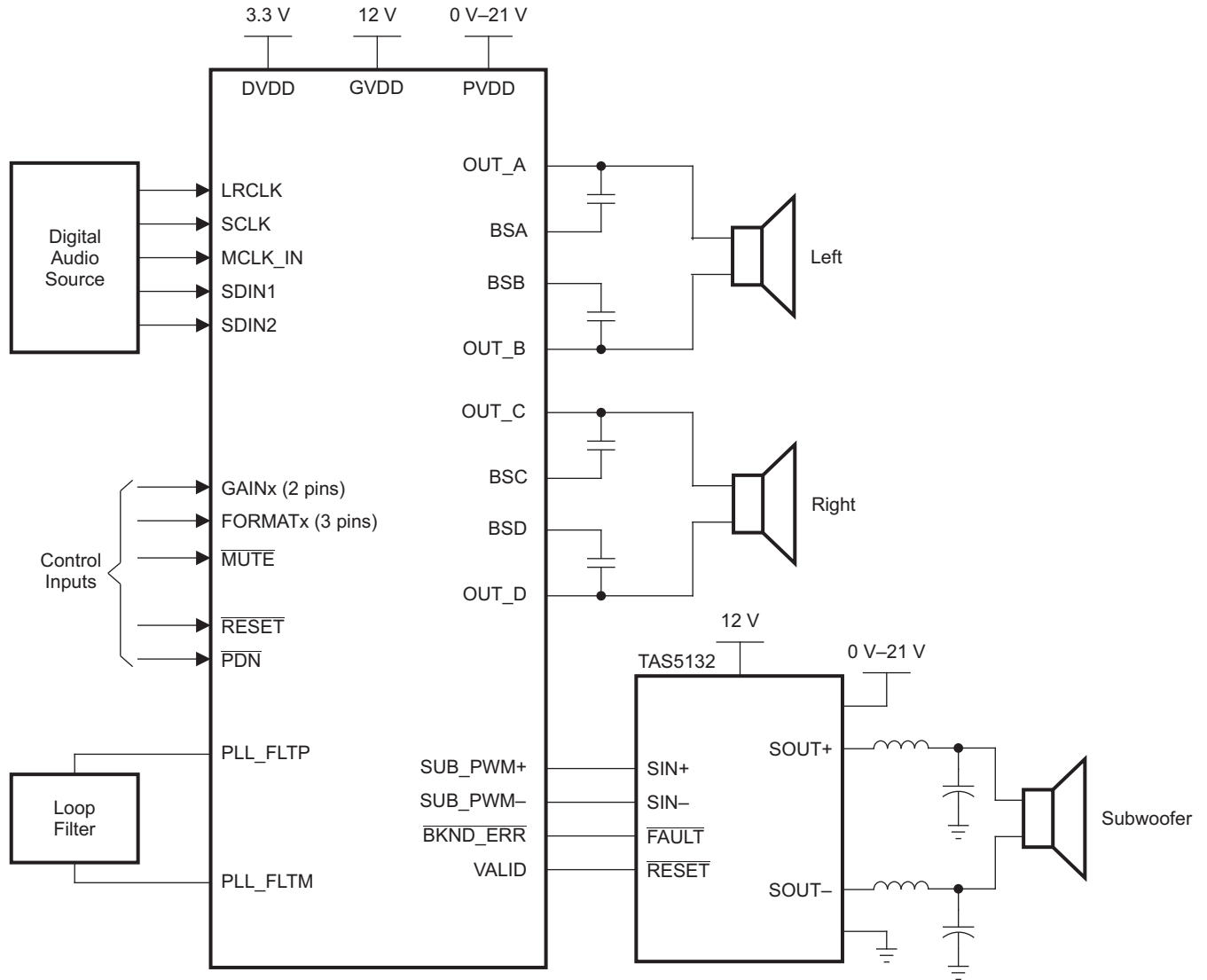


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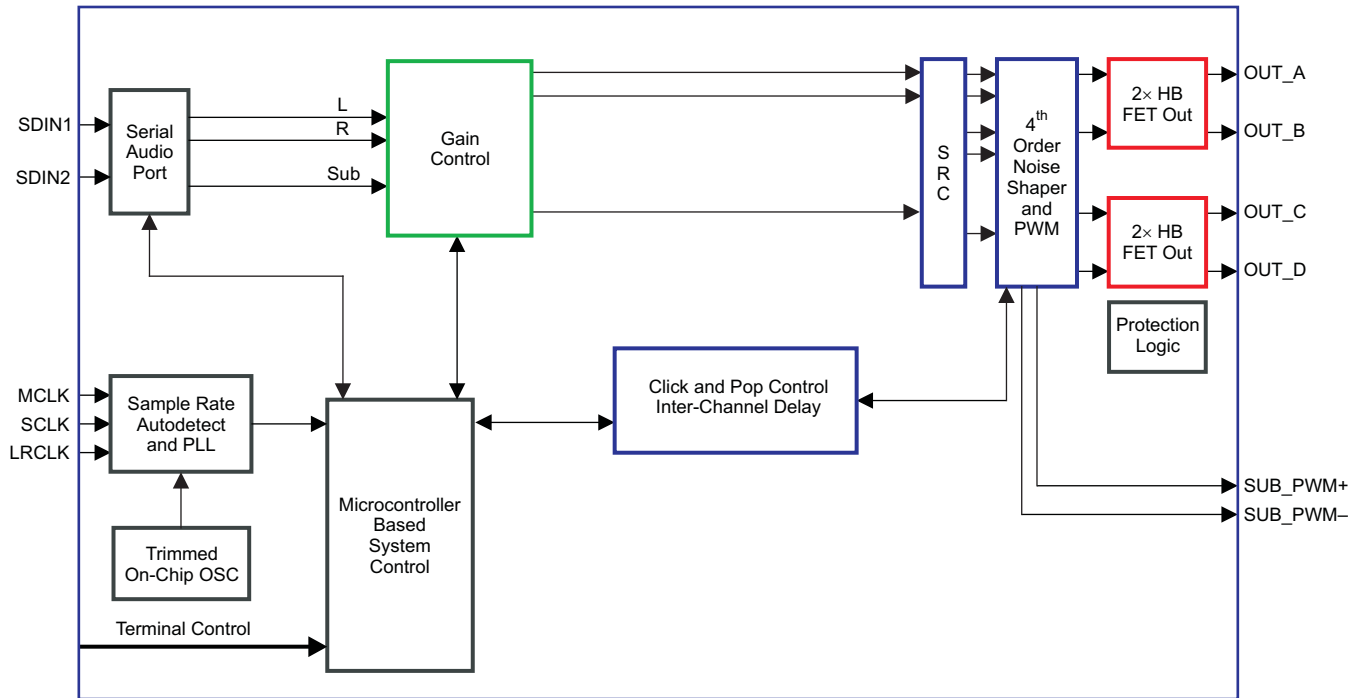
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**SIMPLIFIED APPLICATION DIAGRAM**

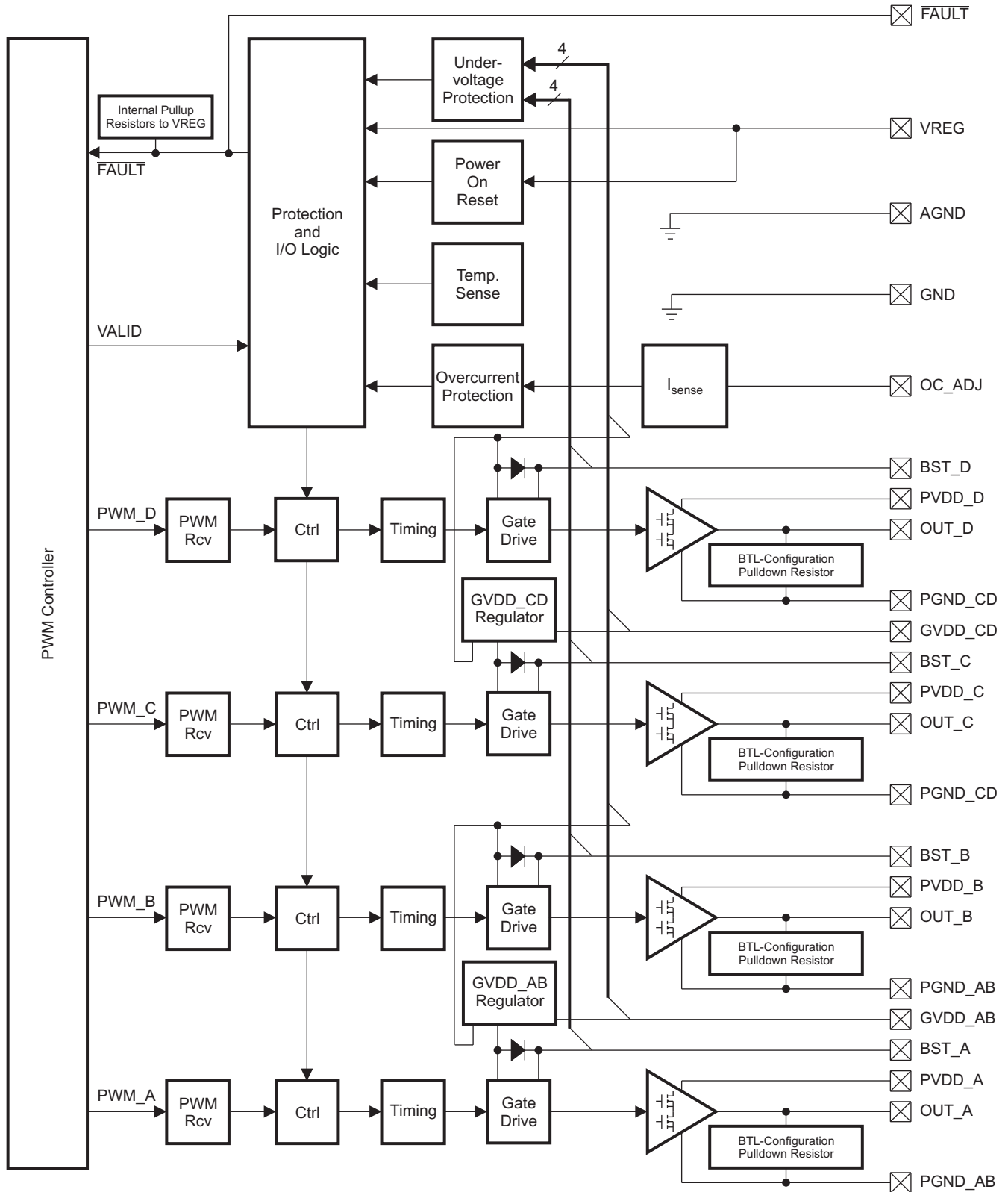


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FUNCTIONAL BLOCK DIAGRAM



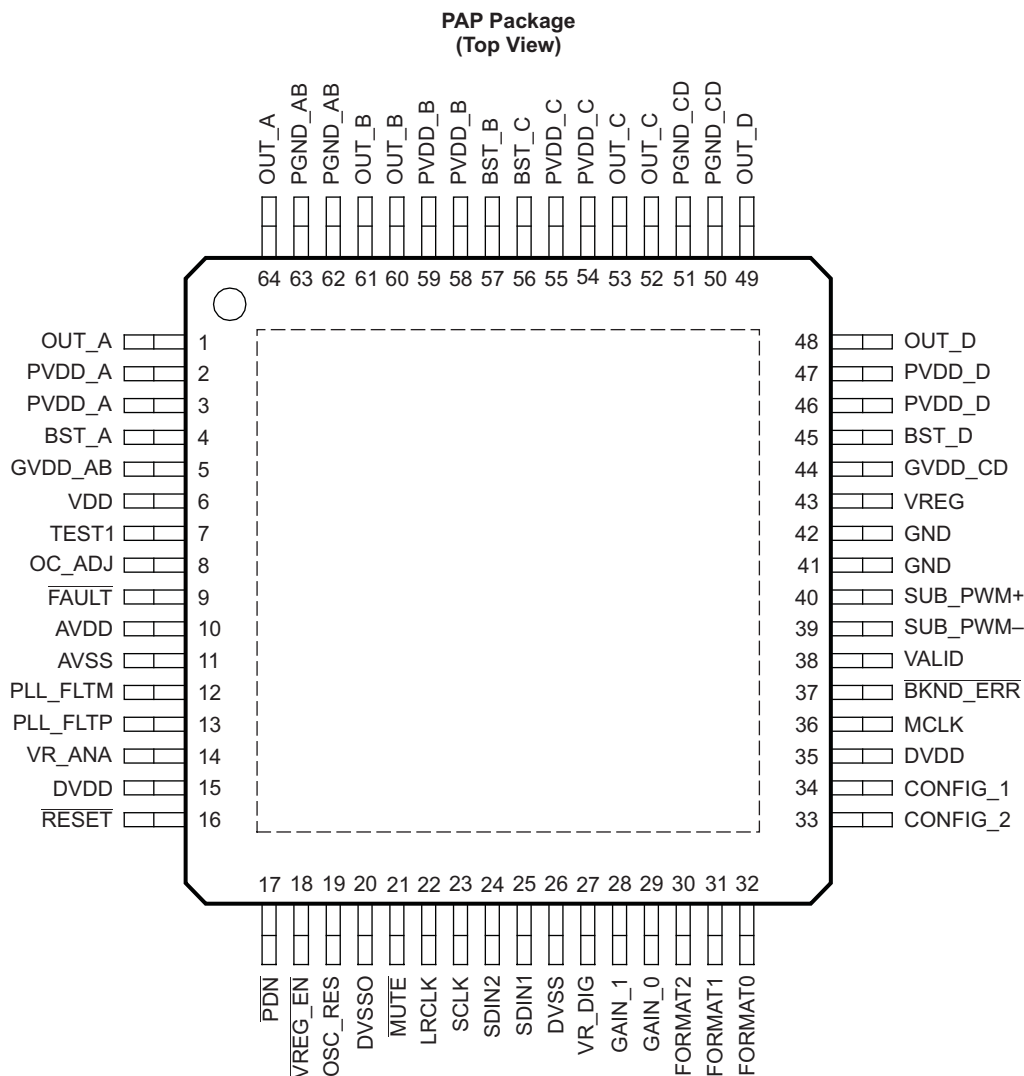
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Figure 1. Power Stage Functional Block Diagram

64-PIN, HTQFP PACKAGE (TOP VIEW)



P0071-03

PIN FUNCTIONS

| PIN      |     | I/O (1) | 5-V TOLERANT | TERMINATION (2) (3) | DESCRIPTION   |
|----------|-----|---------|--------------|---------------------|---|
| NAME     | NO. |         |              |                     |   |
| AVDD     | 10  | P       |              |                     | 3.3-V Analog power supply   |
| AVSS     | 11  | P       |              |                     | Analog 3.3-V supply ground  |
| BKND_ERR | 37  | DI      |              | Pullup              | Active low. A back-end error sequence is initiated by applying a logic low to this pin. Connect to an external power stage. If no external power stage is used, connect directly to DVDD. |
| BST_A    | 4   | P       |              |                     | High-side bootstrap supply for half-bridge A  |
| BST_B    | 57  | P       |              |                     | High-side bootstrap supply for half-bridge B  |
| BST_C    | 56  | P       |              |                     | High-side bootstrap supply for half-bridge C  |

- (1) TYPE: A = analog; D = 3.3-V digital; P = power/ground/decoupling; I = input; O = output
- (2) All pullups are 20- $\mu$ A *weak* pullups and all pulldowns are 20- $\mu$ A *weak* pulldowns. The pullups and pulldowns are included to assure proper input logic levels if the terminals are left unconnected (pullups  $\rightarrow$  logic 1 input; pulldowns  $\rightarrow$  logic 0 input). Devices that drive inputs with pullups must be able to sink 50  $\mu$ A while maintaining a logic-0 drive level. Devices that drive inputs with pulldowns must be able to source 50  $\mu$ A while maintaining a logic-1 drive level.
- (3) If desired, low-ESR capacitance values can be implemented by paralleling two or more ceramic capacitors of equal value. Paralleling capacitors of equal value provides an extended high-frequency supply decoupling. This approach avoids the potential of producing parallel resonance circuits that have been observed when paralleling capacitors of different values.

**PIN FUNCTIONS (continued)**

| PIN                       |        | I/O <sup>(1)</sup> | 5-V<br>TOLERANT | TERMINATION<br><sup>(2)</sup> <sup>(3)</sup> | DESCRIPTION  |
|---------------------------|--------|--------------------|-----------------|--|--|
| NAME                      | NO.    |                    |                 |  |  |
| BST_D                     | 45     | P                  |                 |  | High-side bootstrap supply for half-bridge D   |
| CONFIG_2                  | 33     | P                  |                 | Pulldown                                     | Input/output configuration. Connect this terminal directly to GND.   |
| CONFIG_1                  | 34     | P                  |                 | Pulldown                                     | Input/output configuration. Connect this terminal directly to DVDD.  |
| DVDD                      | 15, 35 | P                  |                 |  | 3.3-V Digital power supply   |
| DVSS                      | 26     | P                  |                 |  | Digital ground   |
| DVSSO                     | 20     | P                  |                 |  | Oscillator ground  |
| $\overline{\text{FAULT}}$ | 9      | DO                 |                 |  | Overtemperature, undervoltage, and overcurrent fault reporting. Active low indicates fault. If high, normal operation.   |
| FORMAT2                   | 30     | DI                 |                 | Pulldown                                     | Digital data format select MSB.  |
| FORMAT1                   | 31     | DI                 |                 | Pulldown                                     | Digital data format select LSB.  |
| FORMAT0                   | 32     | DI                 |                 | Pulldown                                     | Digital data format select.  |
| GAIN_1                    | 28     | DI                 | 5-V             |  | MSB of gain select.  |
| GAIN_0                    | 29     | DI                 | 5-V             |  | LSB of gain select. GAIN_0 and GAIN_1 allow 4 possible gain selections.  |
| GND                       | 41, 42 | P                  |                 |  | Analog ground for power stage.   |
| GVDD_AB                   | 5      | P                  |                 |  | Gate drive voltage for half-bridges A and B (10.8 V to 13.2 V)   |
| GVDD_CD                   | 44     | P                  |                 |  | Gate drive voltage for half-bridges C and D (10.8 V to 13.2 V)   |
| LRCLK                     | 22     | DI                 | 5-V             |  | Input serial audio data left/right clock (sampling rate clock)   |
| MCLK                      | 36     | DI                 | 5-V             |  | Clock master input. The input frequency of this clock can range from 4.9 MHz to 49 MHz.  |
| $\overline{\text{MUTE}}$  | 21     | DI                 | 5-V             | Pullup                                       | Performs a soft mute of outputs, active-low. A logic low on this pin sets the outputs equal to 50% duty cycle. A logic high on this pin allows normal operation. The mute control provides a noiseless volume ramp to silence. Releasing mute provides a noiseless ramp to previous volume.  |
| OC_ADJ                    | 8      | AO                 |                 |  | Analog overcurrent programming. Requires 22-k $\Omega$ resistor to ground.   |
| OSC_RES                   | 19     | AO                 |                 |  | Oscillator trim resistor. Connect an 18.2-k $\Omega$ (1% tolerance is required) resistor to DVSSO.   |
| OUT_A                     | 1, 64  | O                  |                 |  | Output, half-bridge A  |
| OUT_B                     | 60, 61 | O                  |                 |  | Output, half-bridge B  |
| OUT_C                     | 52, 53 | O                  |                 |  | Output, half-bridge C  |
| OUT_D                     | 48, 49 | O                  |                 |  | Output, half-bridge D  |
| $\overline{\text{PDN}}$   | 17     | DI                 | 5-V             | Pullup                                       | Power down, active-low. $\overline{\text{PDN}}$ stops all clocks, and outputs stop switching whenever a logic low is applied. When $\overline{\text{PDN}}$ is released, the device powers up all logic, starts all clocks, and performs a soft start that returns to the previous configuration changes to FORMATx and GAINx pins are ignored on $\overline{\text{PDN}}$ cycling.  |
| PGND_AB                   | 62, 63 | P                  |                 |  | Power ground for half-bridges A and B  |
| PGND_CD                   | 50, 51 | P                  |                 |  | Power ground for half-bridges C and D  |
| PLL_FLTM                  | 12     | AO                 |                 |  | PLL negative loop filter terminal  |
| PLL_FLTP                  | 13     | AI                 |                 |  | PLL positive loop filter terminal  |
| PVDD_A                    | 2, 3   | P                  |                 |  | Power supply input for half-bridge output A (0 V–21 V)   |
| PVDD_B                    | 58, 59 | P                  |                 |  | Power supply input for half-bridge output B (0 V–21 V)   |
| PVDD_C                    | 54, 55 | P                  |                 |  | Power supply input for half-bridge output C (0 V–21 V)   |
| PVDD_D                    | 46, 47 | P                  |                 |  | Power supply input for half-bridge output D (0 V–21 V)   |
| $\overline{\text{RESET}}$ | 16     | DI                 | 5-V             | Pullup                                       | Reset, active-low. A <u>system</u> reset is generated by applying a logic low to this terminal. $\overline{\text{RESET}}$ is an asynchronous control signal that sets the VALID outputs low, and places the PWM in the hard mute state (stop switching). Gain is immediately set to full attenuation. Upon the release of $\overline{\text{RESET}}$ , if $\overline{\text{PDN}}$ is high, the system performs a 4-ms to 5-ms device initialization and sets the gain and format to the settings determined by the hardware pins. |

**PIN FUNCTIONS (continued)**

| PIN      |     | I/O <sup>(1)</sup> | 5-V<br>TOLERANT | TERMINATION<br><sup>(2)</sup> <sup>(3)</sup> | DESCRIPTION   |
|----------|-----|--------------------|-----------------|--|---|
| NAME     | NO. |                    |                 |  |   |
| SCLK     | 23  | DI                 | 5-V             |  | Serial audio data clock (shift clock). SCLK is the serial audio port input data bit clock.  |
| SDIN1    | 25  | DI                 | 5-V             |  | Serial audio data 1 input is one of the serial data input ports. SDIN1 supports three discrete (stereo) data formats.   |
| SDIN2    | 24  | DI                 | 5-V             |  | Serial audio data 2 input is one of the serial data input ports. SDIN2 supports three discrete (stereo) data formats.   |
| SUB_PWM– | 39  | DO                 |                 |  | Subwoofer negative PWM output. BD modulated signal.   |
| SUB_PWM+ | 40  | DO                 |                 |  | Subwoofer positive PWM output. BD modulated signal.   |
| TEST1    | 7   | DI                 |                 |  | Test pin. Connect directly to GND.  |
| VALID    | 38  | DO                 |                 |  | Output indicating validity of ALL PWM channels, active-high. This pin is connected to an external power stage. If no external power stage is used, leave this pin floating. |
| VDD      | 6   | P                  |                 |  | Power supply for VREG (10.8 V to 13.2 V)  |
| VR_ANA   | 14  | P                  |                 |  | Internally regulated 1.8-V analog supply voltage. This terminal must not be used to power external devices.   |
| VR_DIG   | 27  | P                  |                 |  | Internally regulated 1.8-V analog supply voltage. This terminal must not be used to power external devices.   |
| VREG     | 43  | P                  |                 |  | Digital regulator output. Not to be used for powering external circuitry.   |
| VREG_EN  | 18  | DI                 |                 | Pulldown                                     | Voltage regulator enable. Connect directly to GND.  |

**ABSOLUTE MAXIMUM RATINGS**

 over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|  |   | VALUE              | UNIT |
|--|---|--------------------|------|
| Supply voltage   | GVDD, VDD                                 | –0.3 to 13.2       | V    |
|  | PVDD                                      | –0.3 to 23         |      |
|  | DVDD                                      | –0.3 to 3.6        |      |
|  | AVDD                                      | –0.3 to 3.6        |      |
|  | OUT_X to GND_X                            | –0.3 to 30         |      |
|  | BST_X to GND_X                            | –0.3 to 43.2       |      |
| Input voltage  | 3.3-V digital input                       | –0.5 to DVDD + 0.5 | V    |
|  | 5-V tolerant <sup>(2)</sup> digital input | –0.5 to DVDD + 2.5 |      |
| Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > 1.8 V)  |   | ±20                | mA   |
| Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > 1.8 V) |   | ±20                | mA   |
| Operating free-air temperature   |   | 0 to 85            | °C   |
| Operating junction temperature range   |   | 0 to 150           | °C   |
| Storage temperature range, T <sub>stg</sub>  |   | –40 to 125         | °C   |

- (1) Stresses beyond those listed under *absolute ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operation conditions* are not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
- (2) 5-V tolerant inputs are PDN, RESET, MUTE, SCLK, LRCLK, MCLK, SDIN1, SDIN2.

## THERMAL INFORMATION

| THERMAL METRIC <sup>(1)(2)</sup> |  | TAS5701       | UNITS |
|----------------------------------|--|---------------|-------|
|                                  |  | PAP (64 PINS) |       |
| $\theta_{JA}$                    | Junction-to-ambient thermal resistance       | 27.2          | °C/W  |
| $\theta_{JCTop}$                 | Junction-to-case (top) thermal resistance    | 16            |       |
| $\theta_{JB}$                    | Junction-to-board thermal resistance         | 13            |       |
| $\psi_{JT}$                      | Junction-to-top characterization parameter   | 0.1           |       |
| $\psi_{JB}$                      | Junction-to-board characterization parameter | 7.9           |       |
| $\theta_{JCbott}$                | Junction-to-case (bottom) thermal resistance | 0.9           |       |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

|                              |                                      | MIN   | NOM | MAX  | UNIT     |
|------------------------------|--------------------------------------|---|-----|------|----------|
| Gate drive supply voltage    | GVDD, VDD                            | 10.8  | 12  | 13.2 | V        |
| Output bridge supply voltage | PVDD                                 | 0   |     | 21   | V        |
| Digital supply voltage       | DVDD                                 | 3   | 3.3 | 3.6  | V        |
| Analog supply voltage        | AVDD                                 | 3   | 3.3 | 3.6  | V        |
| $V_{IH}$                     | High-level input voltage             | 3.3-V TTL, 5-V tolerant                                 |     |      | V        |
| $V_{IL}$                     | Low-level input voltage              | 3.3-V TTL, 5-V tolerant                                 |     |      | V        |
| $T_A$                        | Operating ambient temperature range  | 0   |     | 85   | °C       |
| $T_J$                        | Operating junction temperature range | 0   |     | 150  | °C       |
| $R_L$ (BTL)                  | Load impedance                       | Output filter: L = 22 $\mu$ H, C = 680 nF.              | 6.0 | 8    | $\Omega$ |
| $R_L$ (SE)                   |                                      |   | 3.2 | 4    |          |
| $R_L$ (PBTL)                 |                                      |   | 3.2 | 4    |          |
| $L_O$ (BTL)                  | Output-filter inductance             | Minimum output inductance under short-circuit condition | 10  |      | $\mu$ H  |
| $L_O$ (SE)                   |                                      |   | 10  |      |          |
| $L_O$ (PBTL)                 |                                      |   | 10  |      |          |

## PWM OPERATION AT RECOMMENDED OPERATING CONDITIONS

| PARAMETER                            | TEST CONDITIONS                             | MODE                        | VALUE | UNIT |
|--------------------------------------|---|-----------------------------|-------|------|
| Output sample rate 2x–1x oversampled | 32-kHz data rate $\pm 2\%$                  | 12x sample rate             | 384   | kHz  |
|                                      | 44.1-, 88.2-, 176.4-kHz data rate $\pm 2\%$ | 8x, 4x, and 2x sample rates | 352.8 | kHz  |
|                                      | 48-, 96-, 192-kHz data rate $\pm 2\%$       | 8x, 4x, and 2x sample rates | 384   | kHz  |

## PLL INPUT PARAMETERS AND EXTERNAL FILTER COMPONENTS

| PARAMETER                                      | TEST CONDITIONS  | MIN | TYP | MAX  | UNIT     |
|--|--|-----|-----|------|----------|
| $f_{MCLKI}$ Frequency, MCLK ( $1 / t_{cyc2}$ ) |  | 4.9 |     | 49.2 | MHz      |
| MCLK duty cycle                                |  | 40% | 50% | 60%  |          |
| MCLK minimum high time                         | $\geq 2$ -V MCLK = 49.152 MHz, within the min and max duty cycle constraints   | 8   |     |      | ns       |
| MCLK minimum low time                          | $\leq 0.8$ -V MCLK = 49.152 MHz, within the min and max duty cycle constraints | 8   |     |      | ns       |
| LRCLK allowable drift before LRCLK reset       |  |     |     | 4    | MCLKs    |
| External PLL filter capacitor C1               | SMD 0603 Y5V   |     | 47  |      | nF       |
| External PLL filter capacitor C2               | SMD 0603 Y5V   |     | 4.7 |      | nF       |
| External PLL filter resistor R                 | SMD 0603, metal film   |     | 470 |      | $\Omega$ |



## ELECTRICAL CHARACTERISTICS

### DC Characteristics

 $T_A = 25\text{ }^\circ\text{C}$ ,  $PVCC\_X = 18\text{ V}$ ,  $DVDD = AVDD = 3.3\text{ V}$ ,  $R_L = 8\text{ }\Omega$  (unless otherwise noted)

| PARAMETER                           |   | TEST CONDITIONS   | MIN   | TYP | MAX      | UNIT          |                  |
|-------------------------------------|---|---|---|-----|----------|---------------|------------------|
| $V_{OH}$                            | High-level output voltage                                     | 3.3-V TTL and 5-V tolerant <sup>(1)</sup>   | $I_{OH} = -4\text{ mA}$                             | 2.4 |          | V             |                  |
| $V_{OL}$                            | Low-level output voltage                                      | 3.3-V TTL and 5-V tolerant <sup>(1)</sup>   | $I_{OL} = 4\text{ mA}$                              |     | 0.5      | V             |                  |
| $I_{IL}$                            | Low-level input current                                       | LRCLK, SCLK, SDINx, MCLK, GAIN_x, VREG_EN, FORMATx, CONFIG_x  | $V_I = 0\text{ V}$ , $DVDD = 3.6\text{ V}$          |     | $\pm 2$  | $\mu\text{A}$ |                  |
|                                     |   | BKND_ERR, RESET, PDN, MUTE  | $V_I = 0\text{ V}$ , $DVDD = 3.6\text{ V}$          |     | $\pm 50$ |               |                  |
| $I_{IH}$                            | High-level input current                                      | RESET, PDN, MUTE, GAIN_x, BKND_ERR  | $V_I = 3.6\text{ V}$ , $DVDD = 3.6\text{ V}$        |     | $\pm 2$  | $\mu\text{A}$ |                  |
|                                     |   | VREG_EN, FORMAT_x, CONFIG_x, LRCLK, SCLK, SDINx, MCLK   | $V_I = 3.6\text{ V}$ , $DVDD = 3.6\text{ V}$        |     | $\pm 50$ |               |                  |
|                                     |   | RESET, PDN, MUTE, LRCLK, SCLK, SDINx, MCLK, GAIN_x  | $V_I = 5.5\text{ V}$ , $DVDD = 3.6\text{ V}$        |     | $\pm 50$ |               |                  |
| $I_{DD}$                            | Input digital supply current                                  | Supply voltage (DVDD, AVDD)   | Normal mode, 50% duty cycle                         |     | 65       | 80            | mA               |
|                                     |   |   | Power down ( $\overline{\text{PDN}} = \text{low}$ ) |     | 8        | 16            |                  |
|                                     |   |   | Reset ( $\overline{\text{RESET}} = \text{low}$ )    |     | 23       | 33            |                  |
| $I_{GVDD}$                          | Gate supply current per GVDD_xx input                         |   | Normal mode, 50% duty cycle                         |     | 5        | 10            | mA               |
|                                     |   |   | $\overline{\text{RESET}} = 0$                       |     | 2.2      | 4             |                  |
|                                     |   |   | $\overline{\text{PDN}} = 0$                         |     | 2.2      | 4             |                  |
| $I_{PVDD}$                          | Input power supply current                                    |   | No load   |     | 30       | 60            | mA               |
| $I_{PVDD}(\overline{\text{PDN}})$   | Power-down current  |   | No load, $\overline{\text{PDN}} = 0$                |     | 1        | 100           | $\mu\text{A}$    |
| $I_{PVDD}(\overline{\text{RESET}})$ | Reset current   |   | No load, $\overline{\text{RESET}} = 0$              |     | 1        | 100           | $\mu\text{A}$    |
| $r_{DS(on)}$                        | Drain-to-source resistance, LS                                | $T_J = 25\text{ }^\circ\text{C}$ , includes metallization resistance                                      |   |     | 140      |               | m $\Omega$       |
|                                     | Drain-to-source resistance, HS                                | $T_J = 25\text{ }^\circ\text{C}$ , includes metallization resistance                                      |   |     | 140      |               |                  |
| <b>I/O Protection</b>               |   |   |   |     |          |               |                  |
| $V_{uvp}$                           | Undervoltage protection limit                                 | PVDD falling  |   |     | 9.2      |               | V                |
| $V_{uvp,hyst}$                      | Undervoltage protection limit                                 | PVDD rising   |   |     | 9.6      |               | V                |
| OTE <sup>(2)</sup>                  | Overtemperature error   |   |   |     | 150      |               | $^\circ\text{C}$ |
| OTE <sub>HYST</sub> <sup>(2)</sup>  | Extra temperature drop required to recover from error         |   |   |     | 30       |               | $^\circ\text{C}$ |
| OLPC                                | Overload protection counter                                   | $f_{PWM} = 384\text{ kHz}$  |   |     | 1.25     |               | ms               |
| $I_{OC}$                            | Overcurrent limit protection                                  | $R_{OCP} = 22\text{ k}\Omega$   |   |     | 4.5      |               | A                |
| $I_{OCT}$                           | Overcurrent response time                                     |   |   |     | 150      |               | ns               |
| $R_{OCP}$                           | OC programming resistor range                                 | Resistor tolerance = 5% for typical value; the minimum resistance should not be less than 20 k $\Omega$ . |   |     | 20       | 22            | k $\Omega$       |
| $R_{PD}$                            | Internal pull-down resistor at the output of each half-bridge | Connected when $\overline{\text{RESET}}$ is active to provide bootstrap capacitor charge.                 |   |     | 3        |               | k $\Omega$       |

(1) 5-V tolerant inputs are  $\overline{\text{PDN}}$ ,  $\overline{\text{RESET}}$ ,  $\overline{\text{MUTE}}$ , SCLK, LRCLK, MCLK, SDIN1, SDIN2, GAIN\_0, and GAIN\_1.

(2) Specified by design.

## AC Characteristics (BTL)

PVDD\_X = 18 V, BTL mode,  $R_L = 8 \Omega$ ,  $R_{OC} = 22 \text{ k}\Omega$ ,  $C_{BST} = 33\text{-nF}$ , audio frequency = 1 kHz, AES17 filter,  $F_{PWM} = 384 \text{ kHz}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted). All performance is in accordance with recommended operating conditions, unless otherwise specified.

| PARAMETER      |   | TEST CONDITIONS   | MIN | TYP   | MAX | UNIT          |
|----------------|---|---|-----|-------|-----|---------------|
| P <sub>O</sub> | Power output per channel                                    | PVDD = 18 V, 10% THD, 1-kHz input signal                  |     | 20.0  |     | W             |
|                |   | PVDD = 18 V, 7% THD, 1-kHz input signal                   |     | 18.6  |     |               |
|                |   | PVDD = 12 V, 10% THD, 1-kHz input signal                  |     | 9     |     |               |
|                |   | PVDD = 12 V, 7% THD, 1-kHz input signal                   |     | 8.3   |     |               |
| THD+N          | Total harmonic distortion + noise                           | PVDD = 18 V, P <sub>O</sub> = 10 W (half-power)           |     | 0.1%  |     |               |
|                |   | PVDD = 12 V, P <sub>O</sub> = 4.5 W (half-power)          |     | 0.08% |     |               |
|                |   | 1 W   |     | 0.05% |     |               |
| V <sub>n</sub> | Output integrated noise                                     | A-weighted  |     | 50    |     | $\mu\text{V}$ |
|                | Crosstalk   | P <sub>O</sub> = 1 W, f = 1 kHz                           |     | -73   |     | dB            |
| SNR            | Signal-to-noise ratio <sup>(1)</sup>                        | A-weighted, f = 1 kHz, maximum power at THD < 1%          |     | 101   |     | dB            |
| P <sub>D</sub> | Power dissipation due to idle losses (I <sub>PVDD_X</sub> ) | P <sub>O</sub> = 0 W, 4 channels switching <sup>(2)</sup> |     | 0.6   |     | W             |

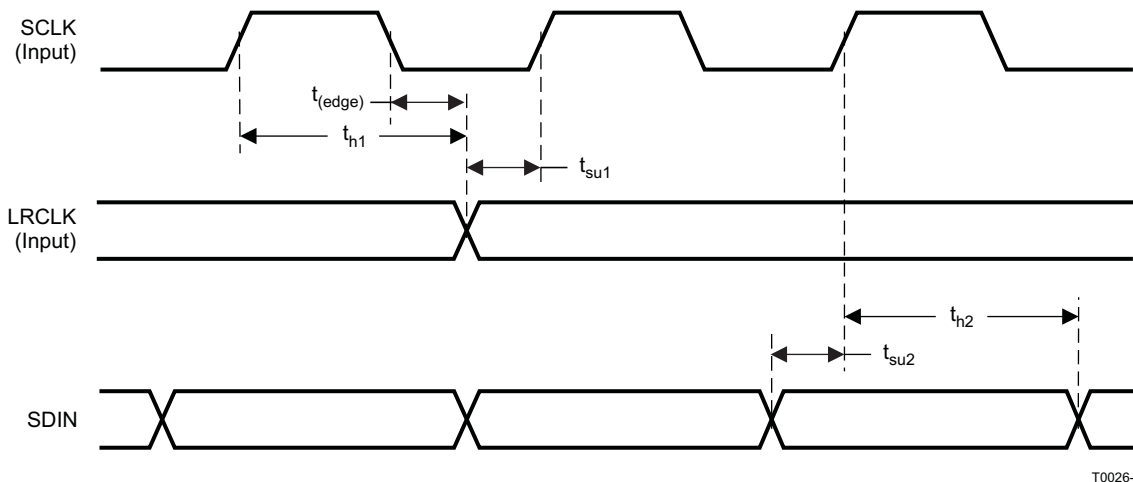
(1) SNR is calculated relative to 0-dBFS input level.

(2) Actual system idle losses are affected by core losses of output inductors.

### SERIAL AUDIO PORTS SLAVE MODE

Serial audio ports slave mode over recommended operating conditions (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS | MIN   | TYP | MAX    | UNIT        |
|--|-----------------|-------|-----|--------|-------------|
| $f_{SCLKIN}$ Frequency, SCLK $32 \times f_s$ , $48 \times f_s$ , $64 \times f_s$ | $C_L = 30$ pF   | 1.024 |     | 12.288 | MHz         |
| $t_{su1}$ Setup time, LRCLK to SCLK rising edge                                  |                 | 10    |     |        | ns          |
| $t_{h1}$ Hold time, LRCLK from SCLK rising edge                                  |                 | 10    |     |        | ns          |
| $t_{su2}$ Setup time, SDIN to SCLK rising edge                                   |                 | 10    |     |        | ns          |
| $t_{h2}$ Hold time, SDIN from SCLK rising edge                                   |                 | 10    |     |        | ns          |
| LRCLK frequency  |                 | 32    | 48  | 192    | kHz         |
| SCLK duty cycle  |                 | 40%   | 50% | 60%    |             |
| LRCLK duty cycle   |                 | 40%   | 50% | 60%    |             |
| SCLK rising edges between LRCLK rising edges                                     |                 | 32    |     | 64     | SCLK edges  |
| $t_{(edge)}$ LRCLK clock edge with respect to the falling edge of SCLK           |                 | -1/4  |     | 1/4    | SCLK period |



T0026-03

Figure 2. Slave Mode Serial Data Interface Timing

### HARDWARE SELECT PINS

over recommended operating conditions (unless otherwise noted)

| PARAMETER  | MIN | TYP | MAX | UNIT    |
|--|-----|-----|-----|---------|
| $t_{su}$ Setup time, FORMAT <sub>x</sub> , CONFIG <sub>x</sub> , GAIN <sub>x</sub> to $\overline{RESET}$ rising edge | 100 |     |     | $\mu$ s |

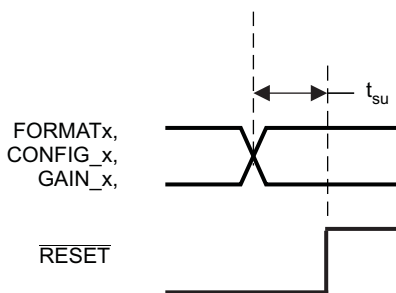
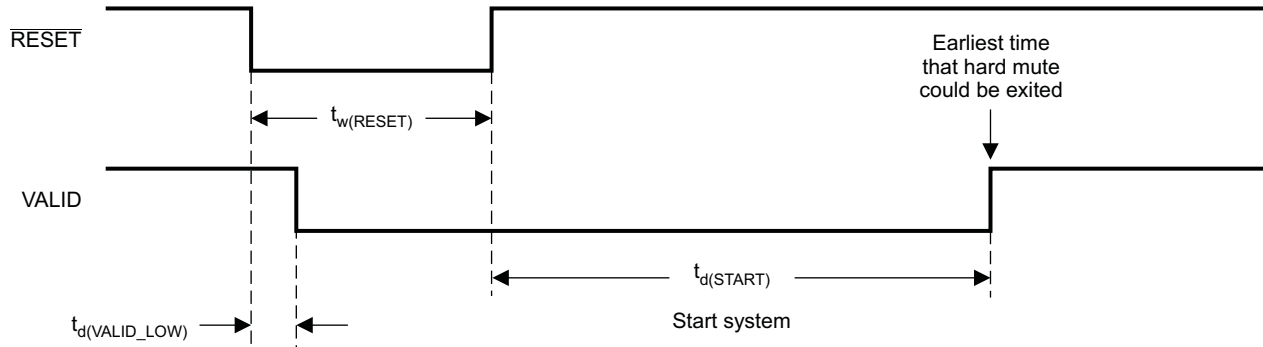


Figure 3. Mode Pins Setup Time

### RESET TIMING ( $\overline{\text{RESET}}$ ) AND POWER-ON RESET

Control signal parameters over recommended operating conditions (unless otherwise noted)

| PARAMETER                  |  | MIN | TYP | MAX | UNIT |
|----------------------------|--|-----|-----|-----|------|
| $t_{d(\text{VALID\_LOW})}$ | Time to assert VALID (reset to power stage) low  |     | 100 |     | ns   |
| $t_w(\text{RESET})$        | Pulse duration, $\overline{\text{RESET}}$ active | 100 | 200 |     | ms   |
| $t_{d(\text{START})}$      | Time to start-up                                 |     | 3.6 |     | ms   |



T0029-05

Figure 4. Reset Timing

When power is applied to DVDD,  $\overline{\text{RESET}}$  must be held low for at least 100  $\mu\text{s}$  after DVDD reaches 3.0 V.

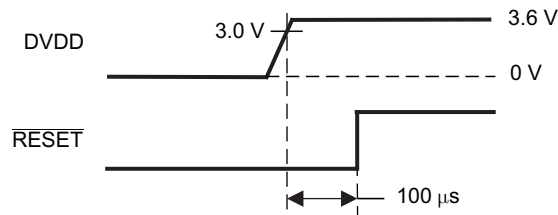
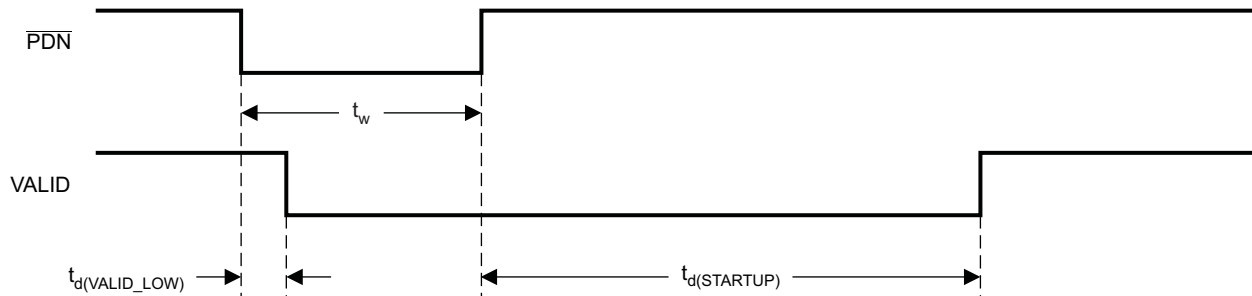


Figure 5. Power-On Reset Timing

### POWER-DOWN ( $\overline{\text{PDN}}$ ) TIMING

Control signal parameters over recommended operating conditions (unless otherwise noted)

| PARAMETER                  |   | MIN | TYP | MAX | UNIT          |
|----------------------------|---|-----|-----|-----|---------------|
| $t_{d(\text{VALID\_LOW})}$ | Time to assert VALID (reset to power stage) low |     | 725 |     | $\mu\text{s}$ |
| $t_{d(\text{STARTUP})}$    | Device start-up time                            |     | 650 |     | $\mu\text{s}$ |
| $t_w$                      | Minimum pulse duration required                 | 1   |     |     | $\mu\text{s}$ |



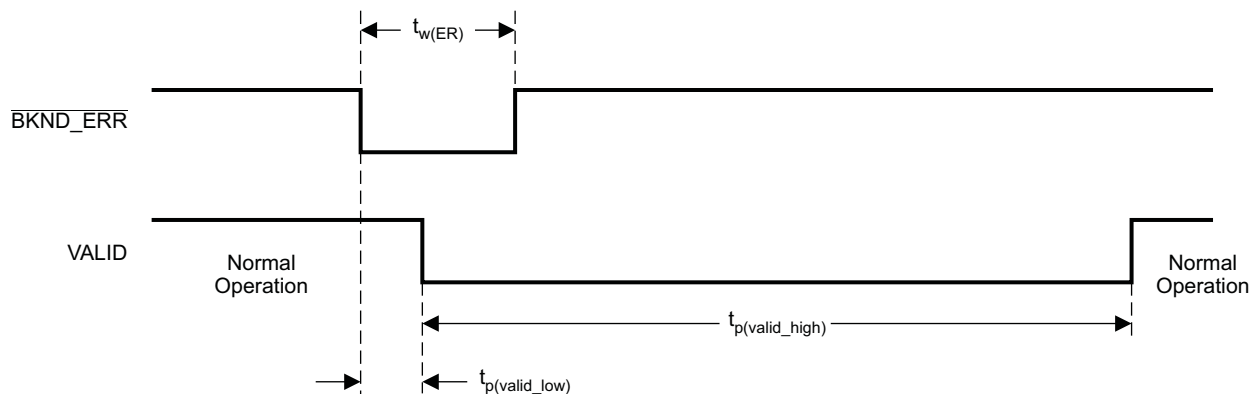
T0030-04

Figure 6. Power-Down Timing

### BACK-END ERROR ( $\overline{\text{BKND\_ERR}}$ )

Control signal parameters over recommended operating conditions (unless otherwise noted)

| PARAMETER                   |  | MIN | TYP | MAX | UNIT |
|-----------------------------|--|-----|-----|-----|------|
| $t_{w(\text{ER})}$          | Pulse duration, $\overline{\text{BKND\_ERR}}$ active (active-low)  | 350 |     |     | ns   |
| $t_{p(\text{valid\_high})}$ | Time to stay in the $\text{OUT}_x$ low state. After $t_{p(\text{valid\_high})}$ , the TAS5701 attempts to bring the system out of the $\text{OUT}_x$ low state if $\overline{\text{BKND\_ERR}}$ is high. |     | 300 |     | ms   |
| $t_{p(\text{valid\_low})}$  | Time TAS5701 takes to bring $\text{OUT}_x$ low after $\overline{\text{BKND\_ERR}}$ assertion.  |     | 350 |     | ns   |



T0031-04

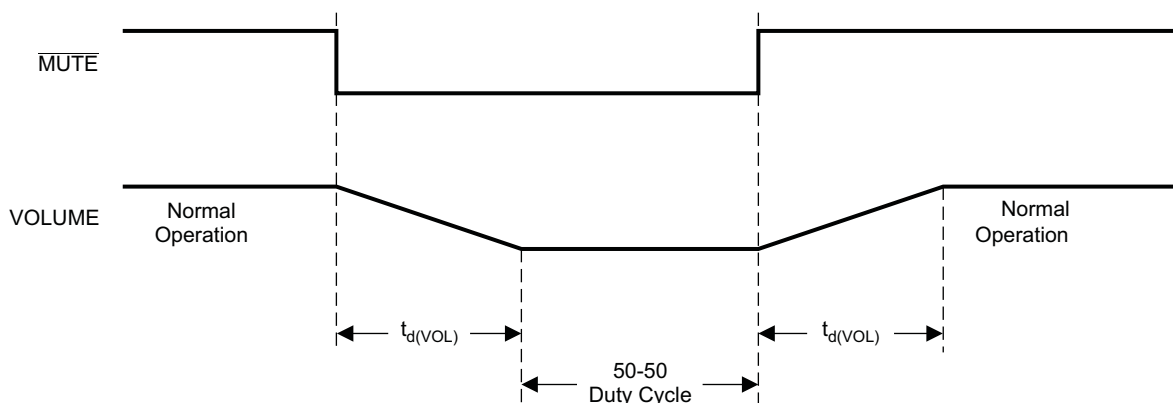
Figure 7. Error Recovery Timing

### MUTE TIMING ( $\overline{\text{MUTE}}$ )

Control signal parameters over recommended operating conditions (unless otherwise noted)

| PARAMETER           |  | MIN | TYP  | MAX | UNIT  |
|---------------------|--|-----|------|-----|-------|
| $t_{d(\text{VOL})}$ | Volume ramp time. Ramp time = Number of steps $\times$ stepsize <sup>(1)</sup> |     | 1024 |     | steps |

(1) Stepsize = 4 LRCLKs (for 32–48 kHz sample rate); 8 LRCLKs (for 88.2–96 kHz sample rate); 16 LRCLKs (for 176.4–192 kHz sample rate)



T0032-03

Figure 8. Mute Timing

**TYPICAL CHARACTERISTICS, BTL CONFIGURATION**

**TOTAL HARMONIC DISTORTION + NOISE  
vs  
OUTPUT POWER**

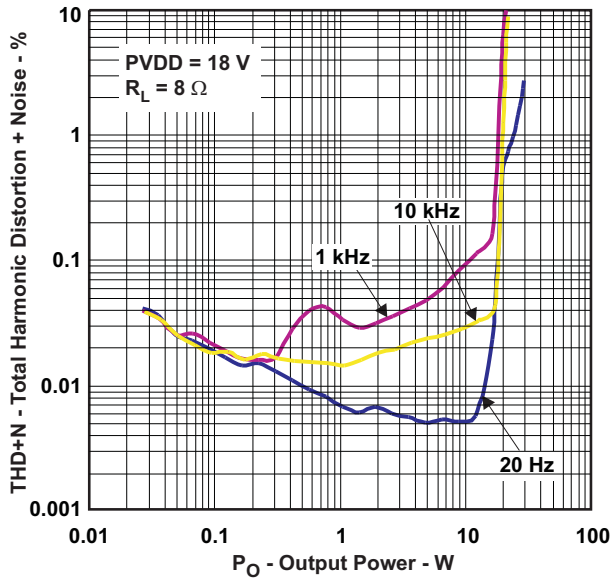


Figure 9.

**TOTAL HARMONIC DISTORTION + NOISE  
vs  
OUTPUT POWER**

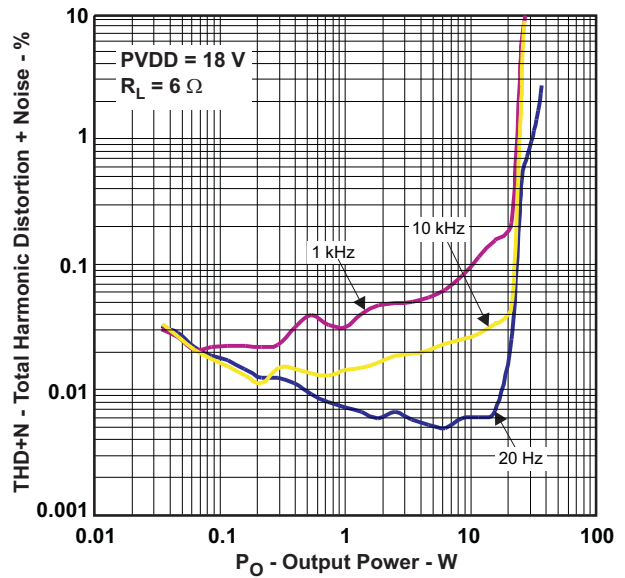


Figure 10.

**TOTAL HARMONIC DISTORTION + NOISE  
vs  
FREQUENCY**

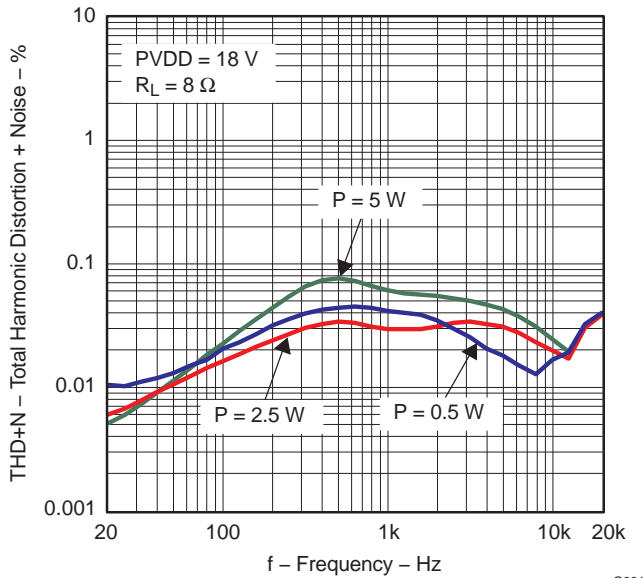


Figure 11.

**TOTAL HARMONIC DISTORTION + NOISE  
vs  
FREQUENCY**

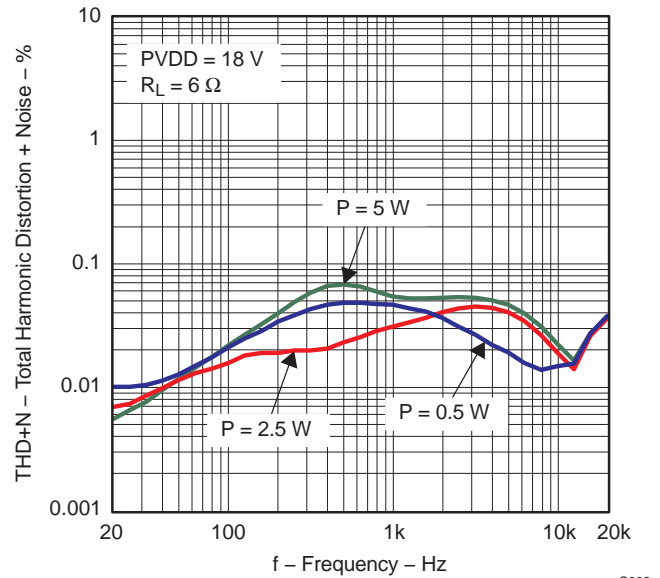


Figure 12.

**TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)**

**SYSTEM EFFICIENCY  
vs  
OUTPUT POWER**

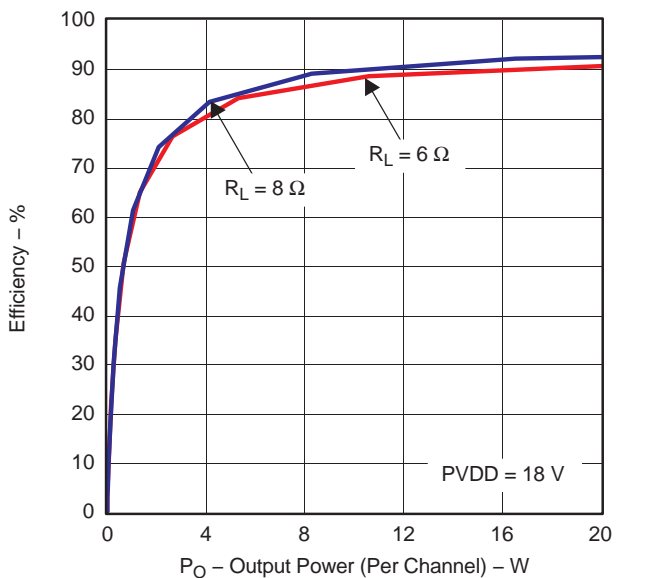


Figure 13.

**SUPPLY CURRENT  
vs  
OUTPUT POWER**

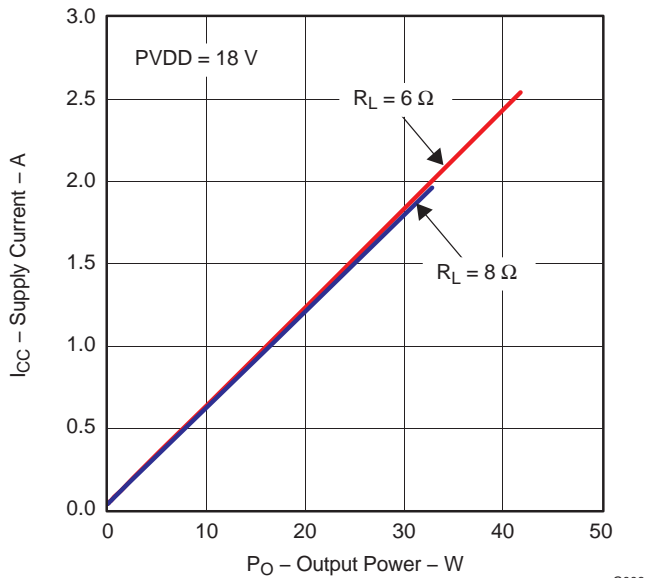


Figure 14.

**OUTPUT POWER  
vs  
SUPPLY VOLTAGE**

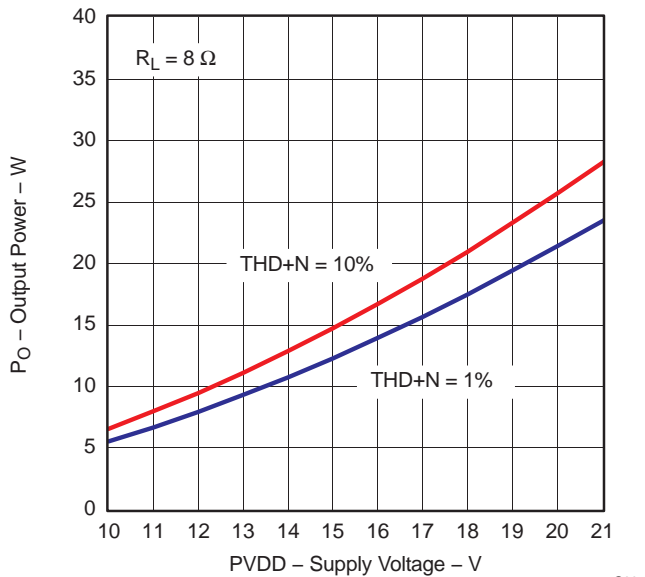


Figure 15.

**OUTPUT POWER  
vs  
SUPPLY VOLTAGE**

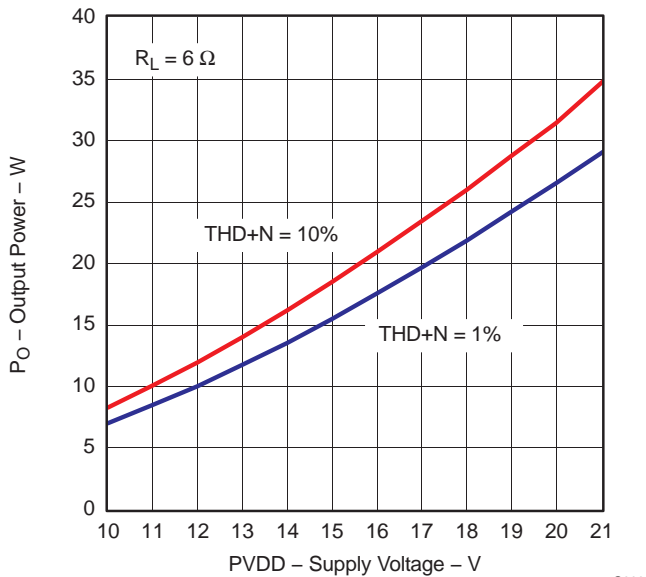


Figure 16.

## TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

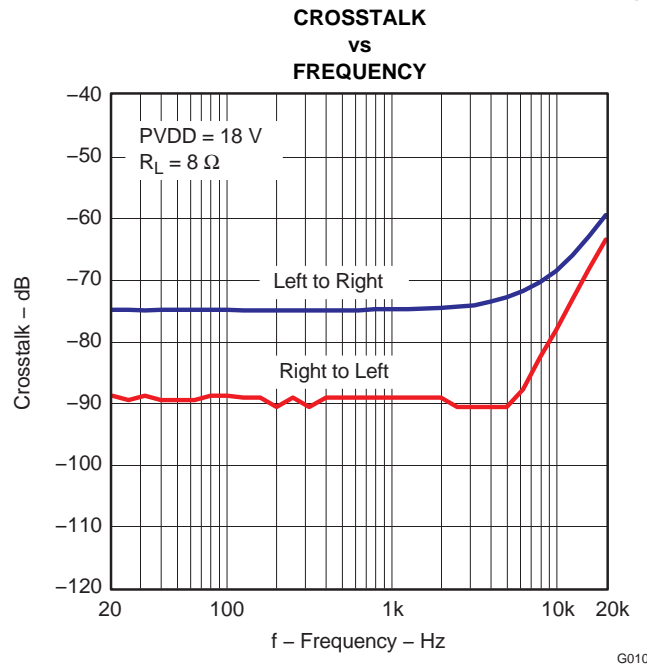


Figure 17.

## DETAILED DESCRIPTION

### POWER SUPPLY

The digital portion of the chip requires 3.3 V, and the analog portion can work with a variable range up to 12 V. PVDD has a maximum operational range up to 22 V.

To facilitate system design, the TAS5701 needs only a 12-V supply in addition to the (typical) 18-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

In order to provide outstanding electrical and acoustical characteristics, the PWM signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate gate drive supply (GVDD\_X), bootstrap pins (BST\_X), and power-stage supply pins (PVDD\_X). Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided.

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST\_X) to the power-stage output pin (OUT\_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD\_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 352 kHz to 384 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle. In an application running at a reduced switching frequency, generally 192 kHz, the bootstrap capacitor might need to be increased in value.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD\_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD\_X pin is decoupled with a 100-nF ceramic capacitor placed as close as possible to each supply pin.



The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 18-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5701 is fully protected against erroneous power-stage turnon due to parasitic gate charging.

### Clock, Auto Detection, and PLL

The TAS5701 digital audio processor (DAP) is a clock slave device. It accepts MCLK, SCLK, and LRCLK.

The TAS5701 checks to verify that SCLK is a specific value of  $32 \cdot f_s$ ,  $48 \cdot f_s$ , or  $64 \cdot f_s$ . The DAP only supports a  $1 \times f_s$  LRCLK. The timing relationship of these clocks to SDIN1 and SIN2 is shown in subsequent sections. The clock section uses MCLK or the internal oscillator clock (when MCLK is unstable or absent) to produce the internal clock.

The DAP can auto-detect and set the internal clock control logic to the appropriate settings for the frequencies of 32 kHz, normal speed (44.1 or 48 kHz), double speed (88.2 kHz or 96 kHz), and quad speed (176.4 kHz or 192 kHz).

### SERIAL DATA INTERFACE

Serial data is input on SDIN1 and SIN2. The PWM outputs are derived from SDIN1 and SIN2. The TAS5701 DAP accepts 32-, 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz serial data in 16-, 18-, 20-, or 24-bit data in left-justified, right-justified, and I<sup>2</sup>S serial data formats. See [Table 1](#) for format control settings.

SDIN1 left channel data is sent to OUTA/OUTB configured in BTL. SDIN1 right channel data is sent to OUTC/OUTD. SDIN2 left channel data is sent to SUB\_PWM+/- . The right channel data of SDIN2 is ignored.

### PWM SECTION

The DAP (digital audio processor) has three channels of high-performance digital PWM modulators that are designed to drive bridge-tied output H-bridge configurations with BD modulation.

The DAP uses noise-shaping and sophisticated error correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The DAP uses a fourth-order noise shaper to provide >100-dB SNR performance from 20 Hz to 20 kHz.

The PWM section accepts 24-bit PCM data from the DAP and outputs three PWM audio output channels. The PWM section output supports bridge-tied loads ONLY.

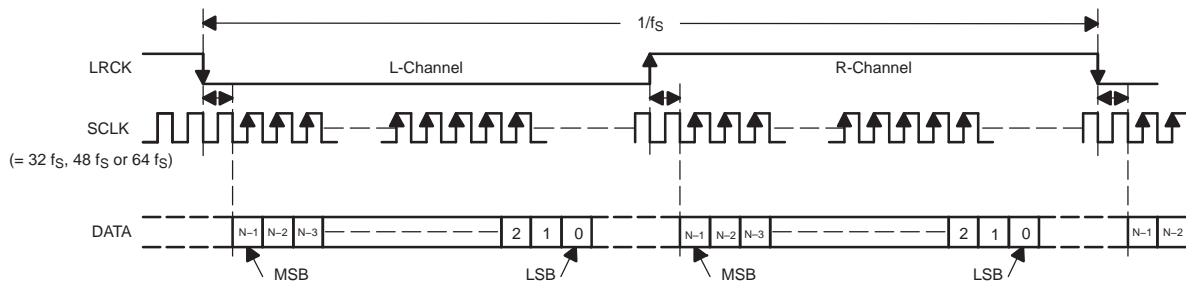
The PWM section has individual channel dc blocking filters that are ALWAYS enabled. The filter cutoff frequency is less than 1 Hz.

Finally, the PWM section has a fixed maximum modulation limit of 97.7%.

### SERIAL INTERFACE CONTROL AND TIMING

#### I<sup>2</sup>S Timing

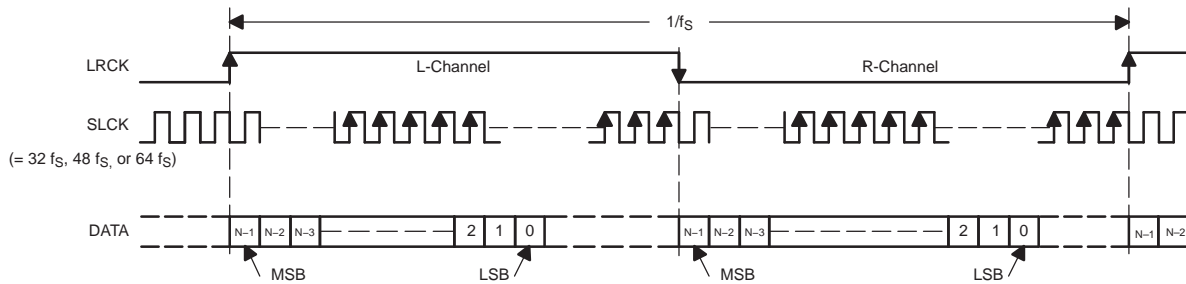
I<sup>2</sup>S timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A system clock (SCLK) running at  $32$ ,  $48$ , or  $64 \times f_s$  is used to clock in the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.



**Figure 18. I<sup>2</sup>S Format**

### Left-Justified

Left-justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at  $32, 48, \text{ or } 64 \times f_s$  is used to clock in the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.



**Figure 19. Left-Justified Format**

### Right-Justified

Right-justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at  $32, 48, \text{ or } 64 \times f_s$  is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCLK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused leading data bit positions.

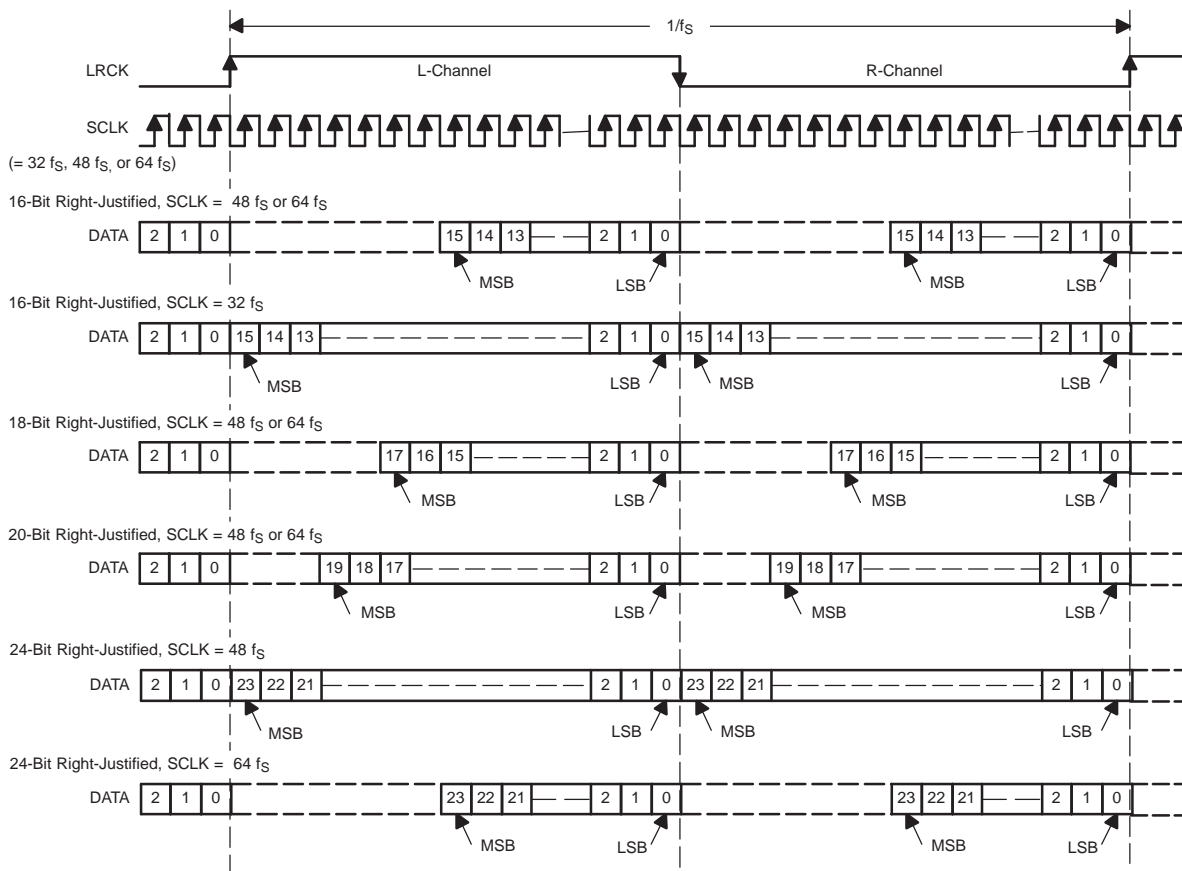


Figure 20. Right-Justified Format

### Format Control

The digital data input format is selected via three external terminals (FORMAT0, FORMAT1, and FORMAT2). Table 1 lists the corresponding data format for SDIN1 and SDIN2. LRCLK and SCLK are shared clocks for SDIN1 and SDIN2. Changes to the FORMATx terminals are latched in immediately on a rising edge of RESET. Changes to the FORMATx terminals while RESET is high are not allowed.

Table 1. Format Control

| FORMAT2 | FORMAT1 | FORMAT0 | SERIAL DIGITAL DATA FORMAT        |
|---------|---------|---------|-----------------------------------|
| 0       | 0       | 0       | 16-Bit right-justified            |
| 0       | 0       | 1       | 18-Bit right-justified            |
| 0       | 1       | 0       | 20-Bit right-justified            |
| 0       | 1       | 1       | 24-Bit right-justified            |
| 1       | 0       | 0       | 16-, 24-Bit I <sup>2</sup> S      |
| 1       | 0       | 1       | 16-, 24-Bit left-justified        |
| 1       | 1       | 0       | Reserved. Setting is not allowed. |
| 1       | 1       | 1       | Reserved. Setting is not allowed. |

### Gain Control

The gain of the DAP is selected via two external gain pins (GAIN\_0 and GAIN\_1). Table 2 lists the corresponding channel gain (for ALL channels) for GAIN\_0 and GAIN\_1 settings. Individual channel gain is not possible. Changes to the GAIN\_x terminals are latched in immediately on a rising edge of RESET. Changes to the GAIN\_x terminals while RESET is high are not allowed.

**Table 2. Gain Control**

| GAIN_1 | GAIN_0 | CHANNEL GAIN (dB) |
|--------|--------|-------------------|
| 0      | 0      | 0                 |
| 0      | 1      | 6                 |
| 1      | 0      | 12                |
| 1      | 1      | 18                |

## DEVICE PROTECTION SYSTEM

The TAS5701 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overtemperature, and undervoltage. The TAS5701 responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and reporting the error on the  $\overline{\text{FAULT}}$  pin ( $\overline{\text{FAULT}} = 0$ ); the device automatically recovers when the fault condition has been removed.

### Short-Circuit Protection

The device has independent, fast-reacting current detectors on all high-side and low-side power-stage FETs. The detector outputs are closely monitored by a protection system. If a high-current condition situation exists, i.e., the power stage outputs are shorted, the protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state and  $\overline{\text{FAULT}}$  going low. Overcurrent protection is not independent for half-bridges A and B and, respectively, C and D. That is, if the bridge-tied load between half-bridges A and B causes an overcurrent fault, half-bridges A, B, C, and D are shut down.

### Overtemperature Protection

If the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and  $\overline{\text{FAULT}}$  going low. Once the temperature decreases 30°C (typical), the device resumes normal operation.

### Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5701 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the protection circuitry and ensures that all circuits are fully operational when the VDD and GVDD\_X supply voltages reach 9.6 V (typical). Although GVDD\_x and VDD pins are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD\_x pin results in all outputs immediately being set in the high-impedance (Hi-Z) state and  $\overline{\text{FAULT}}$  pin being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

## REVISION HISTORY

### Changes from Original (June 2008) to Revision A

Page

- Replaced the with the DISSIPATION RATINGS table Thermal Information table ..... 8

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| TAS5701PAP       | ACTIVE        | HTQFP        | PAP                | 64   | 160         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  | 0 to 85      | TAS5701                  | <a href="#">Samples</a> |
| TAS5701PAPG4     | ACTIVE        | HTQFP        | PAP                | 64   | 160         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  | 0 to 85      | TAS5701                  | <a href="#">Samples</a> |
| TAS5701PAPR      | ACTIVE        | HTQFP        | PAP                | 64   | 1000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  | 0 to 85      | TAS5701                  | <a href="#">Samples</a> |
| TAS5701PAPRG4    | ACTIVE        | HTQFP        | PAP                | 64   | 1000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  | 0 to 85      | TAS5701                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TAS5701PAPR | HTQFP        | PAP             | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 1.5     | 16.0    | 24.0   | Q2            |

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TAS5701PAPR | HTQFP        | PAP             | 64   | 1000 | 367.0       | 367.0      | 45.0        |



PAP (S-PQFP-G64)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

## THERMAL PAD MECHANICAL DATA

PAP (S-PQFP-G64)

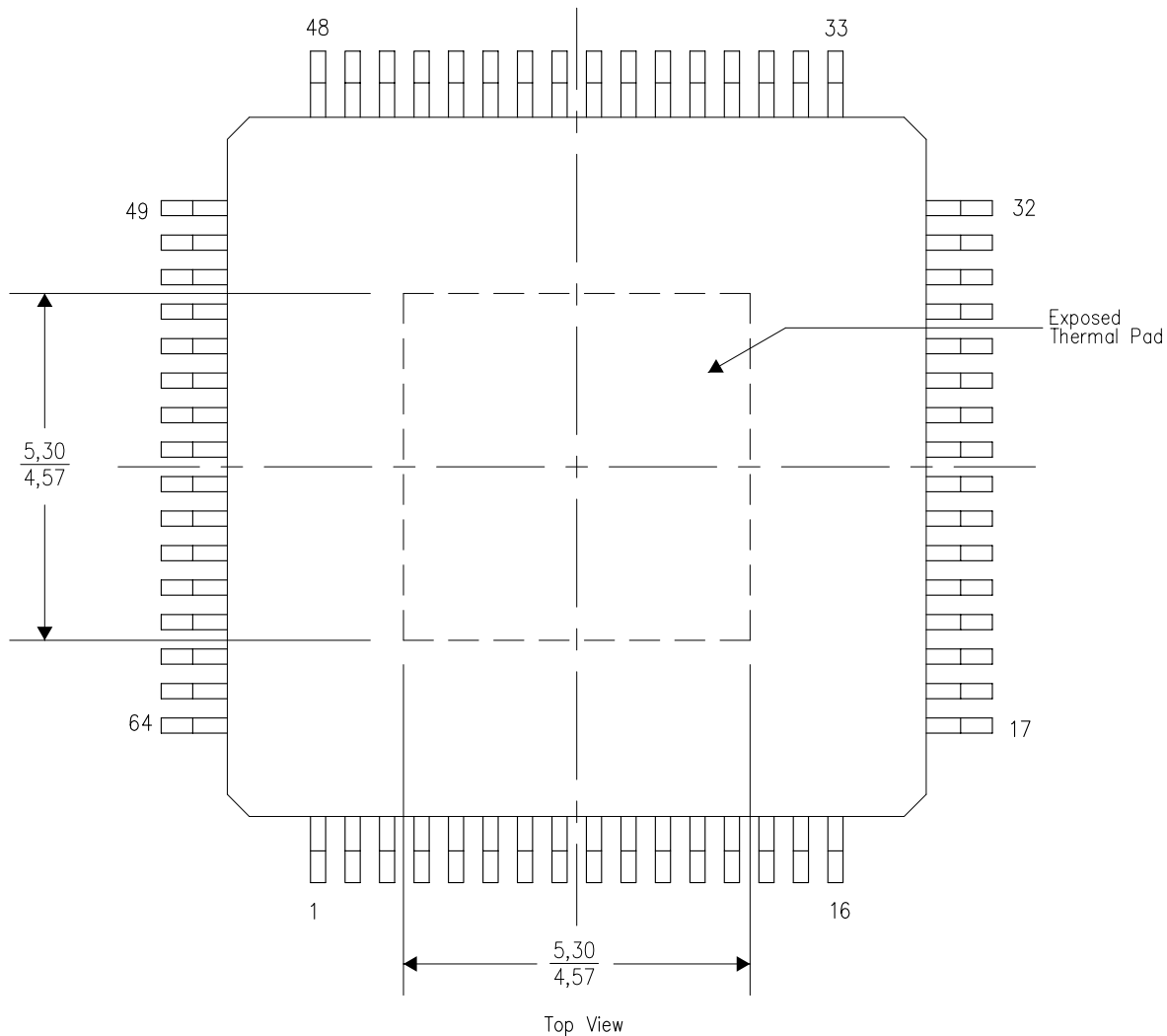
PowerPAD™ PLASTIC QUAD FLATPACK

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

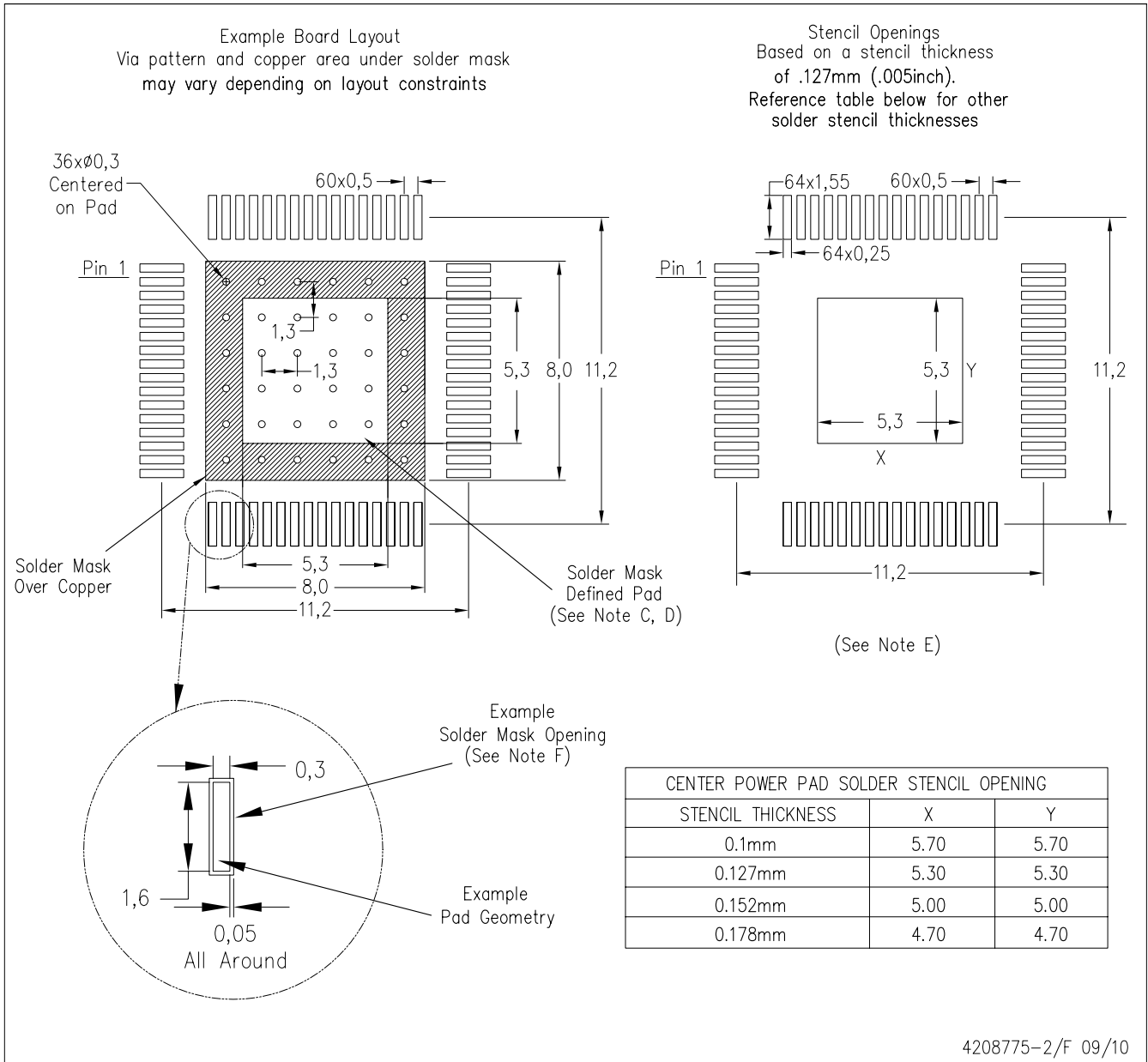
4206326-8/M 09/10

NOTES: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PAP (S-PQFP-G64)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
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|                               |  |
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