

AUDIO DSP WITH ANALOG INTERFACE

Check for Samples: [TAS3202](#)

1 Introduction

1.1 Features

- **High-Quality Audio Performance:**
102-dB Analog-to-Digital Converter (ADC)/105-dB Digital-to-Analog Converter (DAC) (Typical) DNR
- **Two Differential Stereo Analog Inputs Multiplexed to One Stereo Input ADC**
- **One Differential Stereo Output DAC**
- **Two Serial Audio Inputs (Four Channels) and Two Serial Audio Outputs (Four Channels)**
- **135-MHz Maximum Speed, >2812 Total Processing Cycles Per Sample at 48 kHz (2000 Available for Application Code)**
- **512×Fs XTAL Input in Master Mode, 512×Fs MCLK_IN in Slave Mode**
- **48-kHz Sample Rate in Clock Master Mode**
- **44.1-kHz or 48-kHz Sample Rate in Clock Slave Mode**
- **48-Bit Data Path and 28-Bit Coefficients**
- **768 Words of 48-Bit Data Memory**
- **1022 Words of 28-Bit Coefficient Memory**
- **3K Words of 55-Bit Program RAM**
- **Hardware Single-Cycle Multiplier (28×48)**
- **5.88K Words of 24-Bit Delay Memory (122.5 ms at 48 kHz)**
- **Data Formats: Left Justified, Right Justified, and I²S**
- **Two I²C Ports for Slave/Master Download**
- **Single 3.3-V Power Supply**

1.2 Applications

- **MP3 Docking Systems**
- **Digital Televisions**
- **Mini-Component Audio**

1.3 Description

The TAS3202 is an audio system-on-a-chip (SOC) designed for mini/micro systems, multimedia-speaker, and MP3 player docking systems. It includes analog interface functions: two multiplex (MUX) stereo inputs with one stereo analog-to-digital converter (ADC) and one stereo digital-to-analog converter (DAC) with analog outputs consisting of differential stereo line drivers. Four channels of serial digital audio processing are also provided. The TAS3202 has a programmable audio digital signal processor (DSP) that preserves high-quality audio by using a 48-bit data path, 28-bit filter coefficients, and a single-cycle 28×48-bit multiplier. The programmability feature allows users to customize features in the DSP RAM.

The TAS3202 is composed of eight functional blocks:

1. Analog input/mux/stereo ADC
2. Stereo DAC
3. Analog reference system
4. Power supply
5. Clocks, digital PLL, and serial data interface
6. I²C control interface
7. 8051 microcontroller
8. Audio DSP – digital audio processing



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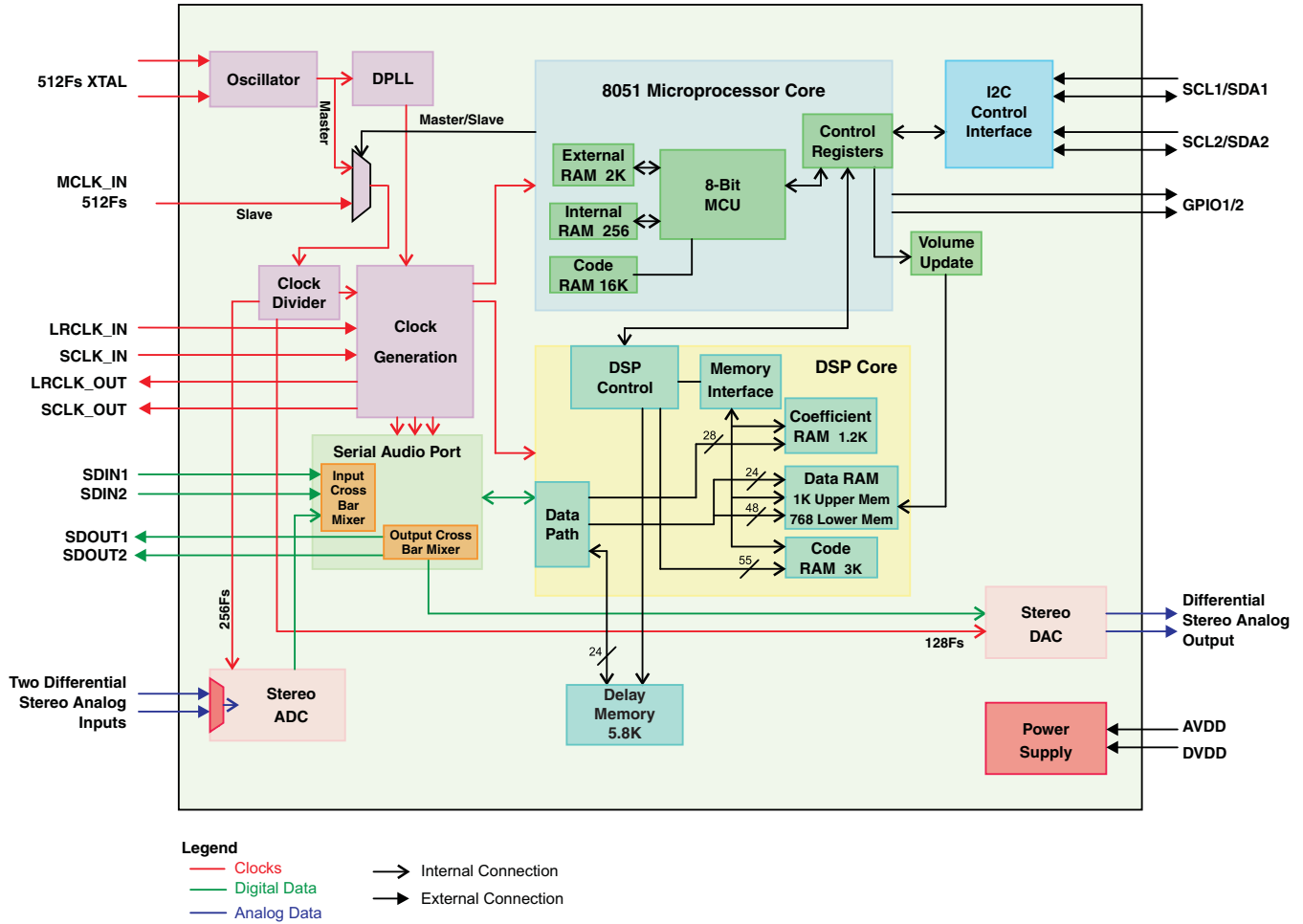


Figure 1-1. Expanded Functional Block Diagram

1.4 Ordering Information

| | |
|-------------|---|
| T_A | PLASTIC 64-PIN PQFP (PN)⁽¹⁾ |
| 0°C to 70°C | TAS3202PAG |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

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2 Functional Description

2.1 Analog Input/Mux/Stereo ADC

These modules allow two differential analog stereo inputs to be sent to one ADC to be converted to digital data. The input multiplexers include a preamplifier. This amplifier is driving the ADC, and it is digitally controlled with changes synchronized with the sample clock of the ADC. Minimal crosstalk between selected channels and unselected channels is maintained. When inputs are not needed, they are configured for minimal noise. Also included in this module is one fully differential oversampled stereo ADC. The ADC is a sigma-delta modulator with 256 times oversampling ratio. Because of the oversampling nature of the audio ADC and integrated digital decimation filter, requirements for analog anti-aliasing filtering are relaxed. Filter performance for the ADC is specified under physical characteristics.

2.2 Stereo DAC

This module includes one stereo audio DAC, which consists of a digital interpolation filter, digital sigma-delta modulator, and an analog reconstruction filter. The DAC can operate at a maximum of 48 kHz. The DAC upsamples the incoming data by 128 and performs interpolation filtering and processing on this data before conversion to a stereo analog output signal. The sigma-delta modulator always operates at a rate of 128Fs, which ensures that quantization noise generated within the modulator stays low within the frequency band below $F_s/2.4$ at all sample rates. The digital interpolation filters for interpolation from F_s to 8Fs are included in the audio DSP upper memory (reserved for analog processing), while interpolation from 8Fs to 128Fs is done in a dedicated hardware sample and hold filter. The TAS3202 includes one stereo line driver output. The line driver is capable of driving up to a 10-k Ω load. The stereo output can be in power-down mode when not used. Popless operation is achieved by conforming to start and stop sequences in the device controller code.

2.3 Analog Reference System

This module provides all internal references needed by the analog modules. It also provides bias currents for all analog blocks. External decoupling capacitors are needed along with an external 1%-tolerance resistor to set the internal bias currents. It includes a band-gap reference and several voltage buffers and a tracking current reference. The TAS3202 also uses an internally generated mid-rail supply that is used to rereference all analog inputs and is present on all analog outputs. VMID is the analog mid-rail supply and can be used when buffered externally to rereference the analog inputs and outputs. The voltage reference REXT requires a 22-k Ω 1% resistor to ground. The reference system can be powered down separately.

2.4 Power Supply

The power supply contains supply regulators that provide analog and digital regulated power for various sections of the TAS3202. Only one external 3.3-V supply is required. All other voltages are generated on chip from the external 3.3-V supply.

2.5 Clocks, Digital Phase-Locked Loop (PLL), and Serial Data Interface

These modules provide the timing and serial data interface for the TAS3202. The clocking system for the device is illustrated in Figure 2-1. The TAS3202 can be either clock master or clock slave depending on the configuration. However, clock master mode is the primary mode of operation.

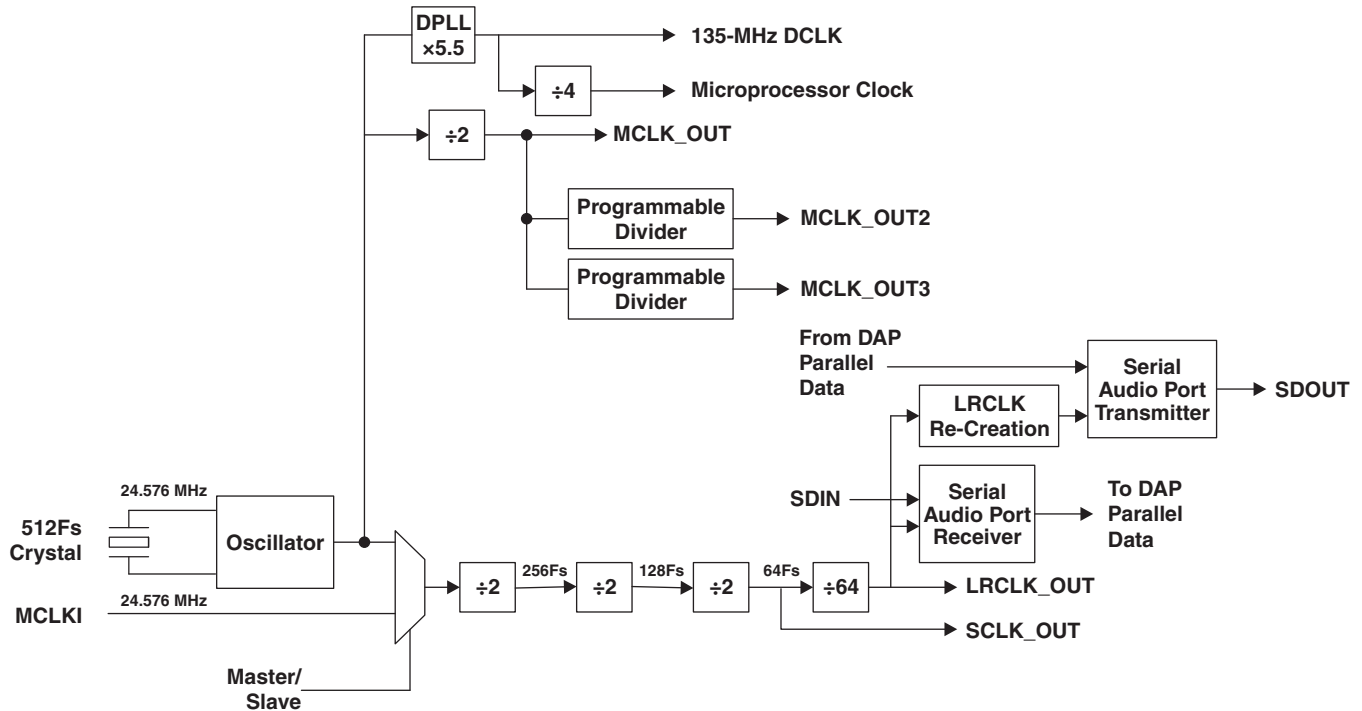


Figure 2-1. Clock Generation

DISCLAIMER: Analog performance is not ensured in slave mode, as the analog performance depends upon the quality of the MCLK_IN. The TAS3202 is not robust with respect to MCLK_IN errors (glitches, etc.); if the MCLK_IN frequency changes under operation, the device must be reset.

I²C clock master operation:

- External 512Fs crystal oscillator is used to generate all internal clocks plus all clocks for external asynchronous sampling rate converter (ASRC) output (if external ASRC is present).
- LRCLK_OUT is fixed at 48 kHz (Fs).
- SCLK_OUT is fixed at 64Fs.
- MCLK_OUT is fixed at 256Fs. In master mode, the external ASRC converts incoming serial audio data to 48-kHz sample rate synchronous to the internally generated serial audio data clocks.
- In master mode, all clocks generated for the TAS3202 are derived from the 24.576-MHz crystal. The internal oscillator drives the crystal and generates the main clock to digital PLL (DPLL), master clock outputs, 256Fs clock to the ADC, and 128Fs clock to the DAC. The DPLL generates internal clocks for the DAP and the 8051 microprocessor.

I²S clock slave operation:

- MCLK_IN (512Fs), SCLK_IN (64Fs), and LRCLK_IN (Fs) are supplied externally. Clock generation is similar to the master mode with the exception of the ADC and the DAC blocks. MCLK_IN signal is divided down and sent directly to the ADC and the DAC blocks. Therefore, audio performance depends on the MCLK_IN signal.
- DSP, MCU, and I²C clocks are still derived from external crystal oscillator.
- MCLK_OUT, SCLK_OUT, and LRCLK_OUT are passed through from clock inputs (MCLK_IN, SCLK_IN, and LRCLK_IN).
- Internal analog clocks for ADC and DACs are derived from external MCLK_IN input, so analog performance depends on MCLK_IN quality (i.e., jitter, phase noise, etc.). Degradation in analog performance is to be expected.
- Sample rate change/clock change
 - Sample rate change on the fly should be handled by the customer system controller. The TAS3202 device does not include any internal clock error or click/pop detection/management.
 - Sample rate dependent DAP filter coefficients must be uploaded by customer system controller on changing sample rate.

In I²S clock slave mode, all incoming serial audio data must be synchronous to an incoming LRCLK_IN of 44.1 kHz or 48 kHz.

2.6 I²C Control Interface

The TAS3202 has an I²C slave-only interface (SDA1 and SCL1) for receiving commands and providing status to the system controller, and a separate master I²C interface (SDA2 and SCL2) to download programs and data from external memory, such as an EEPROM. See [Section 6](#) for more information. I²C interface is not 5-V tolerant.

2.7 8051 Microcontroller

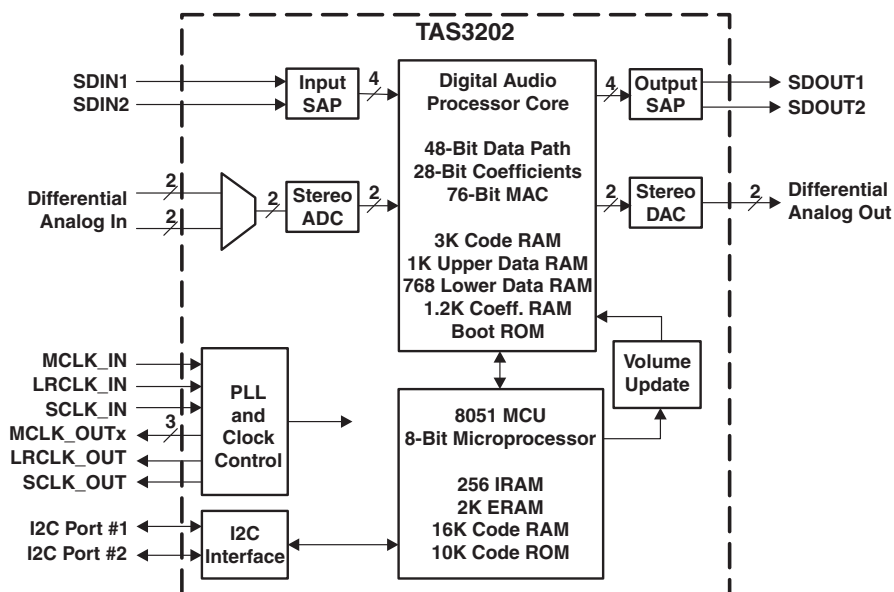
The 8051 microcontroller receives and distributes I²C write data. It retrieves and outputs data as requested from the I²C bus controller. It performs most processing tasks requiring multi-frame processing cycles. The microprocessor has its own data RAM for storing intermediate values and queuing I²C commands, a fixed boot program ROM, and a programmable RAM. The microprocessor's boot program cannot be altered. The microcontroller has specialized hardware for an I²C master and slave interface operation, volume updates, and a programmable interval-timer interrupt.

2.8 Audio Digital Signal Processor (DSP) Core

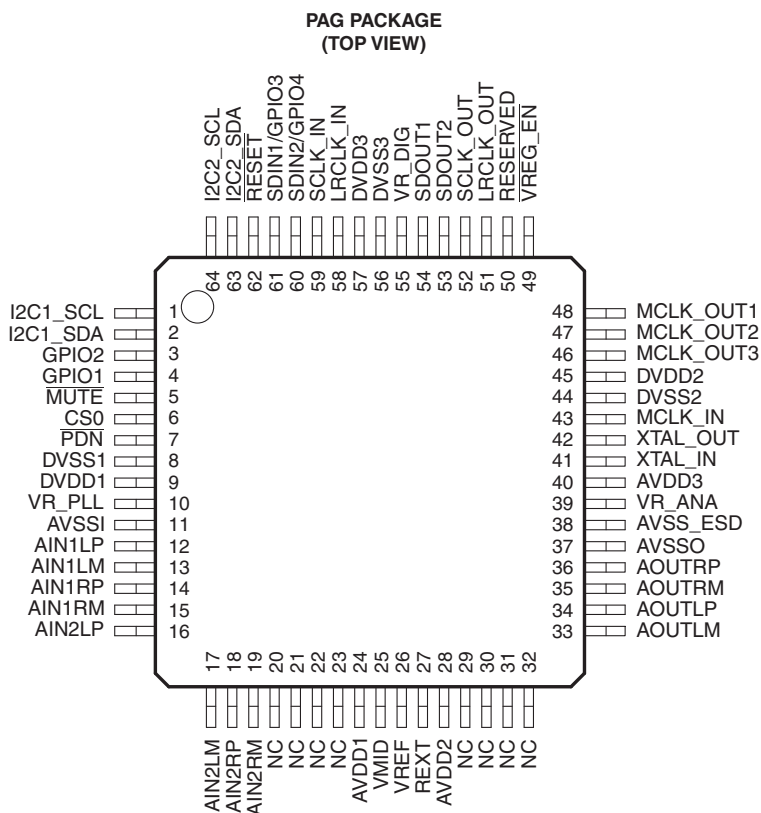
The audio DSP core arithmetic unit is a fixed-point computational engine consisting of an arithmetic unit and data and coefficient memory blocks. The audio processing structure, which can include mixers, multiplexers, volume, bass and treble, equalizers, dynamic range compression, or third-party algorithms, is running in the DAP. The 8051 microcontroller has access to digital audio processor (DAP) resources such as coefficient RAM and is able to support the DAP with certain tasks; for example, a volume ramp. The primary blocks of the audio DSP core are:

- 48-bit data path with 76-bit accumulator
- DSP controller
- Memory interface
- Coefficient RAM (1K×28)
- Data RAM – 24-bit upper memory (1K×24), 48-bit lower memory (768×48)
- Program RAM (3K×55)

3 Physical Characteristics



3.1 Terminal Assignments



NC – No internal connection

3.2 Terminal Descriptions

| TERMINAL | | INPUT/ OUTPUT ⁽¹⁾ | PULLUP/ PULLDOWN ⁽²⁾ | DESCRIPTION |
|-----------|-----|---------------------------------|------------------------------------|--|
| NAME | NO. | | | |
| AIN1LM | 13 | Analog input | Pull to VMID ⁽³⁾ | Analog input, channel 1, left, – input |
| AIN1LP | 12 | Analog input | | Analog input, channel 1, left, + input |
| AIN1RM | 15 | Analog input | Pull to VMID ⁽³⁾ | Analog input, channel 1, right, – input |
| AIN1RP | 14 | Analog input | | Analog input, channel 1, right, + input |
| AIN2LM | 17 | Analog input | Pull to VMID ⁽³⁾ | Analog input, channel 2, left, – input |
| AIN2LP | 16 | Analog input | | Analog input, channel 2, left, + input |
| AIN2RM | 19 | Analog input | Pull to VMID ⁽³⁾ | Analog input, channel 2, right, – input |
| AIN2RP | 18 | Analog input | | Analog input, channel 2, right, + input |
| AOUTLM | 33 | Analog output | | Analog output, channel 1, left, – output |
| AOUTLP | 34 | Analog output | | Analog output, channel 1, left, + output |
| AOUTRM | 35 | Analog output | | Analog output, channel 1, right, – output |
| AOUTRP | 36 | Analog output | | Analog output, channel 1, right, + output |
| AVDD1 | 24 | Power | | 3.3-V analog power supply. This pin must be decoupled according to good design practices. |
| AVSS1 | 11 | Power | | Analog supply ground |
| AVDD2 | 28 | Power | | 3.3-V analog power supply. This pin must be decoupled according to good design practices. |
| AVSS2 | 37 | Power | | Analog supply ground |
| AVDD3 | 40 | Power | | 3.3-V analog power supply. This pin must be decoupled according to good design practices. |
| AVSS3 | 38 | Power | | Analog supply ground |
| CS0 | 6 | Digital input | | I ² C Chip select |
| DVDD1 | 9 | Power | | 3.3-V digital power supply. This pin must be decoupled according to good design practices. |
| DVSS1 | 8 | Power | | Digital supply ground |
| DVDD2 | 45 | Power | | 3.3-V digital power supply. This pin must be decoupled according to good design practices. |
| DVSS2 | 44 | Power | | Digital supply ground |
| DVDD3 | 57 | Power | | 3.3-V digital power supply. This pin must be decoupled according to good design practices. |
| DVSS3 | 56 | Power | | Digital supply ground |
| GPIO1 | 4 | Digital I/O | | General-purpose input/output |
| GPIO2 | 3 | Digital I/O | | General-purpose input/output |
| I2C1_SCL | 1 | Digital I/O | | Slave I ² C serial clock input/output. Normally connected to the system microprocessor. |
| I2C1_SDA | 2 | Digital I/O | | Slave I ² C serial control data interface input/output. Normally connected to system micro. |
| I2C2_SCL | 64 | Digital output | | Master I ² C serial clock output. Normally connected to EEPROM. |
| I2C2_SDA | 63 | Digital I/O | | Master I ² C serial control data interface input/output. Normally connected to EEPROM. |
| LRCLK_IN | 58 | Digital input | Pulldown | Serial data input left/right clock for I ² S interface |
| LRCLK_OUT | 51 | Digital output | | Serial data output left/right clock for I ² S interface |
| MCLK_IN | 43 | Digital input | Pulldown | MCLK input is used in slave mode. MCLK_IN must be locked to LRCLK_IN, and the frequency is 512Fs (24.576 MHz for 48-kHz Fs). |
| MCLK_OUT1 | 48 | Digital output | | 12.288-MHz clock output. This output is valid even when reset is LOW. |

(1) I = input; O = output

(2) All pullups are 20- μ A weak pullups, and all pulldowns are 20- μ A weak pulldowns. The pullups and pulldowns are included to ensure proper input logic levels if the terminals are left unconnected (pullups \rightarrow logic 1 input; pulldowns \rightarrow logic 0 input). Devices that drive inputs with pullups must be able to sink 20 μ A while maintaining a logic-0 drive level. Devices that drive inputs with pulldowns must be able to source 20 μ A while maintaining a logic-1 drive level.

(3) Pull to VMID when analog input is in single-ended mode.

| TERMINAL | | INPUT/ OUTPUT ⁽¹⁾ | PULLUP/ PULLDOWN ⁽²⁾ | DESCRIPTION |
|------------------------------|-----------------|---------------------------------|------------------------------------|--|
| NAME | NO. | | | |
| MCLK_OUT2 | 47 | Digital output | | The frequency for this clock is 6.144 MHz/(n+1), where n is programmable in the range 0 to 255. Default value is 1.024 MHz. This output is valid even when reset is LOW. |
| MCLK_OUT3 | 46 | Digital output | | The frequency for this clock is 512 kHz/(n+1) where n is programmable in the range 0 to 255. Default value is 512 kHz. This output is valid even when reset is LOW. |
| $\overline{\text{MUTE}}$ | 5 | Digital input | Pulldown | This pin can be programmed by the application firmware to mute the TAS3202. It has no default functionality |
| NC | 20–23, 29–32 | | | No connect |
| $\overline{\text{PDN}}$ | 7 | Digital input | | This pin can be programmed by the application firmware to power down the TAS3202. Default operation is to stop the DSP. |
| RESERVED | 50 | N/A | Pulldown | Connect to ground. |
| $\overline{\text{RESET}}$ | 62 | Digital input | Pullup | System reset input, active low. A system reset is generated by applying a logic LOW to this terminal. |
| REXT | 27 | Analog output | | Requires a 22-k Ω (1%) external resistor to ground to set analog currents. Trace capacitance must be kept low. |
| SCLK_IN | 59 | Digital input | | Serial data input bit clock for I ² S interface |
| SCLK_OUT | 52 | Digital output | | Serial data output bit clock for I ² S interface |
| SDIN1/GPIO3 | 61 | Digital I/O | Pullup | Serial data input 1 for I ² S interface or programmable for GPIO #3 |
| SDIN2/GPIO4 | 60 | Digital I/O | Pullup | Serial data input 2 for I ² S interface or programmable for GPIO #4 |
| SDOUT1 | 54 | Digital output | | Serial data output 1 for I ² S interface |
| SDOUT2 | 53 | Digital output | | Serial data output 2 for I ² S interface |
| VMID | 25 | Analog output | | Analog mid supply reference. This pin must be decoupled with a 0.1- μF low-ESR capacitor and an external 10- μF filter cap. ⁽⁴⁾ |
| VR_ANA | 39 | Power | | Voltage reference for analog supply. A pinout of the internally regulated 1.8-V power. A 0.1- μF low ESR capacitor and a 4.7- μF filter capacitor must be connected between this terminal and AVSS_PLL. This terminal must not be used to power external devices. ⁽⁴⁾ |
| VR_DIG | 55 | Power | | Voltage reference for digital supply. A pinout of the internally regulated 1.8-V power. A 0.1- μF low ESR capacitor and a 4.7- μF filter capacitor must be connected between this terminal and DVSS. This terminal must not be used to power external devices. ⁽⁴⁾ |
| VR_PLL | 10 | Power | | Voltage reference for DPLL supply. A pinout of internally regulated 1.8-V power supply. A 0.1- μF low-ESR capacitor and a 4.7- μF filter capacitor must be connected between this terminal and DVSS. This terminal must not be used to power external devices. ⁽⁴⁾ |
| VREF | 26 | Analog output | | Bandgap output. A 0.1- μF low ESR capacitor should be connected between this terminal and AVSS_PLL. This terminal must not be used to power external devices. ⁽⁴⁾ |
| $\overline{\text{VREG_EN}}$ | 49 | Digital input | | Voltage regulator enable. When enabled LOW, this input causes the power-supply regulators to be enabled. |
| XTAL_IN | 41 | Digital input | | Crystal input. A 24.576-MHz (512Fs) crystal should be used. |
| XTAL_OUT | 42 | Digital output | | Crystal output |

(4) If desired, low ESR capacitance values can be implemented by paralleling two or more ceramic capacitors of equal value. Paralleling capacitors of equal value provide an extended high-frequency supply decoupling.

3.3 Reset ($\overline{\text{RESET}}$) Power-Up Sequence

The $\overline{\text{RESET}}$ pin is an asynchronous control signal that restores all TAS3202 components to the default configuration. When a reset occurs, the audio DSP core is put into an idle state and the 8051 starts initialization. A valid XTAL_IN must be present when clearing the $\overline{\text{RESET}}$ pin to initiate a device reset. A reset can be initiated by applying a logic 0 on $\overline{\text{RESET}}$.

As long as $\overline{\text{RESET}}$ is held LOW, the device is in the reset state. During reset, all I²C and serial data bus operations are ignored. The I²C interface SCL and SDA lines go into a high-impedance state and remain in that state until device initialization has completed.

The rising edge of the reset pulse begins the initialization housekeeping functions of clearing memory and setting the default register values. Once these are complete, the TAS3202 enables its master I²C interface and disables its slave I²C interface.

Using the master interface, the TAS3202 automatically tests to see if an external I²C EEPROM is at address 1010x. The value x can be chip selects, other information, or don't care, depending on the EEPROM selected.

If a memory is present and it contains the correct header information and one or more blocks of program/memory data, the TAS3202 begins to load the program, coefficient and/or data memories from the external EEPROM. If an external EEPROM is present, the download is considered complete when an end-of-program header is read by the TAS3202. At this point, the TAS3202 disables the master I²C interface, enables the slave I²C interface, and starts normal operation. After a successful download, the micro program counter is reset, and the downloaded micro and DAP application firmware controls execution.

If no external EEPROM is present or if an error occurs during the EEPROM read, TAS3202 disables the master I²C interface, enables the slave I²C interface, and proceeds to boot the device according to the ROM. In this default ROM configuration, the TAS3202 streams audio from input to output if the GPIO1 pin is asserted logic low on reset; if the GPIO1 pin is asserted logic high, the ADC and the DAC are muted.

NOTE

The master and slave I²C interfaces do not operate simultaneously.

3.4 Voltage Regulator Enable ($\overline{\text{VREG_EN}}$)

Setting the $\overline{\text{VREG_EN}}$ high shuts down all voltage regulators in the device. Internal register settings are lost in this power-down mode. A full power-up/reset/program-load sequence must be completed before the device is operational.

3.5 Power-On Reset ($\overline{\text{RESET}}$)

On power up, it is recommended that the TAS3202 $\overline{\text{RESET}}$ be held low until DVDD has reached 3.3 V. This can be done by programming the system controller or by using an external RC delay circuit. The 1-k Ω and 1- μ F values provide a delay of approximately 200 μ s. The values of R and C can be adjusted to provide other delay values as necessary.

3.6 Power Down ($\overline{\text{PDN}}$)

The TAS3202 supports a number of power-down modes.

$\overline{\text{PDN}}$ can be used to put the device into power-saving standby mode. In the default ROM configuration, applying a logic low on this pin stops all clocks, powers down all analog circuitry, and ramps down volume for all digital inputs. This mode is used to minimize power consumption while preserving register settings. If the TAS3202 is successfully booted from an external EEPROM, the functionality of the pin is defined by the user's application firmware.

Individual power down DAC and ADC – Both the DAC and the ADC can be powered down individually. This feature is made available to the board controller via the I²C interface.

Power down of analog reference – The analog reference can be powered down if all DAC and ADCs are powered down. This feature is made available to the board controller via the I²C interface.

3.7 I²C Chip Select (CS0)

The TAS3202 has a control to specify the slave and master I²C address. This control permits up to two TAS3202 devices to be placed in a system without external logic. GPIO pins are level sensitive. They are not edge triggered.

See [Section 6.3](#) for a complete description of this pin.

3.8 Programmable General-Purpose I/O (GPIO)

The TAS3202 has four general purpose input/output pins that can be programmed by the user's application firmware.

GPIO1 and GPIO2 pins are single-function I/O pins. Upon power up, GPIO1 is an input. If there is an unsuccessful boot from an external EEPROM and GPIO1 is pulled high externally, the DAC output is disabled. If there is an unsuccessful boot from an external EEPROM and GPIO1 is pulled low externally, the DAC output is enabled. If there is a successful boot from an external EEPROM, GPIO1 will be configured as an output and be driven logic low by the TAS3202 when the user's application code is running.

GPIO3 and GPIO4 are dual function I/O pins. The functionality of GPIO pins must be defined by the user's application code.

Mute and power-down functions have to be programmed in the EEPROM application code. These are general-purpose input pins and are suggested for Mute and Powerdown functions. However, these settings must be defined by the user's application code.

3.8.1 GPIO Pin Function After Device is Programmed

Once the TAS3202 has been programmed, either through a successful boot load or via slave I²C download, the operation of GPIO is defined by the user's application code.

3.9 Input and Output Serial Audio Ports

Serial data is input on SDINx on the TAS3202, allowing up to four channels of digital audio input. The TAS3202 supports serial data in 16-, 20-, or 24-bit data in left, right, and I²S serial data formats. The parameters for the clock and serial data interface input formats are I²C configurable.

Serial data is output on SDOUTx, allowing up to four channels of digital audio output. SDOUTx port supports the same formats as the SDINx port. Output data rate is the same data rate as the input. The SDOUTx output uses the SCLK_OUT and LRCLK_OUT signals to provide synchronization.

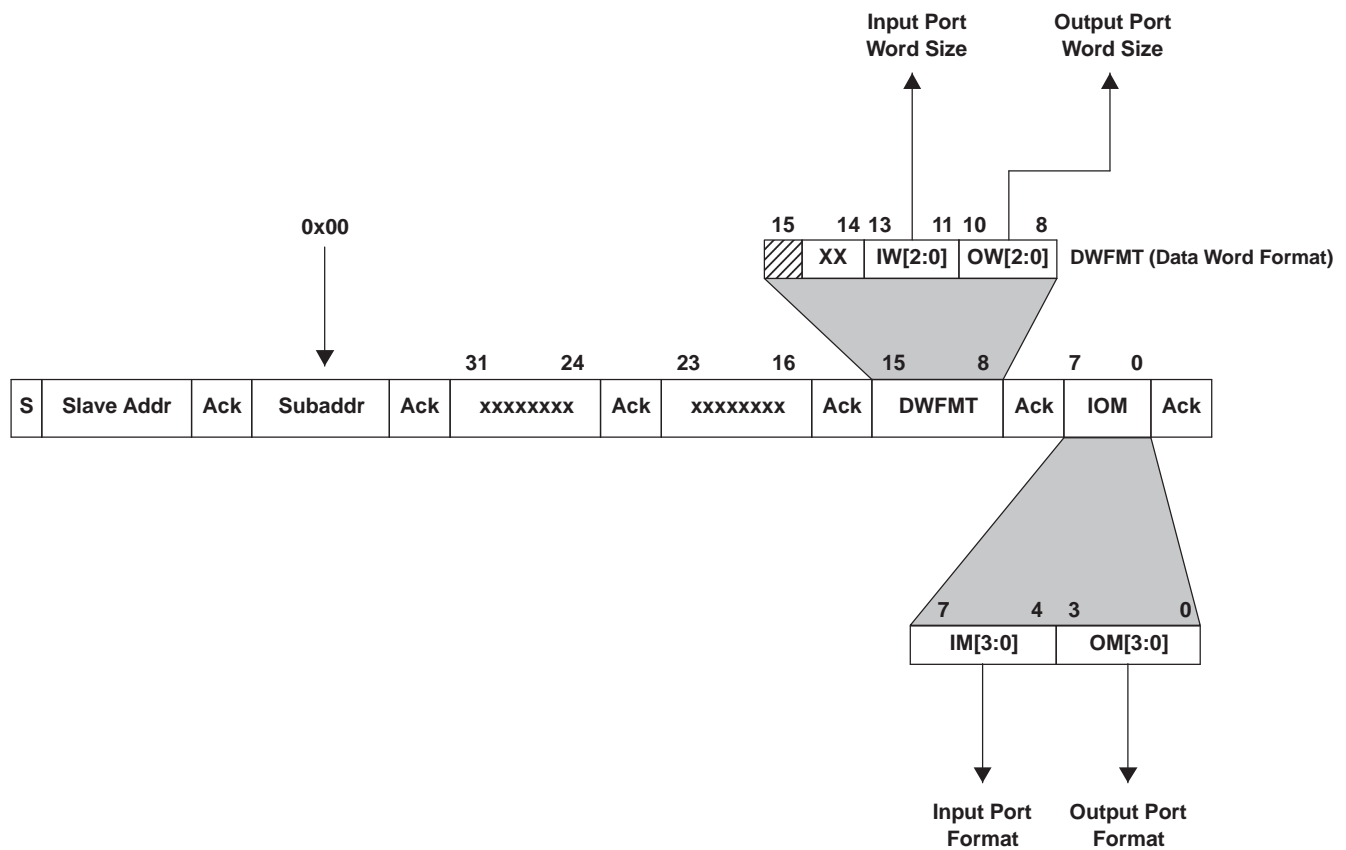
The TAS3202 supported data formats are listed in [Table 3-1](#).

Table 3-1. Supported Data Formats

| INPUT SAP (SDIN) | OUTPUT SAP (SDOUT) |
|----------------------------|----------------------------|
| 2-channel I ² S | 2-channel I ² S |
| 2-channel left-justified | 2-channel left-justified |
| 2-channel right-justified | 2-channel right-justified |

Table 3-2. Serial Data Input and Output Formats

| MODE | INPUT CONTROL IM[3:0] | OUTPUT CONTROL OM[3:0] | SERIAL FORMAT | WORD LENGTHS | DATA RATES (kHz) | MAXIMUM SCLK (MHz) |
|-----------|-----------------------|------------------------|------------------|--------------|------------------|--------------------|
| 2-channel | 0000 | 0000 | Left-justified | 16, 20, 24 | 32–48 | 3.072 |
| | 0001 | 0001 | Right-justified | 16, 20, 24 | | |
| | 0010 | 0010 | I ² S | 16, 20, 24 | | |



R0003-01

Figure 3-1. Serial Data Controls

Table 3-3. Serial Data Input and Output Data Word Sizes

| IW1, OW1 | IW0, OW0 | FORMAT |
|----------|----------|-------------|
| 0 | 0 | Reserved |
| 0 | 1 | 16-bit data |
| 1 | 0 | 20-bit data |
| 1 | 1 | 24-bit data |

Following a reset, ensure that the clock register (0x00) is written before performing volume, treble, or bass updates.

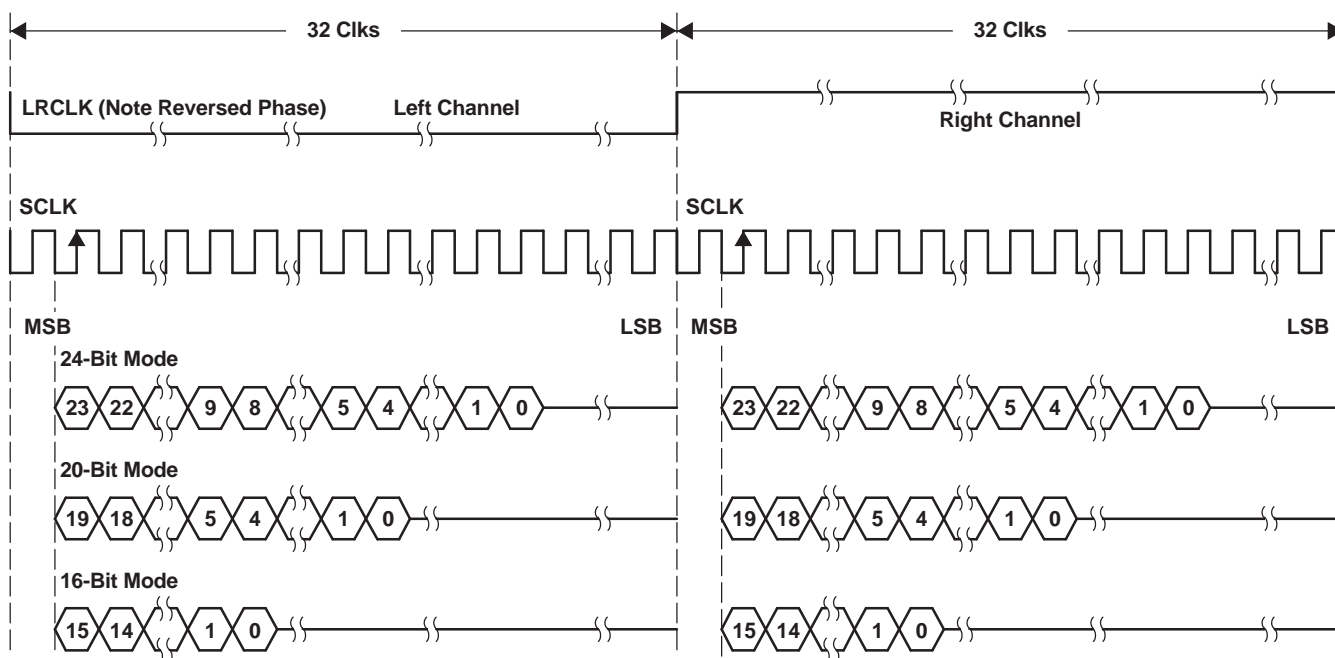
Commands to reconfigure the SAP can be accompanied by mute and unmute commands for quiet operation. However, care must be taken to ensure that the mute command has completed before the SAP is commanded to reconfigure. Similarly, the TAS3202 should not be commanded to unmute until after the SAP has completed a reconfiguration. The reason for this is that an SAP configuration change while a volume or bass or treble update is taking place can cause the update not to be completed properly.

When the TAS3202 is transmitting serial data, it uses the negative edge of SCLK to output a new data bit. The TAS3202 samples incoming serial data on the rising edge of SCLK.

3.9.1 2-Channel I²S Timing

In 2-channel I²S timing, LRCLK is LOW when left-channel data is transmitted and HIGH when right-channel data is transmitted. SCLK is a bit clock running at $64 \times f_s$ and clocks in each bit of the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written most-significant bit (MSB) first and is valid on the rising edge of the bit clock. The TAS3202 masks unused trailing data-bit positions.

2-Channel I²S (Philips Format) Stereo Input/Output



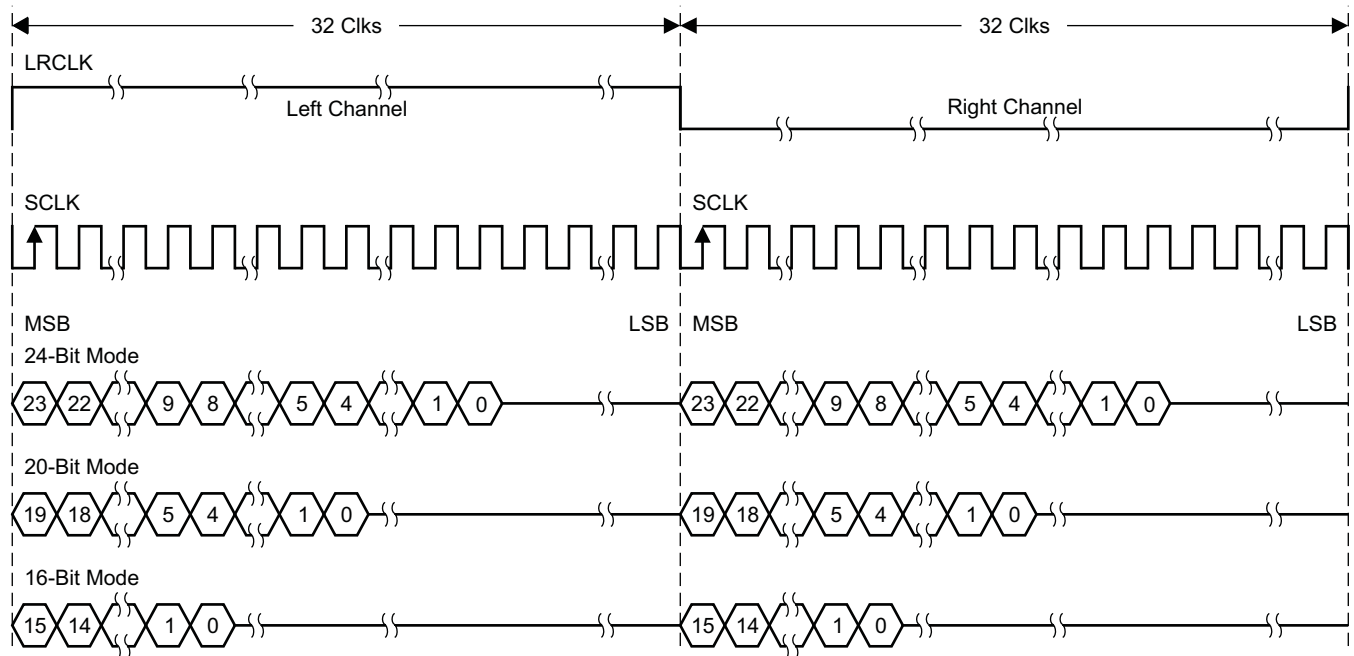
T0034-04

Figure 3-2. I²S 64f_s Format

3.9.2 2-Channel Left-Justified Timing

In 2-channel left-justified timing, LRCLK is HIGH when left-channel data is transmitted and LOW when right-channel data is transmitted. SCLK is a bit clock running at $64 \times f_s$, which clocks in each bit of the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The TAS3202 masks unused trailing data-bit positions.

2-Channel Left-Justified Stereo Input



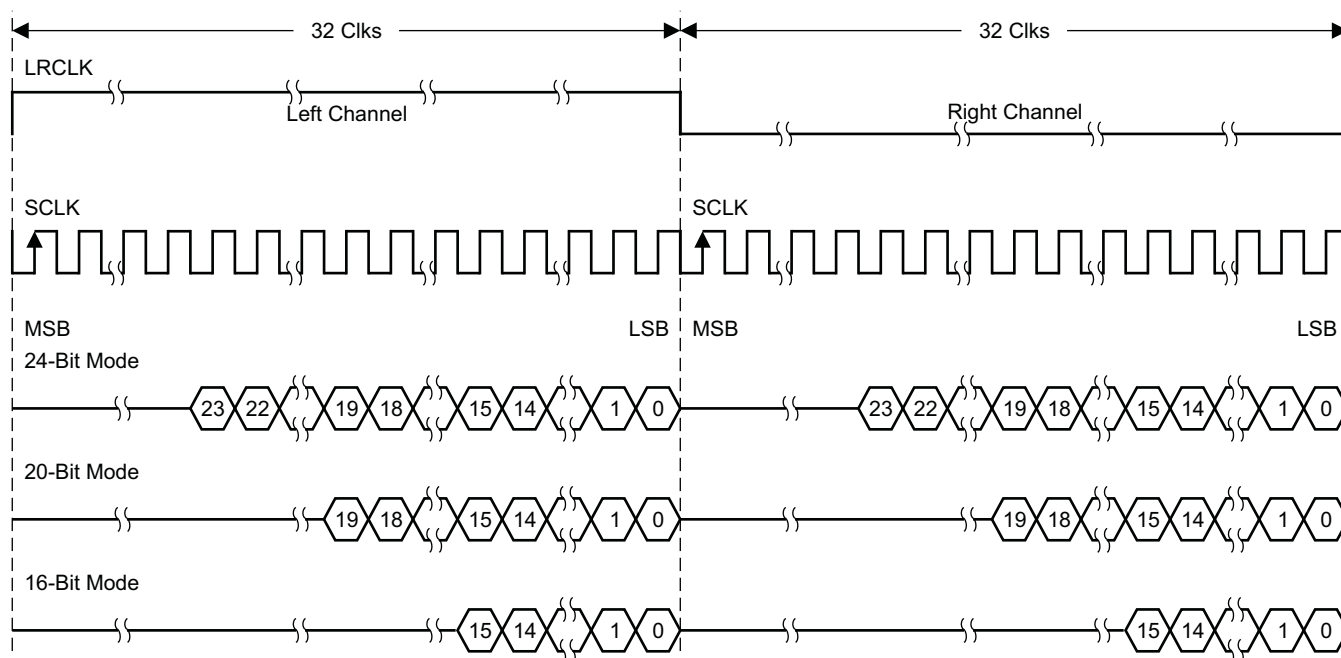
T0034-02

Figure 3-3. Left-Justified $64f_s$ Format

3.9.3 2-Channel Right-Justified Timing

In 2-channel right-justified (RJ) timing, LRCLK is HIGH when left-channel data is transmitted and LOW when right-channel data is transmitted. SCLK is a bit clock running at $64 \times f_s$ which clocks in each bit of the data. The first bit of data appears on the data lines eight bit-clock periods (for 24-bit data) after LRCLK toggles. In the RJ mode, the last bit clock before LRCLK transitions always clocks the least-significant bit (LSB) of data. The data is written MSB first and is valid on the rising edge of the bit clock. The TAS3202 masks unused leading data-bit positions.

2-Channel Right-Justified (Sony Format) Stereo Input



T0034-03

Figure 3-4. Right-Justified $64f_s$ Format

3.9.4 SAP Input to SAP Output—Processing Flow

All SAP data format options other than I²S result in a two-sample delay from input to output. If I²S formatting is used for both the input SAP and the output SAP, the polarity of RCLK must be inverted. However, if I²S format conversions are performed between input and output, the delay becomes either 1.5 samples or 2.5 samples, depending on the processing clock frequency selected for the audio DSP core relative to the sample rate of the incoming data.

The I²S format uses the falling edge of LRCLK to begin a sample period, whereas all other formats use the rising edge of LRCLK to begin a sample period. This means that the input SAP and audio DSP core operate on sample windows that are 180° out of phase with respect to the sample window used by the output SAP. This phase difference results in the output SAP outputting a new data sample at the midpoint of the sample period used by the audio DSP core to process the data. If the processing cycle completes all processing tasks before the midpoint of the processing sample period, the output SAP outputs this processed data. However, if the processing time extends past the midpoint of the processing sample period, the output SAP outputs the data processed during the previous processing sample period. In the former case, the delay from input to output is 1.5 samples. In the latter case, the delay from input to output is 2.5 samples.

The delay from input to output can thus be either 1.5 or 2.5 sample times when data format conversions are performed that involve the I²S format. However, which delay time is obtained for a particular application is determinable and fixed for that application, providing care is taken in the selection of MCLK_IN/XTAL_IN with respect to the incoming sample clock, LRCLK.

4 Algorithm and Software Development Tools for TAS3202

The TAS3202 algorithm and software development tool set is a combination of classical development tools and graphical development tools. The tool set is used to build, debug, and execute programs in the audio DSP section of the TAS3202.

Classical development tooling includes text editors, compilers, assemblers, simulators, and source-level debuggers. The 8051 can be programmed exclusively in ANSI C.

The 8051 tool set is a commercially off-the-shelf (COTS) tool set, with modifications as specified in this document. The 8051 tool set is a complete environment with an IDE, editor, compiler, debugger, and simulator.

The audio DSP core is programmed exclusively in assembly. The audio DSP tool set is a complete environment with an IDE, context-sensitive editor, assembler, and simulator/debugger.

Graphical development tooling provides a means of programming the audio DSP core through a graphical drag-and-drop interface using modular audio software components from a component library. The graphical tooling produces audio DSP assembly. The classical tools can also be used to produce the executable code.

5 Clock Controls

Clock management for the TAS3202 consists of two control structures:

- Master clock management
 - Oversees the selection of the clock frequencies for the 8051 microprocessor, the I²C controller, and the audio DSP core
 - The master clock (MCLK_IN or XTAL_IN) is the source for these clocks.
 - In most applications, the master clock drives an on-chip digital phase-locked loop (DPLL), and the DPLL output drives the microprocessor and audio DSP clocks.
 - Also available is the DPLL bypass mode, in which the high-speed master clock directly drives the microprocessor and audio DSP clocks.
- Serial audio port (SAP) clock management
 - Oversees SAP master/slave mode
 - Controls output of SCLKOUT, and LRCLK in the SAP master mode

Input pin MCLK_IN or XTAL_IN provides the master clock for the TAS3202. Within the TAS3202, these two inputs are combined by an OR gate and, thus, only one of these two sources can be active at any one time. The source that is not active must be logic 0.

The TAS3202 only supports dynamic sample-rate changes between any of the supported sample frequencies when a fixed-frequency master clock is provided. During dynamic sample-rate changes, the TAS3202 remains in normal operation and the register contents are preserved. To avoid producing audio artifacts during the sample-rate changes, a volume or mute control can be included in the application firmware that mutes the output signal during the sample-rate change. The fixed-frequency clock can be provided by a crystal attached to XTAL_IN and XTAL_OUT or an external 3.3-V fixed-frequency TTL source attached to MCLK_IN.

When the TAS3202 is used in a system in which the master clock frequency (f_{MCLK}) can change, the TAS3202 must be reset during the frequency change. In these cases, the procedure shown in [Figure 5-1](#) should be used.

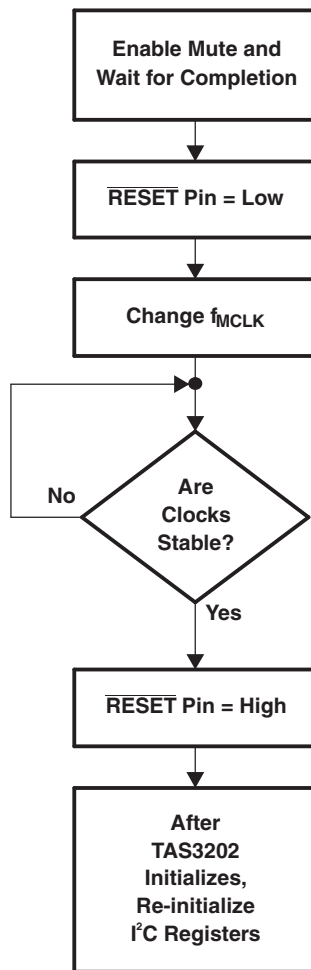


Figure 5-1. Master Clock Frequency (f_{MCLK}) Change Procedure

When the serial audio port (SAP) is in the master mode, the SAP uses the XTAL_IN master clock to drive the serial port clocks SCLK_OUT and LRCLK. When the SAP is in the slave mode, MCLK_IN, SCLK_IN, and LRCLK_IN are input clocks. SCLK_OUT and LRCLK_OUT are derived from SCLK_IN and LRCLK_IN, respectively.

See *Clock Register (0x00)*, [Section 9.1](#), for information on programming the clock register.

Table 5-1. TAS3202 MCLK and LRCLK Common Values (MCLK = 24.576 MHz or MCLK = 22.579 MHz)

| F_s SAMPLE RATE (kHz) | CH PER SDIN | MCLK/ LRCLK RATIO ($\times f_s$) | MCLK FREQ (MHz) | SCLKIN RATE ($\times f_s$) | SCLK_IN FREQ (MHz) | SCLK_OUT RATE ($\times f_s$) | CH PER SDOUT | LRCLK (F_s) | PLL MULTIPLI ER | F_{DSPCLK} (MHz) | f_{DSPCLK}/f_s |
|---|----------------|---|-----------------------|------------------------------------|--------------------------|--------------------------------------|-----------------|--------------------|-----------------------|-----------------------|------------------|
| Slave Mode, 2 Channels In, 2 Channels Out | | | | | | | | | | | |
| 44.1 | 2 | 512 | 22.579 | 64 | 2.822 | 64 | 2 | 64 | 5.5 | 124.2 | 2816 |
| 48 | 2 | 256 | 24.576 | 64 | 3.072 | 64 | 2 | 64 | 5.5 | 135.2 | 2816 |
| Master Mode, 2 Channels In, 2 Channels Out | | | | | | | | | | | |
| 48 | 2 | 256 | 24.576 | N/A | N/A | 64 | 2 | 64 | 5.5 | 135.2 | 2816 |

6 Microprocessor Controller

The 8051 microprocessor receives and distributes I²C write data, retrieves and outputs to the I²C bus controllers the required I²C read data, and participates in most processing tasks requiring multiframe processing cycles. The microprocessor has its own data RAM for storing intermediate values and queuing I²C commands, a fixed boot-program ROM, and a program RAM. The microprocessor boot program cannot be altered. The microprocessor controller has specialized hardware for I²C master and slave interface operation, volume updates, and a programmable interval timer interrupt.

The TAS3202 has a slave-only I²C interface that is compatible with the Inter IC (I²C) bus protocol and supports both 100-kbps and 400-kbps data-transfer rates for multiple 4-byte write and read operations (maximum is 20 bytes). The slave I²C control interface is used to program the registers of the device and to read device status.

The TAS3202 also has a master-only I²C interface that is compatible with the I²C bus protocol and supports 375-kbps data transfer rates for multiple 4-byte write and read operations (maximum is 20 bytes). The master I²C interface is used to load program and data from an external I²C EEPROM.

Once the microprocessor program memory has been loaded, it cannot be updated until the TAS3202 has been reset.

The master and slave I²C ports do not operate simultaneously.

When acting as an I²C master, the data transfer rate is fixed at 375 kHz, assuming MCLK_IN or XTAL_IN = 24.576 MHz.

When acting as an I²C slave, the data transfer rate is determined by the I²C master device on the bus.

The I²C communication protocol for the I²C slave mode is shown in Figure 6-1.

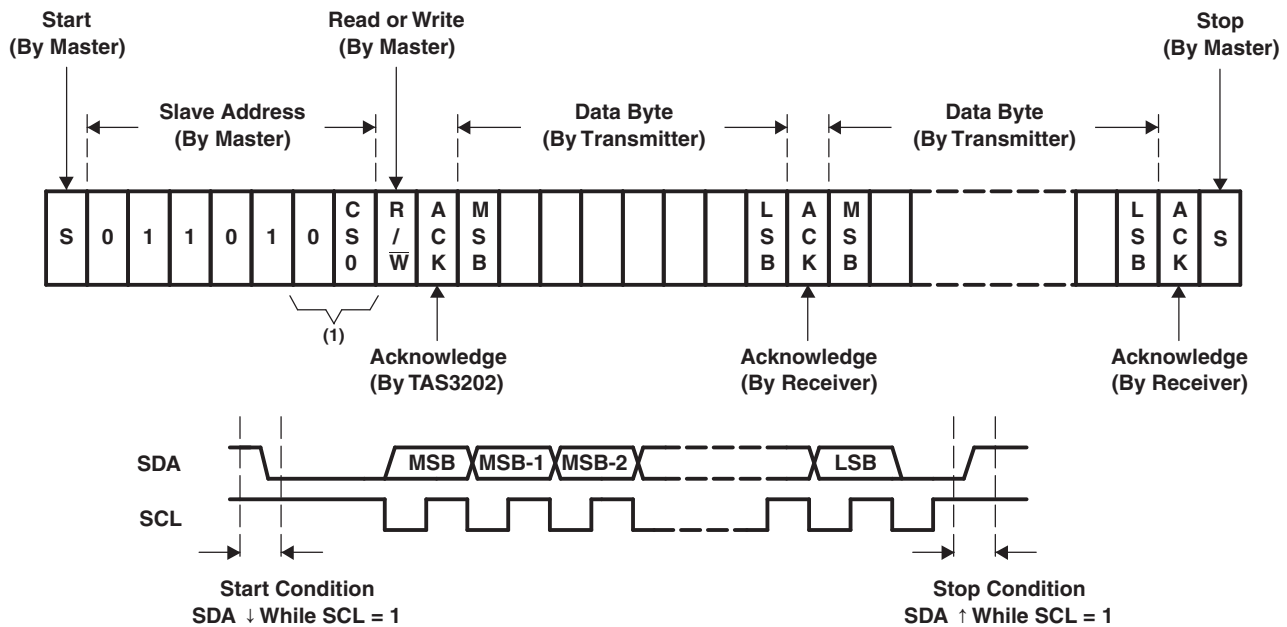


Figure 6-1. I²C Slave-Mode Communication Protocol

6.1 8051 Microprocessor Addressing Mode

The 256 bytes of internal data memory address space is accessible using indirect addressing instructions (including stack operations). However, only the lower 128 bytes are accessible using direct addressing. The upper 128 bytes of direct address Data Memory space are used to access Extended Special Function Registers (ESFRs).

6.1.1 Register Banks

There are four directly addressable register banks, only one of which may be selected at one time. The register banks occupy Internal Data Memory addresses from 00 hex to 1F hex.

6.1.2 Bit Addressing

The 16 bytes of Internal Data Memory that occupy addresses from 20 hex to 2F hex are bit addressable. SFRs that have addresses of the form 1XXXX000 binary are also bit addressable.

6.1.3 External Data Memory

External data memory occupies a 2K × 8 address space. This space contains the ESFRs. The ESFRs permit access and control of the hardware features and internal interfaces of the TAS3202.

6.1.4 Extended Special Function Registers (ESFRs)

ESFRs provide signals needed for the M8051 to control the different blocks in the device. ESFR is an extension to the M8051. Figure 6-2 shows how these registers are arranged.

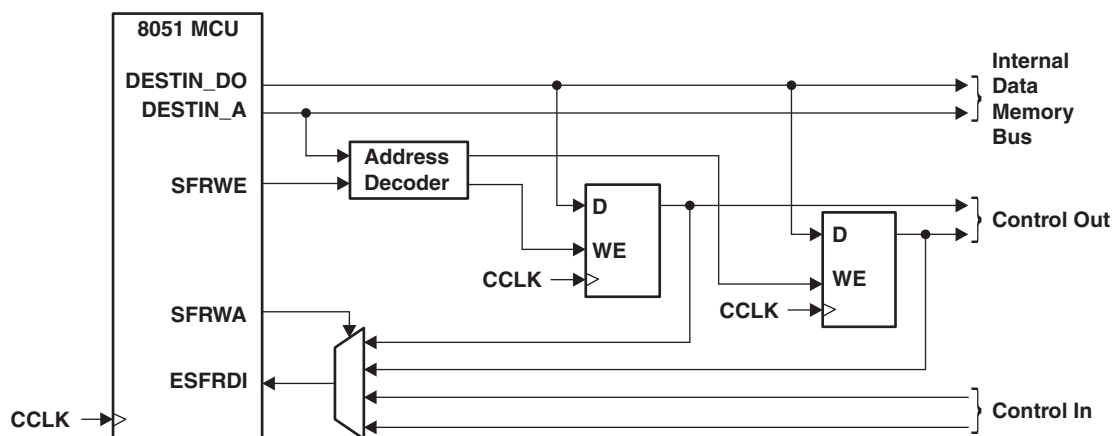


Figure 6-2. ESFRs

6.1.5 Memory-Mapped Registers for DAP Data Memory

The following memory mapped registers are used for communication with the DAP.

Table 6-1. Memory-Mapped Registers

| ADDRESS | REGISTER | COMMENT |
|---------|-------------|--------------------------------------|
| 0x0300 | Dither Seed | Sets the dither seed value |
| 0x0301 | PC Start | Sets the starting address of the DAP |
| 0x0302 | Reserved | Reserved |

NOTE

TAS3202 has the same memory mapped registers distinction of upper and lower memory for these registers.

6.2 General I²C Operations

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. The address and data are transferred in byte (8-bit) format with the MSB transferred first. In addition, each byte transferred on the

bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is HIGH to indicate a start and stop conditions. A HIGH-to-LOW transition on SDA indicates a start, and a LOW-to-HIGH transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The slave holds SDA LOW during acknowledge clock period to indicate an acknowledgement. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (one byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the HIGH level for the bus.

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. Figure 6-3 shows the TAS3202 read and write operation sequences.

As shown in Figure 6-3, an I²C read transaction requires that the master device first issue a write transaction to give the TAS3202 the subaddress to be used in the read transaction that follows. This subaddress assignment write transaction is then followed by the read transaction. For write transactions, the subaddress is supplied in the first byte of data written, and this byte is followed by the data to be written. For I²C write transactions, the subaddress must always be included in the data written. There cannot be a separate write transaction to supply the subaddress, as was required for read transactions. If a subaddress-assignment-only write transaction is followed by a second write transaction supplying the data, erroneous behavior results. The first byte in the second write transaction is interpreted by the TAS3202 as another subaddress replacing the one previously written.

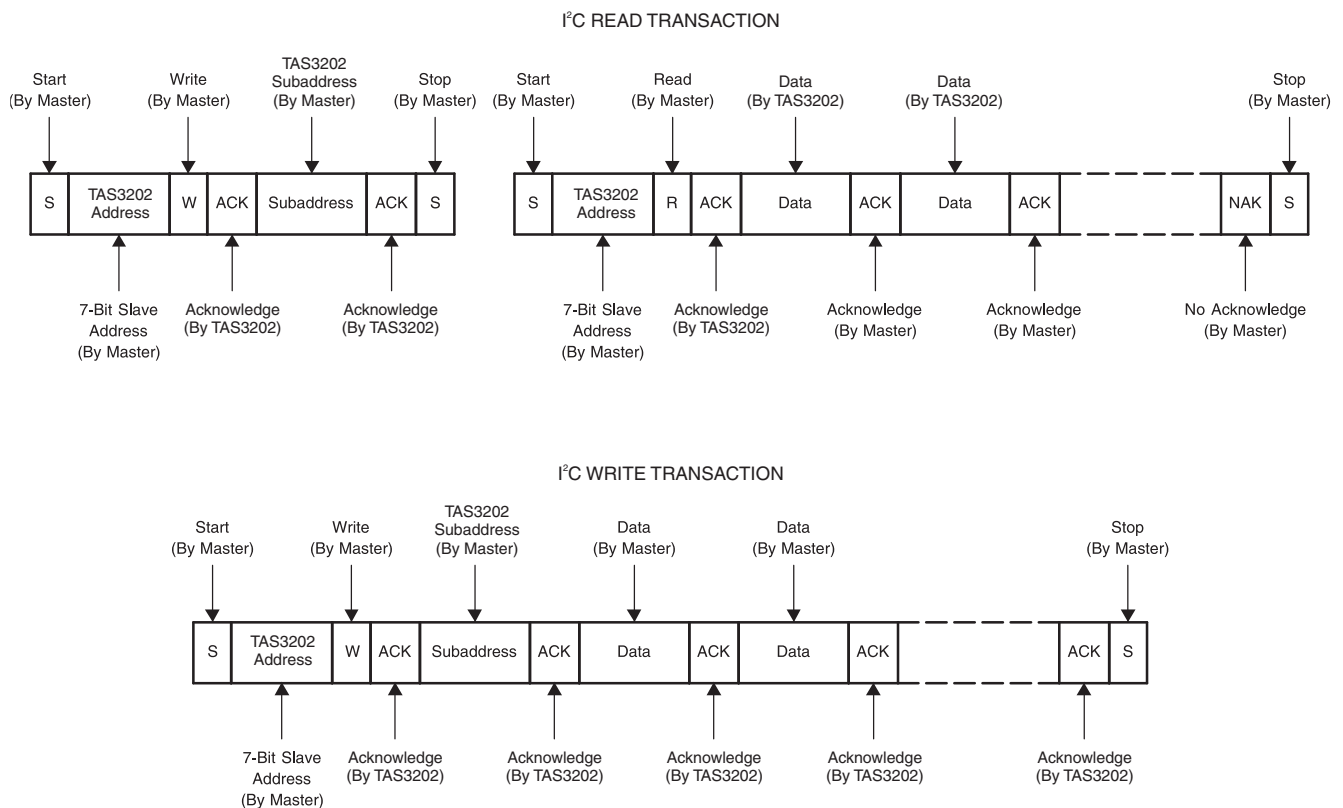


Figure 6-3. I²C Subaddress Access Protocol

6.3 I²C Slave-Mode Operation

The I²C slave mode is the mode that is used to change configuration parameters during operation and to perform program and coefficient downloads from a master device. The coefficient download operation in slave mode can be used to replace the I²C master-mode EEPROM download. The TAS3202 supports both random and sequential I²C transactions. The TAS3202 I²C slave address is 011010xy, where the first six bits are the TAS3202 device address and bit x is CS0, which is set by the TAS3202 internal microprocessor at power up. Bit y is the R/W bit. The pulldown resistance of CS0 creates a default 00 address when no connection is made to the pin. [Table 6-1](#) and [Table 6-3](#) show all the legal addresses for I²C slave and master modes.

The multiword transfers always store first word on the bus at a lower RAM address and increment such that the last word in the transfer is stored with the highest target RAM address. Consecutive I²C frame transfers increment target address such that the data in the last transfer is last in target memory address space.

When the Memory Load Control Register (0x04) is written by the system controller, the TAS3202 updates the status register by setting a error bit to indicate an error for the memory type that is being loaded. This error bit is reset when the operation complete and a valid checksum has been received. For example, when the micro program memory is being loaded, the TAS3202 sets a micro program memory error indication in the status register at the start of the sequence. When the last byte of the micro program memory and checksum is received, the TAS3202 clears the micro program memory error indication. This enables the TAS3202 to preserve any error status indications that occur as a result of incomplete transfers of data/ checksum error during a series of data and program memory load operations.

The checksum is always contained in the last two bytes of the data block. The I²C slave download is terminated when a termination header with a zero-length byte-count file is received.

The status register always reflects status of EEPROM boot attempts, unless the user writes to the slave control register. A write to the slave boot control register causes the EEPROM status register to reflect slave boot attempt status.

Refer to [Section 9.3](#) for formatting details.

NOTE

Once the micro program memory has been loaded, further updates to this memory are prohibited until the device is reset. The TAS3202 I²C block does respond to the broadcast address (00h).

Table 6-2. Slave Addresses

| BASE ADDRESS | CS0 | R/W | SLAVE ADDRESS |
|--------------|-----|-----|---------------|
| 0110 10 | 0 | 0 | 0x68 |
| 0110 10 | 0 | 1 | 0x69 |
| 0110 10 | 1 | 0 | 0x6A |
| 0110 10 | 1 | 1 | 0x6B |

Table 6-3. Master Addresses

| BASE ADDRESS | CS0 | R/W | MASTER ADDRESS |
|--------------|-----|-----|----------------|
| 1010 00 | 0 | 0 | 0xA0 |
| 1010 00 | 0 | 1 | 0xA1 |
| 1010 00 | 1 | 0 | 0xA2 |
| 1010 00 | 1 | 1 | 0xA3 |

The following is an example use of the I²C master address to access an external EEPROM. The TAS3202 can address up to two EEPROMs depending on the state of CS0. Initially, the TAS3202 comes up in I²C master mode. If it finds a memory such as the 24C512 EEPROM, it reads the headers and data as previously described. In this I²C master mode, the TAS3202 addresses the EEPROMs as shown in [Table 6-4](#) and [Table 6-5](#).

Table 6-4. EEPROM Address I²C TAS3202 Master Mode = 0xA1/A0

| MSB | | | | | A0 (EEPROM) | CS0 | R/W |
|-----|---|---|---|---|----------------|-----|-----|
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1/0 |

Table 6-5. EEPROM Address I²C TAS3202 Master Mode = 0xA3/A2

| MSB | | | | | A0 (EEPROM) | CS0 | R/W |
|-----|---|---|---|---|----------------|-----|-----|
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1/0 |

Random I²C Transactions

Supplying a subaddress for each subaddress transaction is referred to as random I²C addressing. For random I²C read commands, the TAS3202 responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a given subaddress does not use all 32 bits, the unused bits are read as logic 0. I²C write commands, however, are treated in accordance with the data assignment for that address space. If a write command is received for a mixer subaddress, for example, the TAS3202 expects to see five 32-bit words. If fewer than five data words have been received when a stop command (or another start command) is received, the data received is discarded.

Sequential I²C Transactions

The TAS3202 also supports sequential I²C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the 15 subaddresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS3202. For I²C sequential write transactions, the subaddress then serves as the start address and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written to. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; just the incomplete data is discarded.

Sequential read transactions do not have restrictions on outputting only complete subaddress data sets.

If the master does not issue enough data-received acknowledges to receive all the data for a given subaddress, the master device simply does not receive all the data.

If the master device issues more data-received acknowledges than required to receive the data for a given subaddress, the master device simply receives complete or partial sets of data, depending on how many data-received acknowledges are issued from the subaddress(es) that follow. I²C read transactions, both sequential and random, can impose I²C clock stretching.

6.3.1 Multiple-Byte Write

Multiple data bytes are transmitted by the master device to slave as shown in Figure 6-4. After receiving each data byte, the TAS3202 responds with an acknowledge bit.

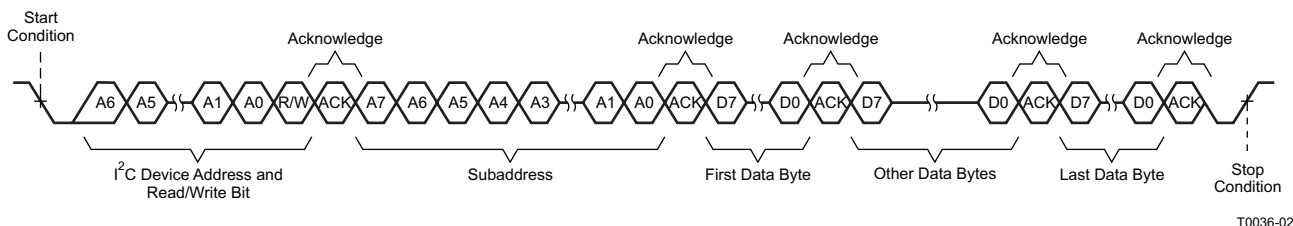


Figure 6-4. Multiple-Byte Write Transfer

6.3.2 Multiple-Byte Read

Multiple data bytes are transmitted by the TAS3202 to the master device as shown in Figure 6-5. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

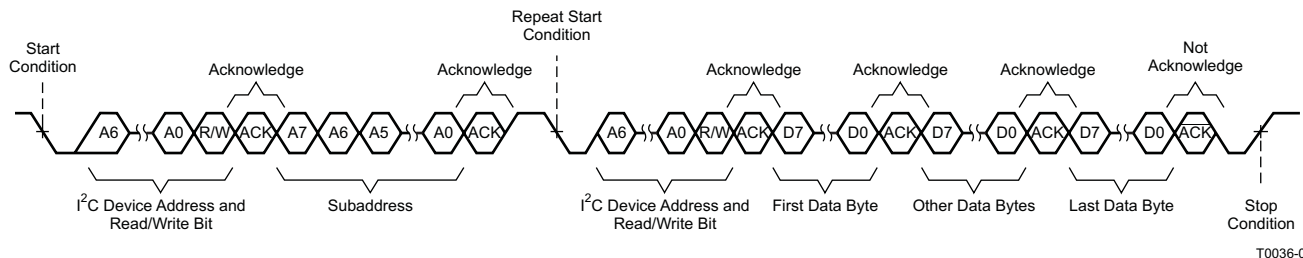


Figure 6-5. Multiple-Byte Read Transfer

6.4 I²C Master-Mode Device Initialization

I²C master-mode operation is enabled following a reset or power-on reset. Master-mode I²C transactions do not start until the I²C bus is idle.

The TAS3202 uses the master mode to download from EEPROM the memory contents for the microprocessor program memory, microprocessor extended memory, audio DSP core program memory, audio DSP core coefficient memory, and audio DSP core data memory.

The TAS3202, when operating as an I²C master, can execute a complete download of any internal memory or any section of any internal memory without requiring any wait states.

The TAS3202 generates a repeated start without an intervening stop command while downloading program and memory data from EEPROM. When a repeated start is sent to the EEPROM in read mode, the EEPROM enters a sequential read mode to transfer large blocks of data quickly.

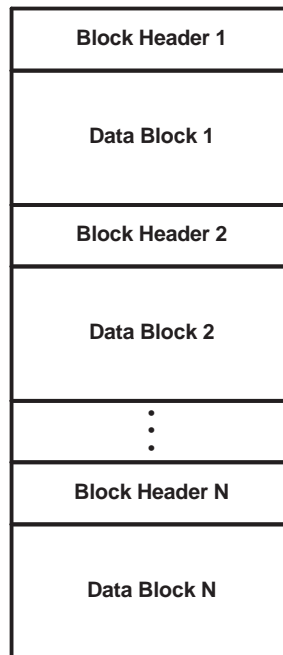
The TAS3202 queries the bus for an I²C EEPROM at address 1010xxx. The value xxx can be chip select, other information, or don't cares, depending on the EEPROM selected.

The first action of the TAS3202 as master is to transmit a start condition along with the device address of the I²C EEPROM with the read/write bit cleared (0) to indicate a write. The EEPROM acknowledges the address byte, and the TAS3202 sends a subaddress byte, which the EEPROM acknowledges. Most EEPROMs have at least 2-byte addresses and acknowledge as many as are appropriate. At this point, the EEPROM sends a last acknowledge and becomes a slave transmitter. The TAS3202 acknowledges each byte repeatedly to continue reading each data byte that is stored in memory.

The memory load information starts with reading the header and data information that starts at subaddress 0 of the EEPROM. This information must then be stored in sequential memory addresses with no intervening gaps. The data blocks are contiguous blocks of data that immediately follow the header locations.

The TAS3202 memory data can be stored and loaded in (almost) any order. Additionally, this addressing scheme permits portions of the TAS3202 internal memories to be loaded.

I²C EEPROM Memory Map



M0040–01

Figure 6-6. EEPROM Address Map

The TAS3202 sequentially reads EEPROM memory and loads its internal memory, unless it does not find a valid memory header block, is not able to read the next memory location because the end of memory was reached, detects a checksum error, or reads an end-of-program header block. When it encounters an invalid header or read error, the TAS3202 attempts to read the header or memory location three times before it determines that it has an error. If the TAS3202 encounters a checksum error, it attempts to reread the entire block of memory two more times before it determines that it has an error.

Once the microprocessor program memory has been loaded, it cannot be reloaded until the TAS3202 has been reset.

If an error is encountered, TAS3202 terminates its memory-load operation, loads the default configuration from ROM, and disables further master I²C bus operations.

If an end-of-program data block is read, the TAS3202 has completed the initial program load.

The I²C master mode uses the starting and ending I²C checksums to verify a proper EEPROM download. The first 16-bit data word received from the EEPROM, the I²C checksum at subaddress 0x00, is stored and compared against the 16-bit data word received for the last subaddress, the ending I²C checksum, and the checksum that is computed during the download. These three values must be equal. If the read and computed values do not match, the TAS3202 sets the memory read error bits in the status register and repeats the download from the EEPROM two more times. If the comparison check fails the third time, the TAS3202 sets the microprocessor program to the default value.

[Table 6-6](#) shows the format of the EEPROM or other external memory load file. Each line of the file is a byte (in ASCII format). The checksum is the summation of all the bytes (with beginning and ending checksum fields = 00). The final checksum inserted into the checksum field is the lowest significant four bytes of the checksum.

Example:

Given the following example 8051 data or program block (must be a multiple of 4 bytes for these blocks):

10h
20h
30h
40h
50h
60h
70h
80h

The checksum = 10h + 20h + 30h + 30h + 40h + 50h + 60h + 70h + 80h = 240h, so

the values put in the checksum fields are MS byte = 02h and LS byte = 40h.

If the checksum is >FFFFh, then the 2-byte checksum field is the least-significant 2 bytes.

For example, if the checksum is 1D 45B6h, the checksum field is MS byte = 45h and LS byte = B6h.

Table 6-6. TAS3202 Memory Block Structures

| STARTING BYTE | DATA BLOCK FORMAT | SIZE | NOTES |
|--|---|---------|---|
| 12-Byte Header Block | | | |
| 0 | Checksum code MS byte | 2 bytes | Checksum of bytes 2 through N + 12. If this is a termination header, this value is 00 00 |
| | Checksum code LS byte | | |
| 2 | Header ID byte 1 = 0x00 | 2 bytes | Must be 0x001F for the TAS3202 to load as part of initialization. Any other value terminates the initialization memory load sequence. |
| | Header ID byte 2 = 0x1F | | |
| 4 | Memory to be loaded | 1 byte | 0x00 – Microprocessor program memory or termination header 0x01 – Microprocessor external data memory 0x02 – Audio DSP core program memory 0x03 – Audio DSP core coefficient memory 0x04 – Audio DSP core data memory 0x05–06 – Audio DSP upper program memory 0x07 – Audio DSP upper coefficient memory 0x08–FF – Reserved for future expansion |
| 5 | 0x00 | 1 byte | Unused |
| 6 | Start TAS3202 memory address MS byte | 2 bytes | If this is a termination header, this value is 0000. |
| | Start TAS3202 memory address LS byte | | |
| 8 | Total number of bytes transferred MS byte | 2 bytes | 12 + data bytes + last checksum bytes. If this is a termination header, this value is 0000. |
| | Total number of bytes transferred LS byte | | |
| 10 | 0x00 | 1 bytes | Unused |
| 11 | 0x00 | 1 bytes | Unused |
| Data Block for Microprocessor Program or Data Memory (Following 12-Byte Header) | | | |
| 12 | Data byte 1 (LS byte) | 4 bytes | 1–4 microprocessor bytes |
| | Data byte 2 | | |
| | Data byte 3 | | |
| | Data byte 4 (MS byte) | | |
| 16 | Data byte 5 | 4 bytes | 5–8 microprocessor bytes |
| | Data byte 6 | | |
| | Data byte 7 | | |
| | Data byte 8 | | |
| | • | | |
| | • | | |
| | • | | |
| N + 8 | Data byte $4 \times (Z - 1) + 1$ | 4 bytes | |
| | Data byte $4 \times (Z - 1) + 2$ | | |
| | Data byte $4 \times (Z - 1) + 3$ | | |
| | Data byte $4 \times (Z - 1) + 4 = N$ | | |
| N + 12 | 0x00 | 4 bytes | Repeated checksum bytes 2 through N + 11 |
| | 0x00 | | |
| | Checksum code MS byte | | |
| | Checksum code LS byte | | |

Table 6-6. TAS3202 Memory Block Structures (continued)

| STARTING BYTE | DATA BLOCK FORMAT | SIZE | NOTES |
|--|--------------------------------------|---------|---|
| Data Block for Audio DSP Core Coefficient Memory (Following 12-Byte Header) | | | |
| 12 | Data byte 1 (LS byte) | 4 bytes | Coefficient word 1 (valid data in D27–D0) D7–D0 |
| | Data byte 2 | | D15–D8 |
| | Data byte 3 | | D23–D16 |
| | Data byte 4 (MS byte) | | D31–D24 |
| 16 | Data byte 5 | 4 bytes | Coefficient word 2 |
| | Data byte 6 | | |
| | Data byte 7 | | |
| | Data byte 8 | | |
| | • | | |
| | • | | |
| | • | | |
| N + 8 | Data byte $4 \times (Z - 1) + 1$ | 4 bytes | Coefficient word Z |
| | Data byte $4 \times (Z - 1) + 2$ | | |
| | Data byte $4 \times (Z - 1) + 3$ | | |
| | Data byte $4 \times (Z - 1) + 4 = N$ | | |
| N + 12 | 0x00 | 4 bytes | Repeated checksum bytes 2 through N + 11 |
| | 0x00 | | |
| | Checksum code MS byte | | |
| | Checksum code LS byte | | |
| Data Block for Audio DSP Core Data Memory (Following 12-Byte Header) | | | |
| 12 | Data byte 1 (LS byte) | 6 bytes | Data word 1 D7–D0 |
| | Data byte 2 | | D15–D8 |
| | Data byte 3 | | D23–D16 |
| | Data byte 4 | | D31–D24 |
| | Data byte 5 | | D39–D32 |
| | Data byte 6 (MS byte) | | D47–D40 |
| 18 | Data byte 7 | 6 bytes | Data 2 |
| | Data byte 8 | | |
| | Data byte 9 | | |
| | Data byte 10 | | |
| | Data byte 11 | | |
| | Data byte 12 | | |
| | • | | |
| | • | | |
| | • | | |
| N + 6 | Data byte $6 \times (Z - 1) + 1$ | 6 bytes | Data Z |
| | Data byte $6 \times (Z - 1) + 2$ | | |
| | Data byte $6 \times (Z - 1) + 3$ | | |
| | Data byte $6 \times (Z - 1) + 4$ | | |
| | Data byte $6 \times (Z - 1) + 5$ | | |
| | Data byte $6 \times (Z - 1) + 6 = N$ | | |

Table 6-6. TAS3202 Memory Block Structures (continued)

| STARTING BYTE | DATA BLOCK FORMAT | SIZE | NOTES |
|--|---|---------|---|
| N + 12 | 0x00 | 6 bytes | Repeated checksum bytes 2 through N + 11 |
| | 0x00 | | |
| | 0x00 | | |
| | 0x00 | | |
| | Checksum code MS byte | | |
| | Checksum code LS byte | | |
| Data Block for Audio DSP Core Program Memory (Following 12-Byte Header) | | | |
| 12 | Program byte 1 (LS byte) | 7 bytes | Program word 1 (valid data in D53–D0) D7–D0 |
| | Program byte 2 | | D15–D8 |
| | Program byte 3 | | D23–D16 |
| | Program byte 4 | | D31–D24 |
| | Program byte 5 | | D39–D32 |
| | Program byte 6 | | D47–D40 |
| | Program byte 7 (MS byte) | | D55–D48 |
| 19 | Program byte 8 | 7 bytes | Program word 2 |
| | Program byte 9 | | |
| | Program byte 10 | | |
| | Program byte 11 | | |
| | Program byte 12 | | |
| | Program byte 14 | | |
| | • | | |
| | • | | |
| | • | | |
| N + 5 | Program byte $7 \times (Z - 1) + 1$ | 7 bytes | Program word Z |
| | Program byte $7 \times (Z - 1) + 2$ | | |
| | Program byte $7 \times (Z - 1) + 3$ | | |
| | Program byte $7 \times (Z - 1) + 4$ | | |
| | Program byte $7 \times (Z - 1) + 5$ | | |
| | Program byte $7 \times (Z - 1) + 6$ | | |
| | Program byte $7 \times (Z - 1) + 7 = N$ | | |
| N + 12 | 0x00 | 7 bytes | Repeated checksum bytes 2 through N + 11 |
| | 0x00 | | |
| | 0x00 | | |
| | 0x00 | | |
| | 0x00 | | |
| | Checksum code MS byte | | |
| Checksum code LS byte | | | |

Table 6-6. TAS3202 Memory Block Structures (continued)

| STARTING BYTE | DATA BLOCK FORMAT | SIZE | NOTES |
|--|-------------------|---------|---|
| 20-Byte Termination Block (Last Block of Entire Load Block) | | | |
| B _{LAST} – 19 | 0x00 | 2 bytes | First 2 bytes of termination block are always 0x0000. |
| | 0x00 | | |
| B _{LAST} – 17 | 0x00 | 2 bytes | Second 2 bytes are always 0x001F. |
| | 0x1F | | |
| B _{LAST} – 15 | 0x00 | 1 byte | Last 16 bytes must each be 0x00. |
| B _{LAST} – 14 | 0x00 | 1 byte | |
| | • | | |
| | • | | |
| | • | | |
| | • | | |
| B _{LAST} | 0x00 | 1 byte | |

7 Digital Audio Processor (DAP) Arithmetic Unit

The DAP arithmetic unit is a fixed-point computational engine consisting of an arithmetic unit and data and coefficient memory blocks. The primary features of the DAP are:

- Two-pipe parallel processing architecture
 - 48-bit data path with 76-bit accumulator
 - Hardware single cycle multiplier (28×48)
 - Three 48-bit general-purpose data registers and one 28-bit coefficient register
 - Four simultaneous operations per machine cycle
 - Shift right, shift left, and bimodal clip
 - Log2/Alog2
 - Magnitude Truncation
- Hardware acceleration units
 - Soft volume controller
 - Delay memory
 - Dither generator
 - Log2/2× estimator
- 1024 + 768 dual-port ports words of data (24 and 48 bits, respectively)
- 1228 words of coefficient memory (28 bits)
- 3K word of program RAM (55 bits)
- 5.88K words of 24-bits delay memory (1.22 ms)
- Coefficient RAM, data RAM, LFSR seed, program counter, and memory pointers are all mapped into the same memory space for convenient addressing by the microcontroller.
- Memory interface block contains four pointers, two for data memory and two for coefficient memory.

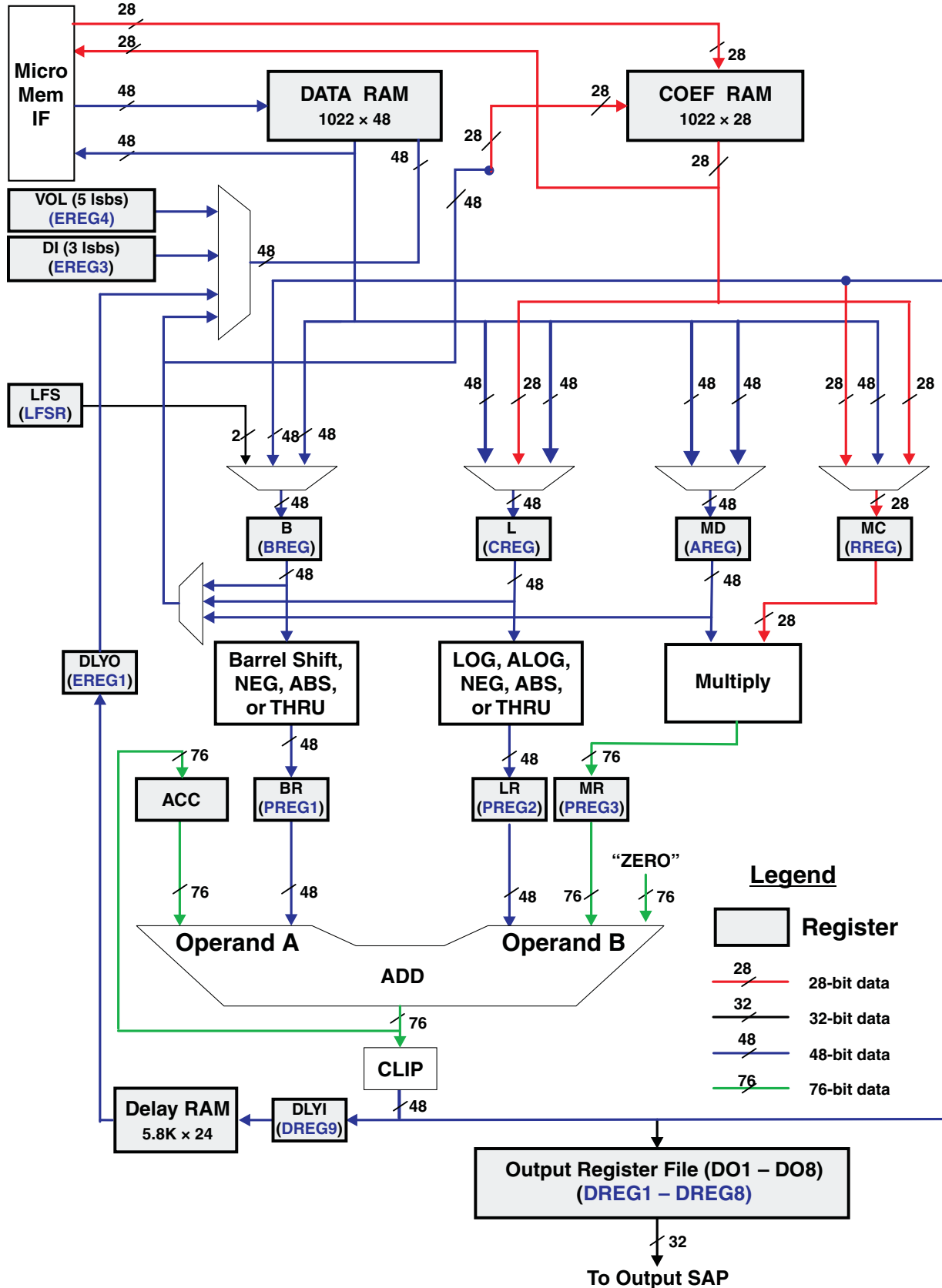


Figure 7-1. DSP Core Block Diagram

7.1 DAP Instructions Set

Please see this information in the *TAS3xxx DAS Instruction Set Reference Guide*, available to those registered to the TAS3xxx-PurePath Studio Extranet.

7.2 DAP Data Word Structure

Figure 7-2 shows the data word structure of the DAP arithmetic unit. Eight bits of overhead or guard bits are provided at the upper end of the 48-bit DAP word, and 16 bits of computational precision or noise bits are provided at the lower end of the 48-bit word. The incoming digital audio words are all positioned with the MSB abutting the 8-bit overhead/guard boundary. The sign bit in bit 39 indicates that all incoming audio samples are treated as signed data samples. The arithmetic engine is a 48-bit (25.23 format) processor consisting of a general-purpose 76-bit ALU and function-specific arithmetic blocks. Multiply operations (excluding the function-specific arithmetic blocks) always involve 48-bit DAP words and 28-bit coefficients (usually I²C programmable coefficients). If a group of products is to be added together, the 76-bit product of each multiplication is applied to a 76-bit adder, where a DSP-like multiply-accumulate (MAC) operation takes place. Biquad filter computations use the MAC operation to maintain precision in the intermediate computational stages.

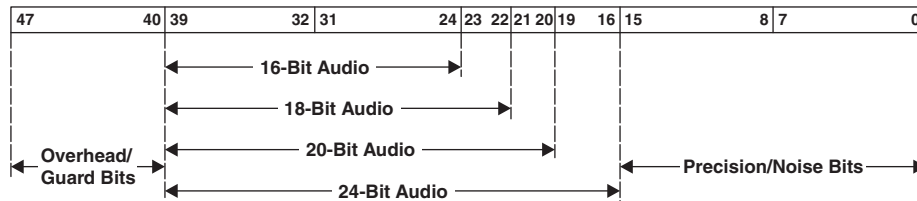


Figure 7-2. Arithmetic Unit Data Word Structure

To maximize the linear range of the 76-bit ALU, saturation logic is not used. In MAC computations, intermediate overflows are permitted, and it is assumed that subsequent terms in the computation flow correct the overflow condition (see Figure 7-3). The DAP memory banks include a dual port data RAM for storing intermediate results, a coefficient RAM, and a fixed program ROM. Only the coefficient RAM, accessible via the I²C bus, is available to the user.

| | | | | | | | | | | |
|----------|---|---|---|---|---|---|---|---|--------|-------|
| | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | (-73) | -73 |
| + | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | (-51) | + -51 |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | (-124) | -124 |
| + | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | (-45) | + -45 |
| Rollover | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | (57) | 57 |
| + | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | (59) | + 59 |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | (-110) | -110 |

Figure 7-3. DSP ALU Operation With Intermediate Overflow

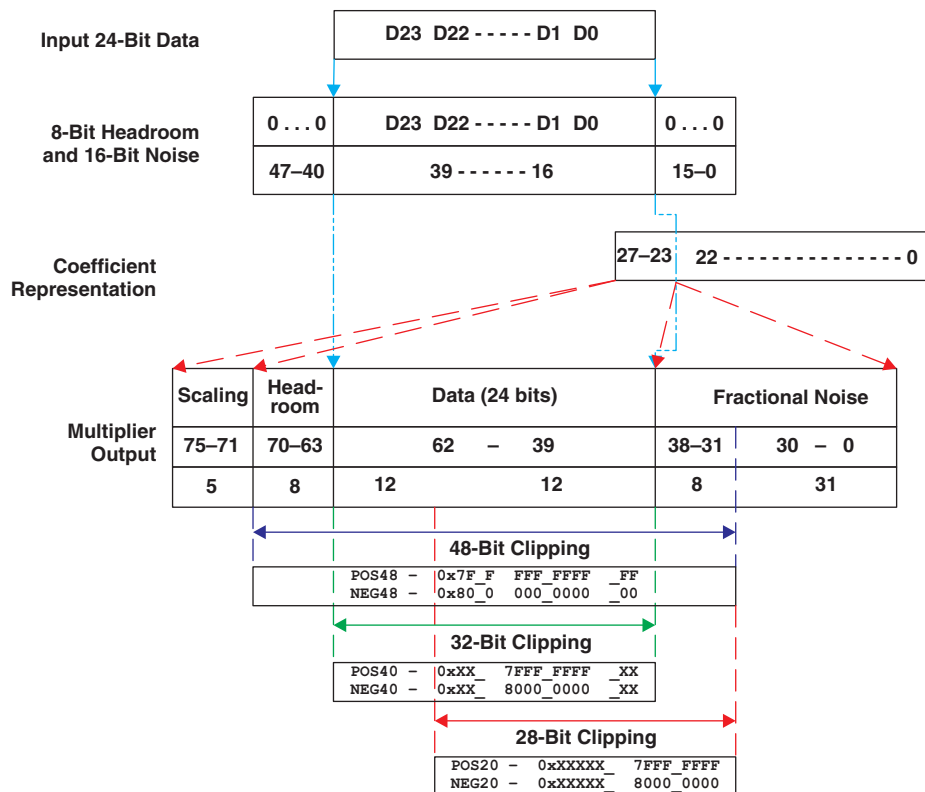


Figure 7-4. DAP Data-Path Data Representation

8 Electrical Specifications

8.1 Absolute Maximum Ratings⁽¹⁾

over operating temperature range (unless otherwise noted)

| | | | |
|------------------|--|---------------------|--------------------------------|
| DVDD | Digital supply voltage range | | –0.5 V to 3.8 V |
| AVDD | Analog supply voltage range | | –0.5 V to 3.8 V |
| V _I | Input voltage range | 3.3-V TTL | –0.5 V to DVDD + 0.5 V |
| | | 1.8 V LVCMOS (XTLI) | –0.5 V to 2.3 V |
| V _O | Output voltage range | 3.3 V TTL | –0.5 V to DVDD + 0.5 V |
| | | 1.8 V LVCMOS (XTLO) | –0.5 V to 2.3 V ⁽²⁾ |
| I _{IK} | Input clamp current (V _I < 0 or V _I > DVDD) | | ±20 µA |
| I _{OK} | Output clamp current (V _O < 0 or V _O > DVDD) | | ±20 µA |
| T _A | Operating free-air temperature range | | 0°C to 70°C |
| T _{stg} | Storage temperature range | | –65°C to 150°C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Pin XTAL_OUT is the only TAS3202 output that is derived from the internal 1.8-V logic supply. The absolute maximum rating listed is for reference; only a crystal should be connected to XTAL_OUT.

Note:

- VR_ANA is derived from TAS3202 internal 1.8-V voltage regulator. This terminal must not be used to power external devices.
- VR_DIG is derived from TAS3202 internal 1.8-V voltage regulator. This terminal must not be used to power external devices.
- VR_PLL is derived from TAS3202 internal 1.8-V voltage regulator. This terminal must not be used to power external devices.

8.2 Package Dissipation Ratings

| PACKAGE DESCRIPTION | | | T _A ≤ 25°C POWER RATING (mW) | DERATING FACTOR ABOVE T _A = 25°C (mW/°C) | T _A = 70°C POWER RATING (mW) |
|---------------------|-----------|--------------------|---|---|---|
| PACKAGE TYPE | PIN COUNT | PACKAGE DESIGNATOR | | | |
| TQFP | 64 | PAG | 1869 | 23.36 | 818 |

8.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|-----------------|-----------------------------------|-----------------------|-----|-----|------------------|
| DVDD | Digital supply voltage | 3 | 3.3 | 3.6 | V |
| AVDD | Analog supply voltage | 3 | 3.3 | 3.6 | V |
| V _{IH} | High-level input voltage | 3.3-V TTL | 2 | | V |
| | | 1.8-V LVCMOS (XTL_IN) | 1.2 | | |
| V _{IL} | Low-level input voltage | 3.3-V TTL | | 0.8 | V |
| | | 1.8-V LVCMOS (XTL_IN) | | 0.5 | |
| T _A | Operating ambient air temperature | 0 | 25 | 70 | °C |
| T _J | Operating junction temperature | 0 | | 105 | °C |
| | Analog differential input | | 2 | | V _{RMS} |
| | Analog output load | Resistance | | 10 | kΩ |
| | | Capacitance | | 100 | pF |

8.4 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---------------------------------|--------------------------------------|------------------------|---|-----|------|------|----|
| V _{OH} | High-level output voltage | 3.3-V TTL | I _{OH} = –4 mA | | | 2.4 | V |
| | | 1.8-V LVCMOS (XTL_OUT) | I _{OH} = –0.55 mA | | | 1.44 | |
| V _{OL} | Low-level output voltage | 3.3-V TTL | I _{OL} = 4 mA | | | 0.5 | V |
| | | 1.8-V LVCMOS (XTL_OUT) | I _{OL} = 0.75 mA | | | 0.4 | |
| I _{OZ} | High-impedance output current | 3.3-V TTL | V _I = V _{IL} | | | ±20 | µA |
| I _{IL} | Low-level input current | 3.3-V TTL | V _I = V _{IL} | | | ±20 | µA |
| | | 1.8-V LVCMOS (XTL_IN) | V _I = V _{IL} | | | ±20 | |
| I _{IH} | High-level input current | 3.3-V TTL | V _I = V _{IH} | | | ±20 | µA |
| | | 1.8-V LVCMOS (XTL_IN) | V _I = V _{IH} | | | ±20 | |
| I _{DVDD} | Digital supply current | Normal operation | MCLK_IN = 24.576 MHz, LRCLK = 48 kHz | | | 130 | mA |
| I _{AVDD} | Analog supply current | Normal operation | MCLK_IN = 24.576 MHz, LRCLK = 48 kHz | | | 60 | mA |
| Power Dissipation (Total) | Digital and analog supply current | Normal operation | MCLK_IN = 24.576 MHz, LRCLK = 48 kHz | | | 627 | mW |
| | | Standby mode | With voltage regulators on | | | 23 | mW |
| | | | With voltage regulators off | | | 825 | µW |
| | | Reset mode | | | | 20 | mW |
| VR_ANA | Internal voltage regulator – analog | | 1.6 | 1.8 | 1.98 | V | |
| VR_PLL | Internal voltage regulator – PLL | | 1.6 | 1.8 | 1.98 | V | |
| VR_DIG | Internal voltage regulator – digital | | 1.6 | 1.8 | 1.98 | V | |

8.5 Audio Specifications

$T_A = 25^\circ\text{C}$, $AVDD = 3.3\text{ V}$, $DVDD = 3.3\text{ V}$, $F_s = 48\text{ kHz}$, 1-kHz sine wave full scale, over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---|---|---|---|----------------------|-----|------------|----|
| Overall performance: input ADC – DAP – DAC – line out | Dynamic range | Evaluation module, A-weighted, –60 dB with respect to full scale | | 100 | | dB | |
| | THD+N | Evaluation module, –3 dB with respect to full scale | | 101 | | dB | |
| ADC section | Dynamic range | A-weighted, –60 dB with respect to full scale | | 102 | | dB | |
| | THD+N | –4 dB with respect to full scale | | 93 | | dB | |
| | Crosstalk | One channel = –3 dB, Other channel = 0 V | | 84 | | dB | |
| | Power supply rejection ratio | 1 kHz, 100 mVpp on AVDD | | 57 | | dB | |
| | Input resistance | | | 20 | | k Ω | |
| | Input capacitance | | | 10 | | pF | |
| ADC decimation filter | Pass-band edge | | | 0.45Fs | | Hz | |
| | Pass-band ripple | | | ± 0.01 | | dB | |
| | Stop-band edge | | | 0.55Fs | | Hz | |
| | Stop-band attenuation | | | 100 | | dB | |
| | Group delay | | | 37 \pm Fs | | Sec | |
| DAC section | Differential full-scale output voltage | | | 2 | | V_{RMS} | |
| | Dynamic range | A-weighted, –60 dB with respect to full scale | | 105 | | dB | |
| | THD+N | –1-dBFS input, 0-dB gain | | 95 | | dB | |
| | Crosstalk | DAC to ADC | One channel –3 dBFS, Other channel 0 V | | 84 | | dB |
| | | ADC to DAC | One channel –3 dB, Other channel 0 V | | 84 | | dB |
| | | DAC to DAC | One channel –3 dBFS; Other channel 0 V | | 84 | | dB |
| | Power-supply rejection ratio | 1 kHz, 100 mVpp on AVDD | | 56 | | dB | |
| DC offset | With respect to V_{REF} | | | | mV | | |
| DAC interpolation filter | Pass-band edge | | | 0.45Fs | | Hz | |
| | Pass-band ripple | | | ± 0.06 | | dB | |
| | Transition band | | | 1.45 Fs to 0.55Fs | | Hz | |
| | Stop-band edge | | | 7.4Fs | | Hz | |
| | Stop-band attenuation | | | –65 | | dB | |
| | Filter group delay | | | 21 \pm Fs | | Sec | |

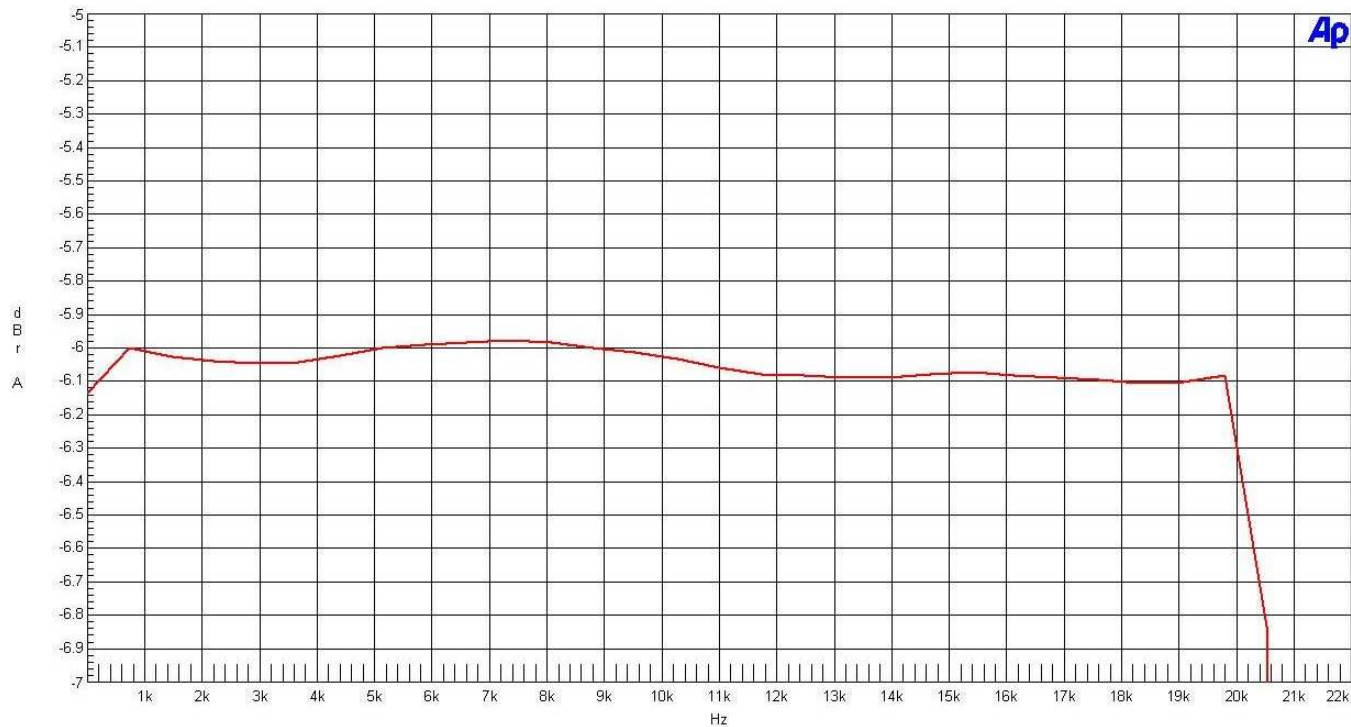


Figure 8-1. Frequency Response (ADC-DAC)

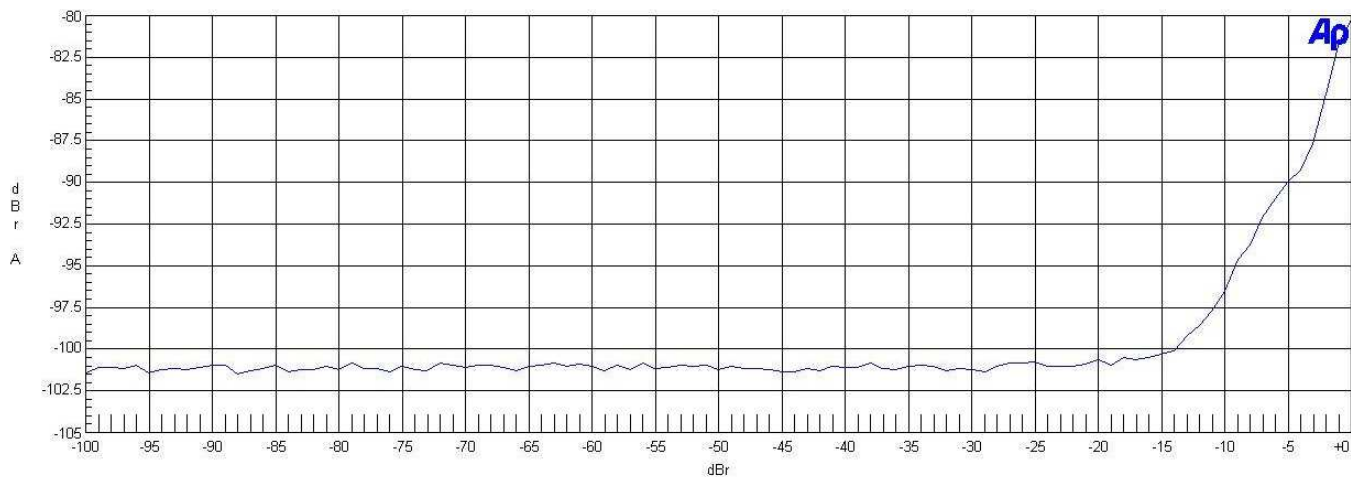


Figure 8-2. THD+N (ADC-DAC)

8.6 Timing Characteristics

The following sections describe the timing characteristics of the TAS3202.

8.7 Master Clock

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|--|-----------------|----------------|----------------|----------------|------|
| $f_{(XTAL_IN)}$ | Frequency, XTAL_IN ($1/ t_{c(1)}$) | See (1) | | 512Fs | | Hz |
| $t_{c(1)}$ | Cycle time, XTAL_IN | | | 1÷512Fs | | Sec |
| $f_{(MCLK_IN)}$ | Frequency, MCLK_IN ($1/ t_{c(2)}$) | | | 512Fs | | Hz |
| $t_{w(MCLK_IN)}$ | Pulse duration, MCLK_IN high | See (2) | 0.4 $t_{c(2)}$ | 0.5 $t_{c(2)}$ | 0.6 $t_{c(2)}$ | ns |
| | Crystal frequency deviation | | | | 50 | ppm |
| $f_{(MCLKO)}$ | Frequency, MCLKO ($1/ t_{c(3)}$) | | | 256Fs | | Hz |
| $t_{r(MCLKO)}$ | Rise time, MCLKO | $C_L = 30$ pF | | | 15 | ns |
| $t_{f(MCLKO)}$ | Fall time, MCLKO | $C_L = 30$ pF | | | 15 | ns |
| $t_{w(MCLK_IN)}$ | Pulse duration, MCLKO high | See (3) | | H_{MCLKO} | | ns |
| MCLKO jitter | XTAL_IN master clock source | | | 80 | | ps |
| | MCLK_IN master clock source | See (4) | | | | |
| $t_{d(MI-MO)}$ | Delay time, MCLK_IN rising edge to MCLKO rising edge | MCLKO = MCLK_IN | See (5) | | 20 | ns |
| | | MCLKO < MCLK_IN | See (5) (6) | | 20 | |

- (1) Duty cycle is 50/50.
- (2) Period of MCLK_IN = $T_{MCLK_IN} = 1/f_{MCLK_IN}$
- (3) $H_{MCLKO} = 1/(2 \times MCLKO)$. MCLKO has the same duty cycle as MCLK_IN when MCLKO = MCLK_IN. When MCLKO = 0.5 MCLK_IN or 0.25 MCLK_IN, the duty cycle of MCLKO is typically 50%.
- (4) When MCLKO is derived from MCLK_IN, MCLKO jitter = MCLK_IN jitter
- (5) Only applies when MCLK_IN is selected as master source clock
- (6) Also applies to MCLKO falling edge when MCLKO = MCLK_IN/2 or MCLK_IN/4

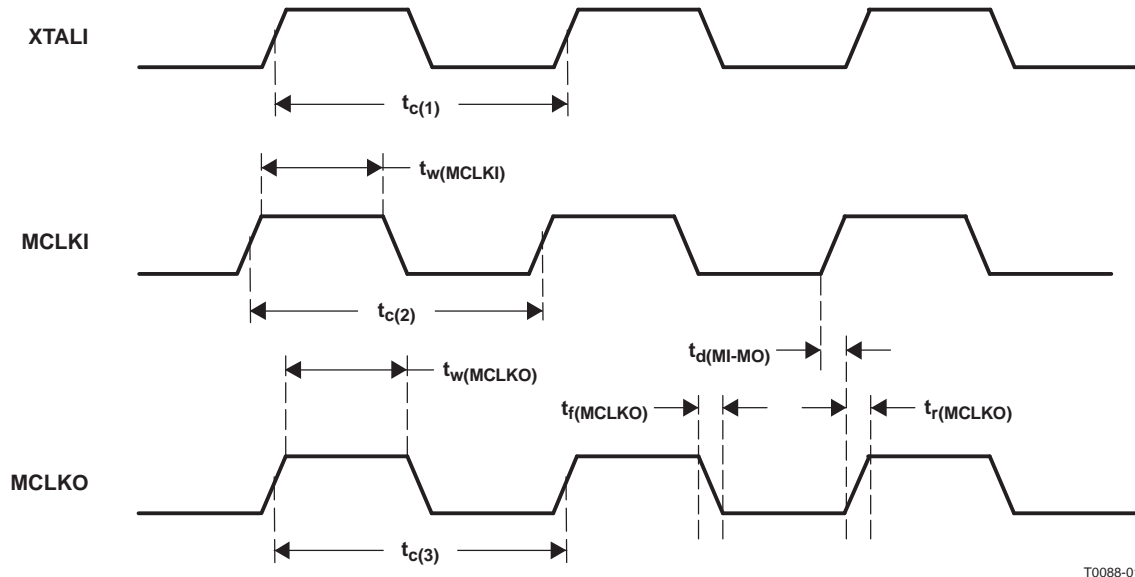


Figure 8-3. Master Clock Signal Timing Waveforms

T0088-01

8.8 Serial Audio Port, Slave Mode

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-----------------|---|---------|---------------------|---------------------|---------------------|----|
| f_{LRCLK} | Frequency, LRCLK (f_s) | | | 48 | kHz | |
| $t_{w(SCLKIN)}$ | Pulse duration, SCLKIN high | See (1) | 0.4 $t_{c(SCLKIN)}$ | 0.5 $t_{c(SCLKIN)}$ | 0.6 $t_{c(SCLKIN)}$ | ns |
| f_{SCLKIN} | Frequency, SCLKIN | See (2) | 64 F_s | | MHz | |
| t_{pd1} | Propagation delay, SCLKIN falling edge to SDOUT | | | 16 | ns | |
| t_{su1} | Setup time, LRCLK to SCLKIN rising edge | 10 | | | ns | |
| t_{h1} | Hold time, LRCLK from SCLKIN rising edge | 5 | | | ns | |
| t_{su2} | Setup time, SDIN to SCLKIN rising edge | 10 | | | ns | |
| t_{h2} | Hold time, SDIN from SCLKIN rising edge | 5 | | | ns | |
| t_{pd2} | Propagation delay, SCLKIN falling edge to SCLKOUT2 falling edge | | | 15 | ns | |

(1) Period of SCLKIN = $T_{SCLKIN} = 1/f_{SCLKIN}$

(2) Duty cycle is 50/50.

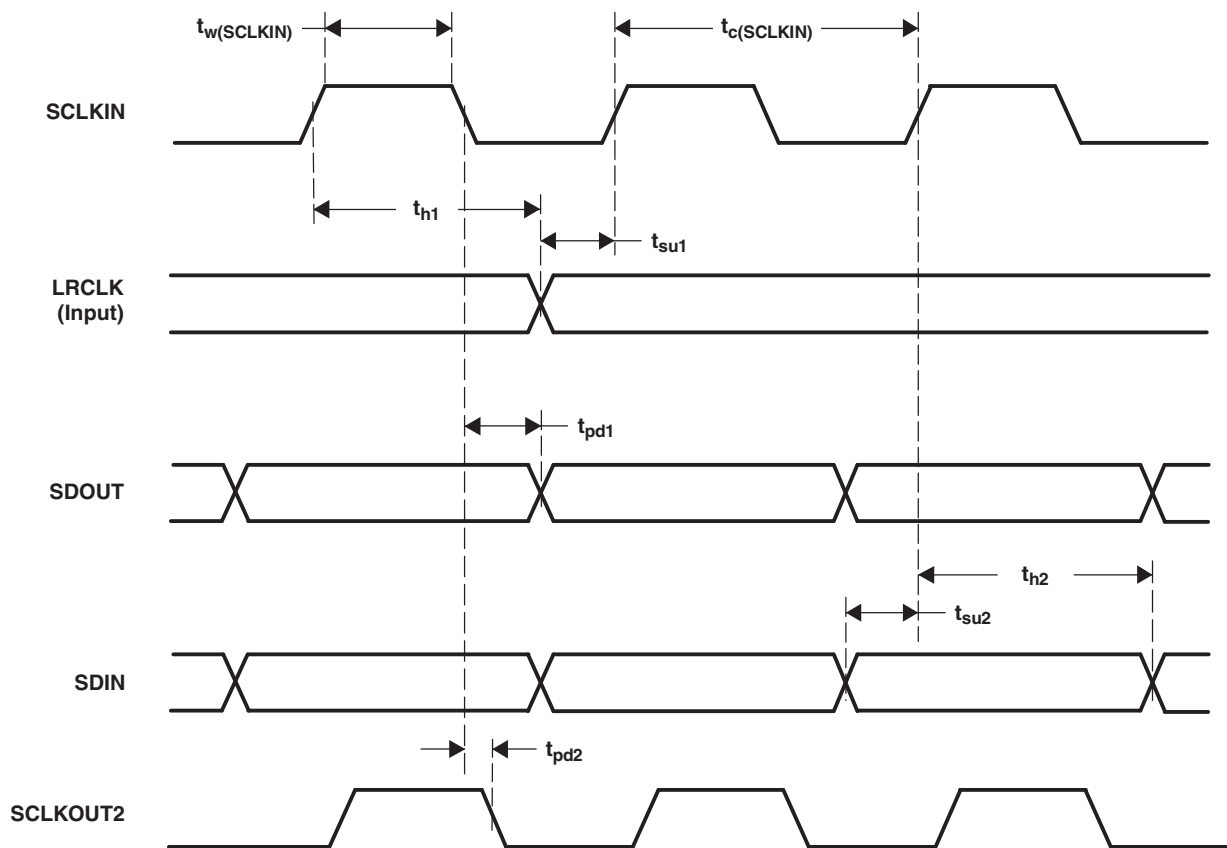


Figure 8-4. Serial Audio Port Slave Mode Timing Waveforms

8.9 Serial Audio Port, Master Mode (TAS3202)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|---|-----------------------|-----|---------|-----|------|
| $f_{(LRCLK)}$ | Frequency LRCLK | $C_L = 30 \text{ pF}$ | | 48 | | kHz |
| $t_{r(LRCLK)}$ | Rise time, LRCLK ⁽¹⁾ | $C_L = 30 \text{ pF}$ | | | 12 | ns |
| $t_{f(LRCLK)}$ | Fall time, LRCLK ⁽¹⁾ | Duty cycle is 50/50 | | | 12 | ns |
| $f_{(SCLKOUT)}$ | Frequency, SCLKOUT | $C_L = 30 \text{ pF}$ | | $64F_S$ | | MHz |
| $t_{r(SCLKOUT)}$ | Rise time, SCLKOUT | $C_L = 30 \text{ pF}$ | | | 12 | ns |
| $t_{f(SCLKOUT)}$ | Fall time, SCLKOUT | $C_L = 30 \text{ pF}$ | | | 12 | ns |
| $t_{pd1(SCLKOUT)}$ | Propagation delay, SCLKOUT falling edge to LRCLK edge | | | | 5 | ns |
| t_{pd2} | Propagation delay, SCLKOUT falling edge to SDOUT | | | | 5 | ns |
| t_{su} | Setup time, SDIN to SCLKOUT rising edge | | 25 | | | ns |
| t_h | Hold time, SDIN from SCLKOUT rising edge | | 30 | | | ns |

(1) Rise time and fall time measured from 20% to 80% of maximum height of waveform.

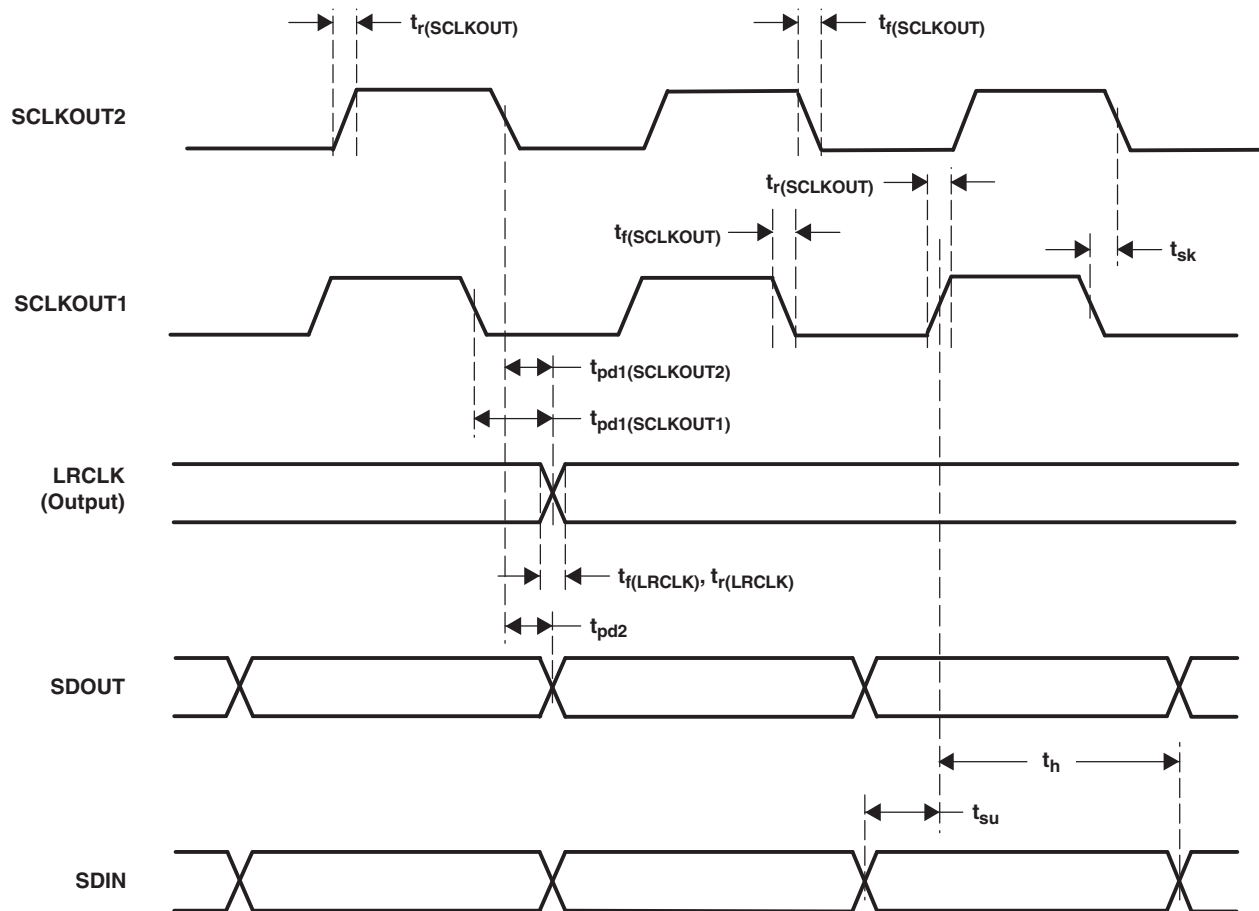


Figure 8-5. Serial Audio Port Master Mode Timing Waveforms

8.10 Pin-Related Characteristics of the SDA and SCL I/O Stages for F/S-Mode I²C-Bus Devices

| PARAMETER | TEST CONDITIONS | STANDARD MODE | | FAST MODE | | UNIT |
|----------------------|--|--------------------------------------|-----|---------------------------|-------------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{IL} | LOW-level input voltage | -0.5 | 0.8 | -0.5 | 0.8 | V |
| V _{IH} | HIGH-level input voltage | 2 | | 2 | | V |
| V _{hys} | Hysteresis of inputs | N/A | N/A | 0.05 V _{DD} | | V |
| V _{OL1} | LOW-level output voltage (open drain or open collector) | 3-mA sink current | | 0 | 0.4 | V |
| t _{of} | Output fall time from V _{IHmin} to V _{ILmax} | Bus capacitance from 10 pF to 400 pF | | 7 + 0.1 C _{b(1)} | 250 | ns |
| I _I | Input current, each I/O pin | -10 | 10 | -10 ⁽²⁾ | 10 ⁽²⁾ | μA |
| t _{SP(SCL)} | SCL pulse duration of spikes that must be suppressed by the input filter | N/A | N/A | 14 ⁽³⁾ | | ns |
| t _{SP(SDA)} | SDA pulse duration of spikes that must be suppressed by the input filter | N/A | N/A | 22 ⁽³⁾ | | ns |
| C _I | Capacitance, each I/O pin | | 10 | | 10 | pF |

(1) C_b = capacitance of one bus line in pF. The output fall time is faster than the standard I²C specification.

(2) The I/O pins of fast-mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.

(3) These values are valid at the 135-MHz DSP clock rate. If DSP clock is reduced by half, the t_{SP} doubles.

8.11 Bus-Related Characteristics of the SDA and SCL I/O Stages for F/S-Mode I²C-Bus Devices

all values are referred to V_{IHmin} and V_{ILmax} (see Section 8.10)

| PARAMETER | STANDARD MODE | | FAST MODE | | UNIT | | |
|---------------------|--|-----|----------------------|------|--|--------------------|-----|
| | MIN | MAX | MIN | MAX | | | |
| f _{SCL} | SCL clock frequency | | 0 | 100 | 0 | 400 ⁽¹⁾ | kHz |
| t _{HD-STA} | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | | 4 | | 0.6 | | μs |
| t _{LOW} | LOW period of the SCL clock | | 4.7 | | 1.3 | | μs |
| t _{HIGH} | HIGH period of the SCL clock | | 4 | | 0.6 | | μs |
| t _{SU-STA} | Setup time for repeated START | | 4.7 | | 0.6 | | μs |
| t _{SU-DAT} | Data setup time | | 250 | | 100 | | μs |
| t _{HD-DAT} | Data hold time ⁽²⁾ ⁽³⁾ | | 0 | 3.45 | 0 | 0.9 | μs |
| t _r | Rise time of both SDA and SCL signals | | | 1000 | 20 + 0.1 C _b ⁽⁴⁾ | 300 | ns |
| t _f | Fall time of both SDA and SCL | | | 300 | 20 + 0.1 C _b ⁽⁴⁾ | 300 | ns |
| t _{SU-STO} | Setup time for STOP condition | | 4 | | 0.6 | | μs |
| t _{BUF} | Bus free time between a STOP and START condition | | 4.7 | | 1.3 | | μs |
| C _b | Capacitive load for each bus line | | | 400 | | 400 | pF |
| V _{nL} | Noise margin at the LOW level for each connected device (including hysteresis) | | 0.1V _{DVDD} | | 0.1V _{DVDD} | | V |
| V _{nH} | Noise margin at the HIGH level for each connected device (including hysteresis) | | 0.2V _{DVDD} | | 0.2V _{DVDD} | | V |

(1) In master mode, the maximum speed is 375 kHz.

(2) Note that SDA does not have the standard I²C specification 300-ns internal hold time. SDA must be valid by the rising and falling edges of SCL. TI recommends that a 2-kΩ pullup resistor be used to avoid potential timing issues.

(3) A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement t_{SU-DAT} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{r-max} + t_{SU-DAT} = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

(4) C_b = total capacitance of one bus line in pF

8.12 Reset Timing

control signal parameters over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|-------------------------|--|-----|-----|---------------|
| $t_{w(\text{RESET})}$ | Pulse duration, $\overline{\text{RESET}}$ active | 200 | | ns |
| $t_{r(\text{DMSTATE})}$ | Time to outputs inactive | | 100 | μs |
| $t_{r(\text{run})}$ | Time to enable I ² C | 50 | | ms |

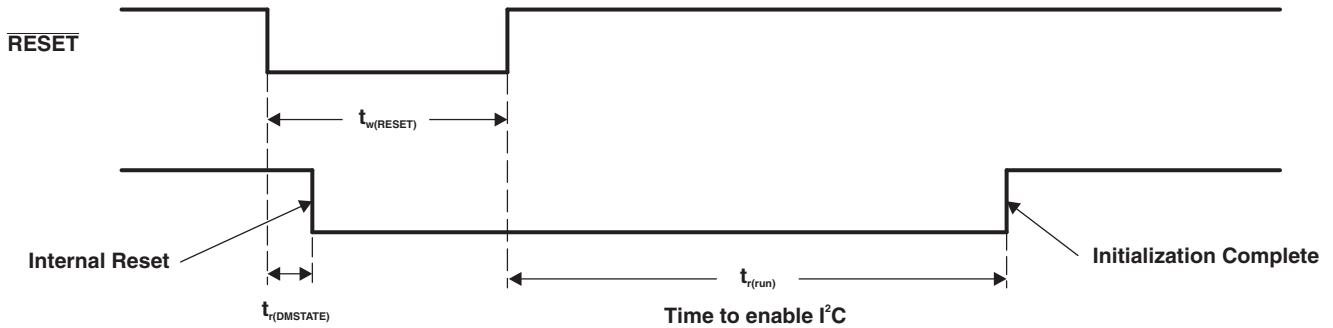


Figure 8-9. Reset Timing

9 I²C Register Map

I²C registers are also mapped to some of the Extended Special Function Registers (ESFRs). They are defined in the following sections.

Table 9-1. I²C Register Map

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | INITIALIZATION VALUE |
|------------|--------------------------------------|--------------|---|--|
| 0x00 | Clock Control Register | 4 | Description shown in Section 9.1 | 0x00, 0x40, 0x1B, 0x22 |
| 0x01 | Reserved | 4 | Reserved | 0x00, 0x00, 0x00, 0x40 |
| 0x02 | Status Register | 4 | Description shown in Section 9.2 | 0x00, 0x00, 0x03, 0xFF |
| 0x03 | Unused | | | 0x00, 0x00, 0x00, 0x00 |
| 0x04 | I ² C Memory Load Control | 8 | Description shown in Section 9.3 | 0x00, 0x00, 0x00, 0x00 0x00, 0x00, 0x00, 0x00 |
| 0x05 | I ² C Memory Load Data | 8 | Description shown in Section 9.3 | 0x00, 0x00, 0x00, 0x00 0x00, 0x00, 0x00, 0x00 |
| 0x06 | Memory Access Register 1 | 4 | u(31:24) ⁽¹⁾ , MemSelect(23:16), Addr(15:8), Addr(7:0) | 0x00, 0x00, 0x00, 0x00 |
| 0x07 | Memory Access Register 2 | 16 | D(63:56), D(55:48), D(47:40), D(39:32), D(31:24), D(23:16), D(15:8), D(7:0) | 0x00, 0x00, 0x00, 0x00 0x00, 0x00, 0x00, 0x00 |
| 0x08 | Device Version | 4 | TAS3202 version | 0x00, 0x00, 0x00, 0x01 |
| 0x09 | Unused | Unused | Unused | Unused |
| 0x10 | Analog Power Down Control 1 | 4 | Analog Power Down Control 1 | 0x00, 0x00, 0x00, 0x1F |
| 0x11 | Analog Power Down Control 2 | 4 | Analog Power Down Control 2 | 0x00, 0x00, 0x00, 0xFF |
| 0x12 | Analog Input Control | 4 | Analog Input Control | 0x00, 0x00, 0x00, 0x01 |
| 0x13 | ADC Dynamic Element Matching | 4 | ADC Dynamic Element Matching | 0x00, 0x00, 0x00, 0x08 |
| 0x14 | Unused | 4 | Unused | 0x00, 0x00, 0x00, 0x00 |
| 0x15 | Unused | 4 | Unused | 0x00, 0x00, 0x00, 0x00 |
| 0x16 | Unused | | Unused | |
| 0x17 | ADC Current Control 1 | 4 | ADC Current Control 1 | 0x00, 0x00, 0x00, 0x00 |
| 0x18 | ADC Current Control 2 | 4 | ADC Current Control 2 | 0x00, 0x00, 0x00, 0x00 |
| 0x19 | Unused | 4 | Unused | |
| 0x1A | DAC Control 1 | 4 | DAC Control 1 | 0x00, 0x00, 0x00, 0x00 |
| 0x1B | DAC Control 2 | 4 | DAC Control 2 | 0x00, 0x00, 0x00, 0x00 |
| 0x1C | Unused | 4 | Analog Test Modes | 0x00, 0x00, 0x00, 0x00 |
| 0x1D | DAC Control 3 | 4 | DAC Modulator Dither | 0x00, 0x00, 0x00, 0x00 |
| 0x1E | ADC and DAC Reset | 4 | ADC/DAC Digital Reset | 0x00, 0x00, 0x00, 0x00 |
| 0x1F | Analog Input Gain Select | | Analog Input Gain Select | 0x00, 0x00, 0x00, 0x00 |
| 0x20 | Unused | 4 | Clock Delay Setting ADC | 0x00, 0x00, 0x00, 0x00 |
| 0x21 | MCLK_OUT2 Divider | 4 | MCLK_OUT2 Divider | 0x00, 0x00, 0x00, 0x05 |
| 0x22 | MCLK_OUT3 Divider | 4 | MCLK_OUT3 Divider | 0x00, 0x00, 0x00, 0x00 |
| 0x30–0x3F | Digital Cross Bar | 32 | Digital Cross Bar | See Section 9.14 |

(1) u indicates unused bits.

In the following sections, **BOLD** indicates the default state of the bit fields.

9.1 Clock Control Register (0x00)

Register 0x00 provides the user with control over MCLK, LRCLK, SCLKOUT1, SCLKOUT2, data-word size, and serial audio port modes. Register 0x00 default = **0x00 00 1B 22**.

Table 9-2. Clock Control Register (0x00)

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | DESCRIPTION |
|-----|-----|-----|-----|-----|-----|-----|-----|-------------------------------|
| – | – | – | – | – | – | – | – | Firmware definable |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | DESCRIPTION |
| – | 1 | – | – | – | – | – | – | Master Mode (XTAL) |
| – | 0 | – | – | – | – | – | – | Slave mode (MCLK_IN) |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | DESCRIPTION |
| – | – | – | – | – | – | 0 | 0 | Output SAP 32-bit word |
| – | – | – | – | – | – | 0 | 1 | Output SAP 16-bit word |
| – | – | – | – | – | – | 1 | 0 | Output SAP 20-bit word |
| – | – | – | – | – | – | 1 | 1 | Output SAP 24-bit word |
| – | – | – | 0 | 0 | – | – | – | Input SAP 32-bit word |
| – | – | – | 0 | 1 | – | – | – | Input SAP 16-bit word |
| – | – | – | 1 | 0 | – | – | – | Input SAP 20-bit word |
| – | – | – | 1 | 1 | – | – | – | Input SAP 24-bit word |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
| IM3 | IM2 | IM1 | IM0 | | | | | Input data format |
| | | | | OM3 | OM2 | OM1 | OM0 | Output data format |

9.2 Status Register (0x02)

During I²C download, the write operation to indicate that a particular memory is to be written causes the TAS3202 to set an error bit to indicate a load for that memory type. This error bit is cleared when the operation completes successfully.

Table 9-3. Status Register (0x02)

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | DESCRIPTION |
|----------|----------|----------|----------|----------|----------|----------|----------|--|
| – | – | – | – | – | – | – | – | Firmware definable |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | DESCRIPTION |
| – | – | – | – | – | – | – | – | Firmware definable |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | DESCRIPTION |
| – | – | – | – | – | – | – | – | Firmware definable |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
| 0 | 0 | – | – | – | – | – | 1 | Microprocessor program memory load error |
| 0 | 0 | – | – | – | – | 1 | – | Microprocessor external data memory load error |
| 0 | 0 | – | – | – | 1 | – | – | Audio DSP core program memory load error |
| 0 | 0 | – | – | 1 | – | – | – | Audio DSP core upper coefficient memory load error |
| 0 | 0 | – | 1 | – | – | – | – | Audio DSP core upper data memory load error |
| 0 | 0 | 1 | – | – | – | – | – | Invalid memory select |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | End-of-load header error |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | N, IC sampling clock is 33 MHz divided by 2N |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | No errors |

9.3 I²C Memory Load Control and Memory Load Data Registers (0x04 and 0x05)

Registers 0x04 (Table 9-4) and 0x05 (Table 9-5) allow the user to download TAS3202 program code and data directly from the system I²C controller. This mode is called the I²C slave mode (from the TAS3202 point of view). See the *TAS3xxx Firmware Programmer's Guide* for more details.

The I²C slave memory load port permits the system controller to load the TAS3202 memories as an alternative to having the TAS3202 load its memory from EEPROM.

- Micro program memory
- Micro extended memory
- DAP program memory
- DAP coefficient memory
- DAP data memory

The transfer is performed by writing to two I²C registers. The first register is an 8-byte register that holds the checksum, the memory to be written, the starting address, the number of data bytes to be transferred. The second location holds 8 bytes of data. The memory load operation starts with the first register being set. Then the data is written into the second register using the format shown. After the last data byte is written into the second register, an additional two bytes are written that contain the 2-byte checksum. At that point, the transfer is complete and status of the operation is reported in the status register. The end checksum is always contained in the last two bytes of the data block.

Table 9-4. TAS3202 Memory Load Control Register (0x04)

| BYTE | DATA BLOCK FORMAT | SIZE | NOTES |
|------|--|---------|---|
| 1–2 | Checksum code | 2 bytes | Checksum of bytes 2 through N + 8. If this is a termination header, this value is 00 00. |
| 3–4 | Memory to be loaded | 2 bytes | 0: Microprocessor program memory 1: Microprocessor external data memory 2: Audio DSP core program memory 3: Audio DSP core coefficient memory 4: Audio DSP core data memory 5: Audio DSP core upper data memory 6: Audio DSP core upper coefficient memory 7–15: Reserved for future expansion |
| 5 | Unused | 1 byte | Reserved for future expansion |
| 6–7 | Starting TAS3202 memory address | 2 bytes | If this is a termination header, this value is 0000. |
| 7–8 | Number of data bytes to be transferred | 2 bytes | If this is a termination header, this value is 0000. |

Table 9-5. TAS3202 Memory Load Data Register (0x05)

| BYTE | 8-BIT DATA | 28-BIT DATA | 48-BIT DATA | 54-BIT DATA |
|------|---------------|--------------|-------------|-------------|
| 1 | Datum 1 D7–D0 | 0000 D27–D24 | 0000 0000 | 0000 0000 |
| 2 | Datum 2 D7–D0 | D7–D0 | 0000 0000 | 00 D53–D48 |
| 3 | Datum 3 D7–D0 | D15–D8 | D47–D40 | D47–D40 |
| 4 | Datum 4 D7–D0 | D7–D0 | D39–D32 | D39–D32 |
| 5 | Datum 5 D7–D0 | 0000 D27–D24 | D31–D24 | D31–D24 |
| 6 | Datum 6 D7–D0 | D23–D16 | D23–D16 | D23–D16 |
| 7 | Datum 7 D7–D0 | D15–D8 | D15–D8 | D15–D8 |
| 8 | Datum 8 D7–D0 | D7–D0 | D7–D0 | D7–D0 |

9.4 Memory Access Registers (0x06 and 0x07)

Registers 0x06 (Table 9-6) and 0x07 (Table 9-7) allow the user to access the internal resources of the TAS3202.

Table 9-6. Memory Select and Address Register (0x06)

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | DESCRIPTION |
|-----|-----|-----|-----|-----|-----|-----|-----|--|
| – | – | – | – | – | – | – | – | Unused |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | DESCRIPTION |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Audio DSP core coefficient memory select |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Audio DSP core data memory select |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Reserved |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Microprocessor internal data memory select |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | Microprocessor external data memory select |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | SFR select |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | Microprocessor program RAM select |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Audio DSP core program RAM select |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | Audio DSP core upper memory select |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | Audio DSP core program RAM select |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | DESCRIPTION |
| A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | Memory address |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
| A8 | A9 | A10 | A11 | A12 | A13 | A14 | A15 | Memory address |

Table 9-7. Data Register (Peek and Poke) (0x07)

| D63 | D62 | D61 | D60 | D59 | D58 | D57 | D56 | DESCRIPTION |
|-----|-----|-----|-----|-----|-----|-----|-----|----------------------------|
| D63 | D62 | D61 | D60 | D59 | D58 | D57 | D56 | Data to be written or read |
| D55 | D54 | D53 | D52 | D51 | D50 | D49 | D48 | DESCRIPTION |
| D55 | D54 | D53 | D52 | D51 | D50 | D49 | D48 | Data to be written or read |
| D47 | D46 | D45 | D44 | D43 | D42 | D41 | D40 | DESCRIPTION |
| D47 | D46 | D45 | D44 | D43 | D42 | D41 | D40 | Data to be written or read |
| D39 | D38 | D37 | D36 | D35 | D34 | D33 | D32 | DESCRIPTION |
| D39 | D38 | D37 | D36 | D35 | D34 | D33 | D32 | Data to be written or read |
| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | DESCRIPTION |
| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | Data to be written or read |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | DESCRIPTION |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | Data to be written or read |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | DESCRIPTION |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | Data to be written or read |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Data to be written or read |

9.5 Device Version (0x08)

Table 9-8. Device Version

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | DESCRIPTION |
|-----|-----|-----|-----|-----|-----|-----|-----|------------------------|
| – | – | – | – | – | – | – | – | Firmware definable |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | DESCRIPTION |
| – | – | – | – | – | – | – | – | Firmware definable |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | DESCRIPTION |
| – | – | – | – | – | – | – | – | Firmware definable |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | TAS3202 device version |

9.6 Analog Power Down Control (0x10 and 0x11)

Table 9-9. Analog Power Down Control 1 (0x10)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|------------------------------|
| – | – | – | – | – | – | – | 1 | Central reference enable |
| – | – | – | – | – | – | – | 0 | Power down central reference |
| – | – | – | – | – | – | 1 | – | ADC enable |
| – | – | – | – | – | – | 0 | – | ADC power down |
| – | – | – | – | – | 1 | – | – | Not used |
| – | – | – | – | – | 0 | – | – | Not used |
| – | – | – | – | 1 | – | – | – | ADC reference enable |
| – | – | – | – | 0 | – | – | – | ADC reference power down |
| – | – | – | 1 | – | – | – | – | DAC reference enable |
| – | – | – | 0 | – | – | – | – | DAC reference power down |

Table 9-10. Analog Power Down Control 2 (0x11)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|---------------------------|
| – | – | – | – | – | – | – | 1 | DAC left enable |
| – | – | – | – | – | – | – | 0 | DAC left power down |
| – | – | – | – | – | – | 1 | – | DAC right enable |
| – | – | – | – | – | – | 0 | – | DAC right power down |
| – | – | – | – | – | 1 | – | – | Not used |
| – | – | – | – | – | 0 | – | – | Not used |
| – | – | – | – | 1 | – | – | – | Not used |
| – | – | – | – | 0 | – | – | – | Not used |
| – | – | – | 1 | – | – | – | – | Line out left enable |
| – | – | – | 0 | – | – | – | – | Line out left power down |
| – | – | 1 | – | – | – | – | – | Line out right enable |
| – | – | 0 | – | – | – | – | – | Line out right power down |
| – | 1 | – | – | – | – | – | – | Not used |
| – | 0 | – | – | – | – | – | – | Not used |
| 1 | – | – | – | – | – | – | – | Not used |
| 0 | – | – | – | – | – | – | – | Not used |

9.7 Analog Input Control (0x12)

Table 9-11. Analog Input Control

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|------------------------|
| – | – | – | – | – | – | – | 0 | – |
| – | – | – | – | – | – | – | 1 | Select input 1 to ADC |
| – | – | – | – | – | – | 0 | – | – |
| – | – | – | – | – | – | 1 | – | Not used |
| – | – | – | – | – | 0 | – | – | – |
| – | – | – | – | – | 1 | – | – | Select input 2 to ADC |
| – | – | – | – | 0 | – | – | – | – |
| – | – | – | – | 1 | – | – | – | Not used |
| – | – | – | 0 | – | – | – | – | – |
| – | – | – | 1 | – | – | – | – | Not used |
| – | – | 0 | – | – | – | – | – | – |
| – | – | 1 | – | – | – | – | – | Not used |
| – | 0 | – | – | – | – | – | – | ADC differential input |
| – | 1 | – | – | – | – | – | – | ADC single ended input |
| 0 | – | – | – | – | – | – | – | Not used |
| 1 | – | – | – | – | – | – | – | Not used |

9.8 ADC Dynamic Element Matching (0x13)

Table 9-12. Dynamic Element Matching

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|--|
| – | – | – | – | – | – | – | 0 | ADC dynamic element matching algorithm enabled (recommended setting) |
| – | – | – | – | – | – | – | 1 | ADC dynamic element matching algorithm disabled |
| – | – | – | – | – | – | 0 | – | Dynamic weighted averaging enabled (recommended setting) |
| – | – | – | – | – | – | 1 | – | Dynamic weighted averaging disabled |
| – | – | – | – | – | 0 | – | – | Unused |
| – | – | – | – | – | 1 | – | – | Unused |
| – | – | – | – | 0 | – | – | – | Fast charge of cap on VREF (filtering disabled – recommended setting at startup) |
| – | – | – | – | 1 | – | – | – | Slow charge of cap on VREF (filtering enabled – recommended setting during normal operation) |
| – | – | – | 0 | – | – | – | – | Unused |
| – | – | – | 1 | – | – | – | – | Unused |
| – | – | 0 | – | – | – | – | – | Unused |
| – | – | 1 | – | – | – | – | – | Unused |
| – | 0 | – | – | – | – | – | – | Unused |
| – | 1 | – | – | – | – | – | – | Unused |
| 0 | – | – | – | – | – | – | – | Unused |
| 1 | – | – | – | – | – | – | – | Unused |

9.9 ADC Current Control Select (0x17, 0x18)

Table 9-13. Current Control Select (0x17)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|--|
| – | – | – | – | – | – | 0 | 0 | ADC summer current setting (left and right) = 130% of nominal current (Recommended Setting) |
| – | – | – | – | – | – | 0 | 1 | ADC summer current setting (left and right) = 100% of nominal current |
| – | – | – | – | – | – | 1 | 0 | ADC summer current setting (left and right) = 100% of nominal current |
| – | – | – | – | – | – | 1 | 1 | ADC summer current setting (left and right) = 70% of nominal current |
| – | – | – | – | 0 | 0 | – | – | ADC quantizer current setting (left and right) = 137.5% of nominal current (recommended setting) |
| – | – | – | – | 0 | 1 | – | – | ADC quantizer current setting (left and right) = 100% of nominal current |
| – | – | – | – | 1 | 0 | – | – | ADC quantizer current setting (left and right) = 100% of nominal current |
| – | – | – | – | 1 | 1 | – | – | ADC quantizer current setting (left and right) = 62.5% of nominal current |
| – | – | 0 | 0 | – | – | – | – | ADC third integrator current setting (left and right) = 130% of nominal current (Recommended Setting) |
| – | – | 0 | 1 | – | – | – | – | ADC third integrator current setting (left and right) = 100% of nominal current |
| – | – | 1 | 0 | – | – | – | – | ADC third integrator current setting (left and right) = 100% of nominal current |
| – | – | 1 | 1 | – | – | – | – | ADC third integrator current setting (left and right) = 70% of nominal current |
| 0 | 0 | – | – | – | – | – | – | ADC reference buffer current setting (left and right) = 130% of nominal current (Recommended Setting) |
| 0 | 1 | – | – | – | – | – | – | ADC reference buffer current setting (left and right) = 100% of nominal current |
| 1 | 0 | – | – | – | – | – | – | ADC reference buffer current setting (left and right) = 100% of nominal current |
| 1 | 1 | – | – | – | – | – | – | ADC reference buffer current setting (left and right) = 70% of nominal current |

Table 9-14. Current Control Select (0x18)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|--|
| – | – | – | – | – | – | 0 | 0 | ADC second integrator current setting (left and right) = 130% of nominal current (recommended setting) |
| – | – | – | – | – | – | 0 | 1 | ADC second integrator current setting (left and right) = 100% of nominal current |
| – | – | – | – | – | – | 1 | 0 | ADC second integrator current setting (left and right) = 100% of nominal current |
| – | – | – | – | – | – | 1 | 1 | ADC second integrator current setting (left and right) = 70% of nominal current |
| – | – | – | – | 0 | 0 | – | – | ADC second integrator current setting (left and right) = 130% of nominal current (recommended setting) |
| – | – | – | – | 0 | 1 | – | – | ADC first integrator current setting (left and right) = 100% of nominal current |
| – | – | – | – | 1 | 0 | – | – | ADC first integrator current setting (left and right) = 100% of nominal current |
| – | – | – | – | 1 | 1 | – | – | ADC first integrator current setting (left and right) = 70% of nominal current |
| – | – | 0 | 0 | – | – | – | – | ADC current for common mode buffer to integrator 1 = 3.5 μ A |
| – | – | 0 | 1 | – | – | – | – | ADC current for common mode buffer to integrator 1 = 2.0 μ A |
| – | – | 1 | 0 | – | – | – | – | ADC current for common mode buffer to integrator 2 and 3 = 3.5 μ A |
| – | – | 1 | 1 | – | – | – | – | ADC current for common mode buffer to integrator 2 and 3 = 2.0 μ A |
| 0 | 0 | – | – | – | – | – | – | ADC current for the buffer to the ADC sampling switches = 3.5 μ A |
| 0 | 1 | – | – | – | – | – | – | ADC current for the buffer to the ADC sampling switches = 2.0 μ A |
| 1 | 0 | – | – | – | – | – | – | ADC current for the reference buffer to the ADC DAC = 3.5 μ A |
| 1 | 1 | – | – | – | – | – | – | ADC current for the reference buffer to the ADC DAC = 2.0 μ A |

9.10 DAC Control (0x1A, 0x1B, 0x1D)
Table 9-15. DAC Control (0x1A)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|--|
| – | – | – | – | – | – | 0 | 0 | DAC current control for DAC local reference block and lineout amps = default (recommended setting) |
| – | – | – | – | – | – | 0 | 1 | DAC current control for DAC local reference block and lineout amps = 125% bias current |
| – | – | – | – | – | – | 1 | 0 | DAC current control for DAC local reference block and lineout amps = 75% bias current |
| – | – | – | – | – | – | 1 | 1 | DAC current control for DAC local reference block and lineout amps = 75% bias current |
| – | – | – | – | 0 | 0 | – | – | Not used |
| – | – | – | – | 0 | 1 | – | – | Not used |
| – | – | – | – | 1 | 0 | – | – | Not used |
| – | – | – | – | 1 | 1 | – | – | Not used |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |

Table 9-16. DAC Control (0x1B)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|--------------------------------------|
| – | – | – | – | – | – | – | 0 | DAC chopper stabilization disable |
| – | – | – | – | – | – | – | 1 | DAC chopper stabilization enable |
| – | – | – | – | – | – | 0 | – | Not used |
| – | – | – | – | – | – | 1 | – | Not used |
| – | – | – | – | – | 0 | – | – | DC offset subtraction in DAC disable |
| – | – | – | – | – | 1 | – | – | DC offset subtraction in DAC enable |
| – | – | – | – | 0 | – | – | – | Connected to microprocessor SDA2 |
| – | – | – | – | 1 | – | – | – | |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |

Table 9-17. DAC Control (0x1D)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|--|
| – | – | – | – | – | – | 0 | 0 | DAC current control for DAC local reference block and lineout amps = default (recommended setting) |
| – | – | – | – | – | – | 0 | 1 | DAC current control for DAC local reference block and lineout amps = 125% bias current |
| – | – | – | – | – | – | 1 | 0 | DAC current control for DAC local reference block and lineout amps = 75% bias current |
| – | – | – | – | – | – | 1 | 1 | DAC current control for DAC local reference block and lineout amps = 75% bias current |
| – | – | – | – | 0 | 0 | – | – | Not used |
| – | – | – | – | 0 | 1 | – | – | Not used |
| – | – | – | – | 1 | 0 | – | – | Not used |
| – | – | – | – | 1 | 1 | – | – | Not used |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – |

9.11 ADC and DAC Reset (0x1E)

Table 9-18. ADC and DAC Reset (0x1E)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|---------------------|
| – | – | – | – | – | – | – | 0 | – |
| – | – | – | – | – | – | – | 1 | ADC reset channel 1 |
| – | – | – | – | – | – | 0 | – | – |
| – | – | – | – | – | – | 1 | – | ADC reset channel 2 |
| – | – | – | – | – | 0 | – | – | – |
| – | – | – | – | – | 1 | – | – | Not used |
| – | – | – | – | 0 | – | – | – | – |
| – | – | – | – | 1 | – | – | – | Not used |
| – | – | – | 0 | – | – | – | – | – |
| – | – | – | 1 | – | – | – | – | DAC reset channel 1 |
| – | – | 0 | – | – | – | – | – | – |
| – | – | 1 | – | – | – | – | – | DAC reset channel 2 |
| – | 0 | – | – | – | – | – | – | – |
| – | 1 | – | – | – | – | – | – | Not used |
| 0 | – | – | – | – | – | – | – | – |
| 1 | – | – | – | – | – | – | – | Not used |

9.12 ADC Input Gain Control (0x1F)

Table 9-19. ADC Input Gain Control (0x1F)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|--|
| – | – | – | – | – | – | 0 | 0 | Channel 1Sinc input gain control = 0 dB |
| – | – | – | – | – | – | 0 | 1 | Channel 1Sinc input gain control = +30 dB |
| – | – | – | – | – | – | 1 | 0 | Channel 1Sinc input gain control = +600 dB |
| – | – | – | – | – | – | 1 | 1 | Channel 1Sinc input gain control = 0 dB |
| – | – | – | – | 0 | 0 | – | – | Channel 2Sinc input gain control = 0 dB |
| – | – | – | – | 0 | 1 | – | – | Channel 2Sinc input gain control = +30 dB |
| – | – | – | – | 1 | 0 | – | – | Channel 2Sinc input gain control = +60 dB |
| – | – | – | – | 1 | 1 | – | – | Channel 2Sinc input gain control = 0 dB |
| – | – | 0 | 0 | – | – | – | – | Not used |
| – | – | 0 | 1 | – | – | – | – | Not used |
| – | – | 1 | 0 | – | – | – | – | Not used |
| – | – | 1 | 1 | – | – | – | – | Not used |
| 0 | 0 | – | – | – | – | – | – | Not used |
| 0 | 1 | – | – | – | – | – | – | Not used |
| 1 | 0 | – | – | – | – | – | – | Not used |
| 1 | 1 | – | – | – | – | – | – | Not used |

9.13 MCLK_OUT Divider (0x21 and 0x22)

Table 9-20. MCLK_OUT 2 (0x21)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|--|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | MCLK_OUT2 frequency is 6.144 MHz/(divider+1) |

Table 9-21. MCLK_OUT 3 (0x22)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|--|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MCLK_OUT3 frequency is 512 kHz/(divider+1) |

9.14 Digital Cross Bar (0x30 to 0x3F)

Table 9-22. Digital Cross Bar (0x30 to 0x3F)

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | INITIALIZATION VALUE |
|------------|-----------------|--------------|---------------------|--|
| 0x30 | CH1 Input Mixer | 32 | Input cross bar mux | 0x08 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 |
| 0x31 | CH2 Input Mixer | 32 | Input cross bar mux | 0x00 00 00 00 0x08 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 |
| 0x32 | CH3 Input Mixer | 32 | Input cross bar mux | 0x00 00 00 00 0x00 00 00 00 0x08 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 |
| 0x33 | CH4 Input Mixer | 32 | Input cross bar mux | 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x08 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 |
| 0x34 | CH5 Input Mixer | 32 | Input cross bar mux | 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x08 00 00 00 0x00 00 00 00 0x00 00 00 00 |

Table 9-22. Digital Cross Bar (0x30 to 0x3F) (continued)

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | INITIALIZATION VALUE |
|------------|------------------|--------------|----------------------|---|
| 0x35 | CH6 Input Mixer | 32 | Input cross bar mux | 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x08 00 00 00 0x00 00 00 00 0x00 00 00 00 |
| 0x36 | Reserved | 32 | Reserved | 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x08 00 00 00 0x00 00 00 00 |
| 0x37 | Reserved | 32 | Reserved | 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x08 00 00 00 |
| 0x38 | CH1 Output Mixer | 32 | Output cross bar mux | 0x08 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 |
| 0x39 | CH2 Output Mixer | 32 | Output cross bar mux | 0x00 00 00 00 0x08 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 |
| 0x3A | CH3 Output Mixer | 32 | Output cross bar mux | 0x00 00 00 00 0x00 00 00 00 0x08 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 |
| 0x3B | CH4 Output Mixer | 32 | Output cross bar mux | 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x08 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 |
| 0x3C | CH5 Output Mixer | 32 | Output cross bar mux | 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x08 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 |

Table 9-22. Digital Cross Bar (0x30 to 0x3F) (continued)

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | INITIALIZATION VALUE |
|------------|------------------|--------------|----------------------|---|
| 0x3D | CH6 Output Mixer | 32 | Output cross bar mux | 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x08 00 00 00 0x00 00 00 00 0x00 00 00 00 |
| 0x3E | Reserved | 32 | Reserved | 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x08 00 00 00 0x00 00 00 00 |
| 0x3F | Reserved | 32 | Reserved | 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x00 00 00 00 0x08 00 00 00 |

10 Application Information

10.1 Schematics

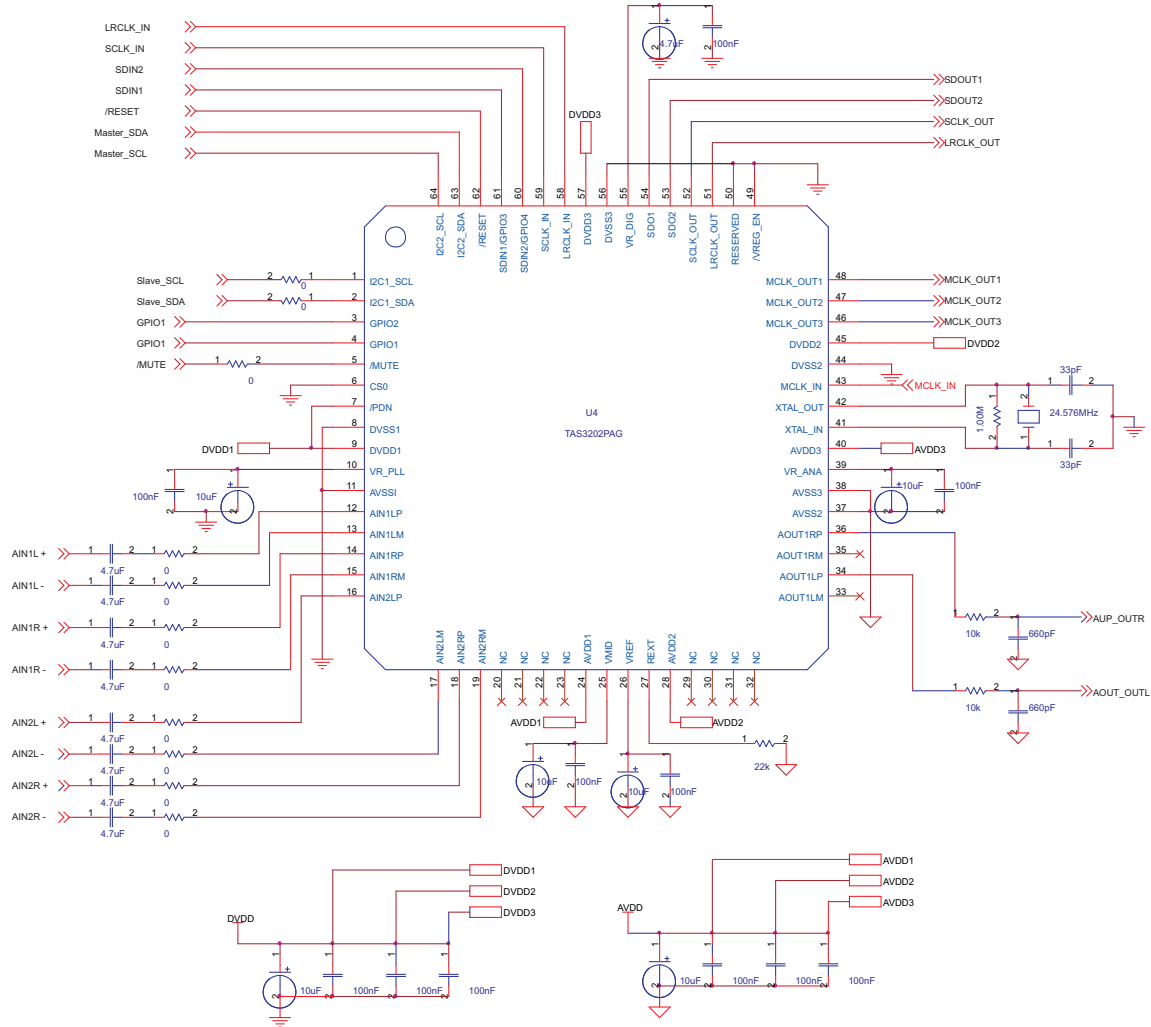
Figure 10-1 shows a typical TAS3202 application. In this application, the following conditions apply:

- TAS3202 is in clock-master mode. The TAS3202 generates MCLK_OUT1, SCLK_OUT, and LRCLOCK_OUT.
- XTAL_IN = 24.576 MHz
- I²C register 0x00 contains the default settings, which means:
 - Audio data word size is 24-bit input and 24-bit output.
 - Serial data format is 2-channel, I²S for input and output.
 - I²C data transfer is approximately 400 kbps for both master and slave I²C interfaces.
 - Sample frequency (f_s) is 48 kHz, which means that $f_{LRCLK} = 48$ kHz and $f_{SCLKIN} = 3.072$ MHz.
- Application code and data are loaded from an external EEPROM using the master I²C interface.
- Application commands come from the system microprocessor to the TAS3202 using the slave I²C interface.

Good design practice requires isolation between the digital and analog power as shown. Power-supply capacitors of 10 μ F and 0.1 μ F should be placed near the power supply pins AVDD (AVSS) and DVDD (DVSS).

The TAS3202 reset needs external glitch protection. Also, $\overline{\text{RESET}}$ going HIGH should be delayed until TAS3202 internal power is good (~ 200 μ s after power up). This is provided by the 1-k Ω resistor, 1- μ F capacitor, and diode placed near the $\overline{\text{RESET}}$ pin.

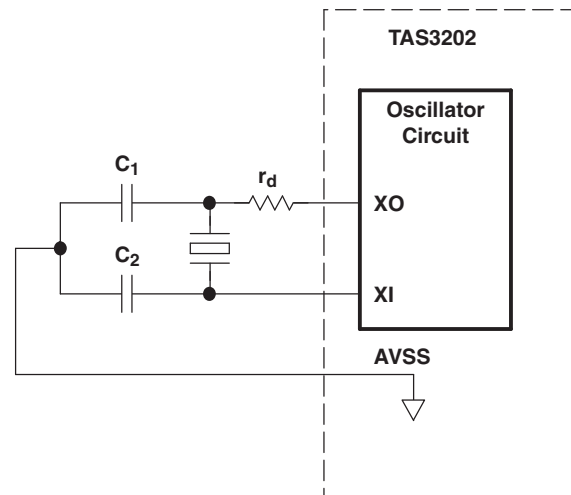
It is recommended that a 4.7- μ F capacitor (fast ceramic type) be placed near pin 28 (VR_DIG). This pin must not be used to source external components.



A. Capacitors should be placed as close as possible to the power supply pins.

Figure 10-1. Typical Application Diagram

10.2 Recommended Oscillator Circuit



- Crystal type = Parallel-mode, fundamental-mode crystal
- r_d = Drive-level control resistor – vendor specified
- C_L = Crystal load capacitance (capacitance of circuitry between the two terminals of the crystal)
- $C_L = (C_1 \times C_2) / (C_1 + C_2) + C_S$ (where C_S = board stray capacitance, ~2 pF)

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| TAS3202PAG | NRND | TQFP | PAG | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-4-260C-72 HR | |
| TAS3202PAGR | NRND | TQFP | PAG | 64 | 1500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-4-260C-72 HR | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

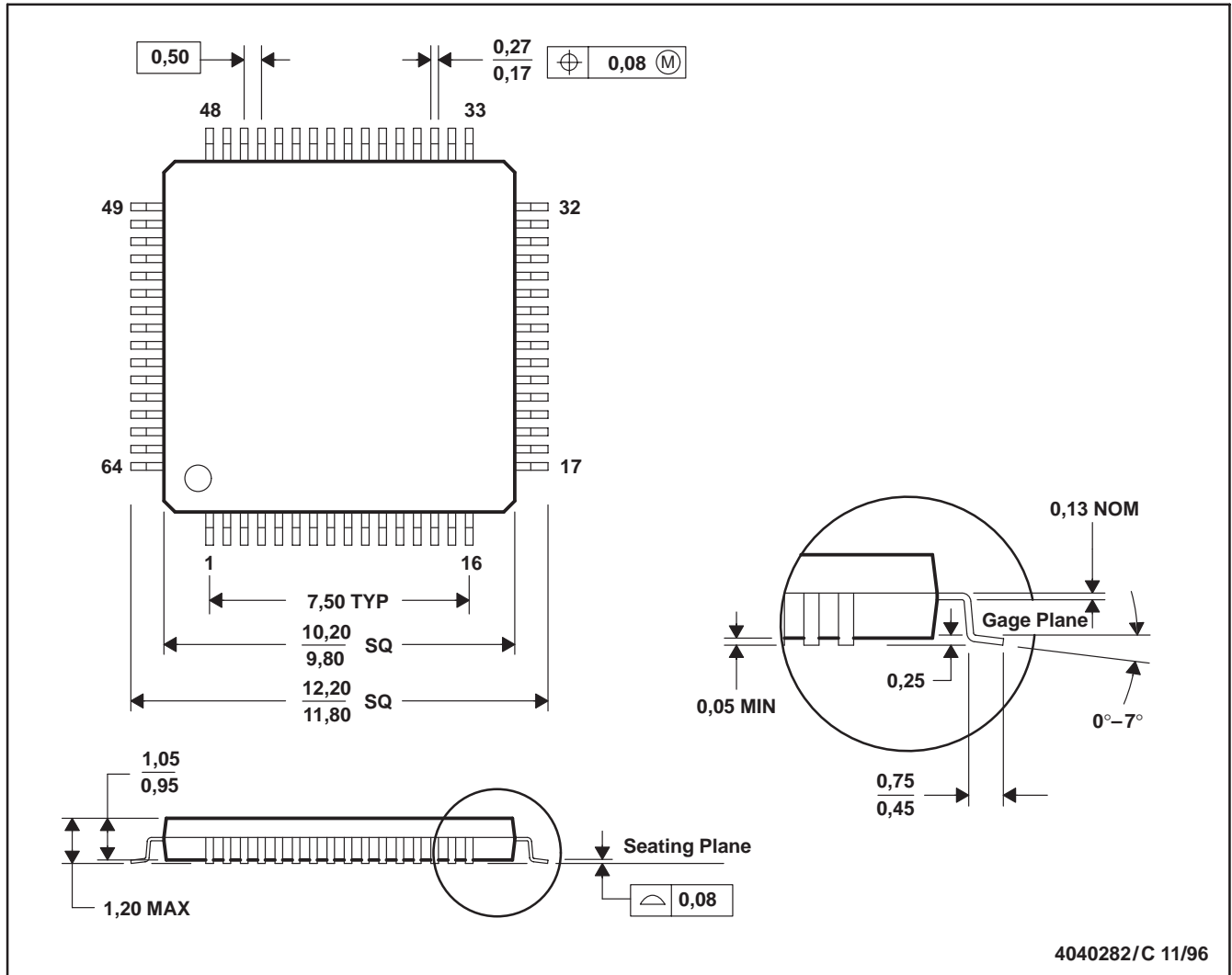
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PAG (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

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