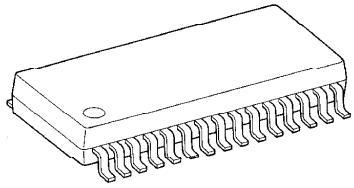
TENTATIVE TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8899AF

FM DEMODULATION IC FOR BROADCASTING SATELLITE RECEIVER

TA8899AF combines the necessary function on a single monolithic integrated circuit to modulate FM signal of the 2nd IF of DBS.



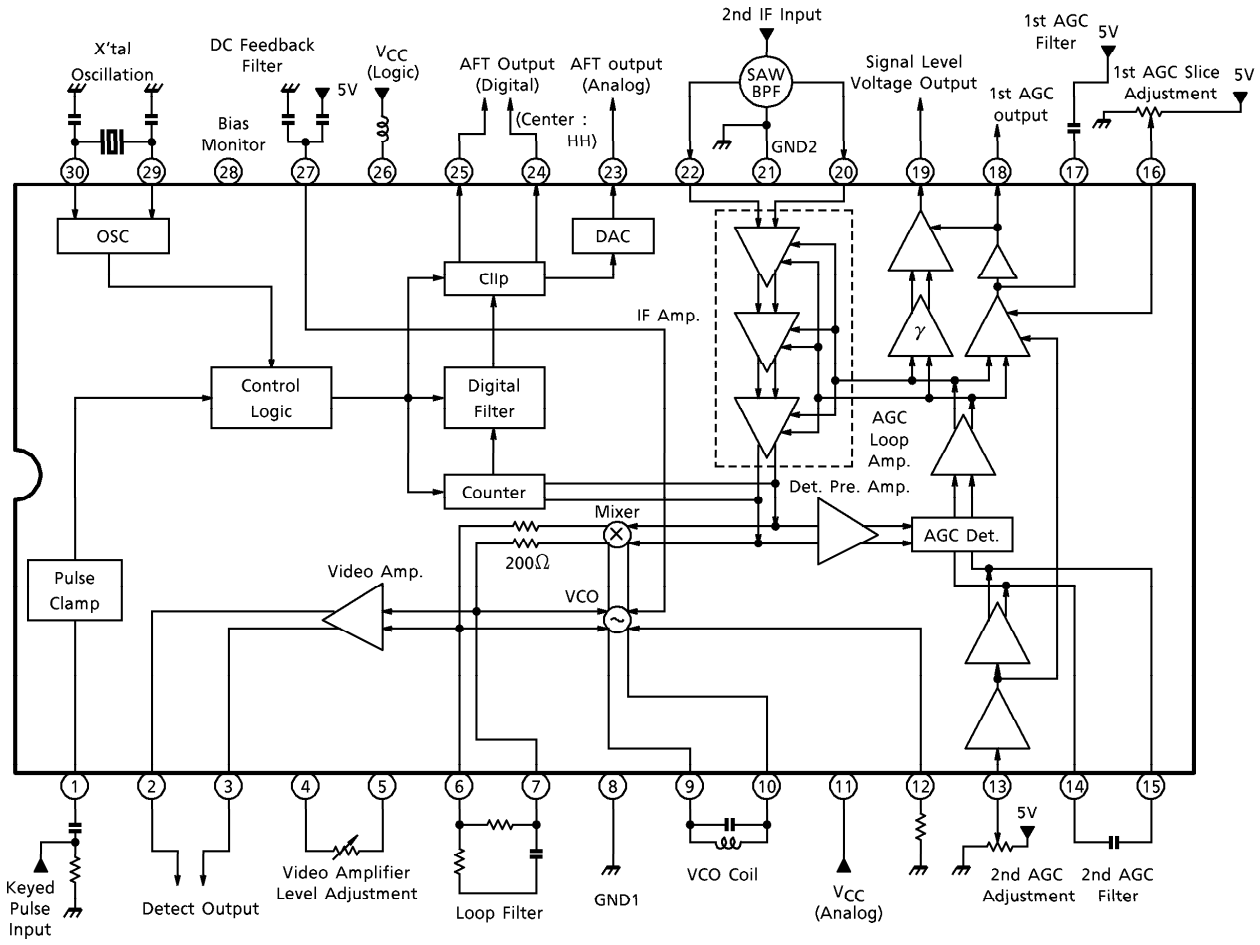
SSOP30-P-375-1.00

Weight : 0.63g (Typ.)

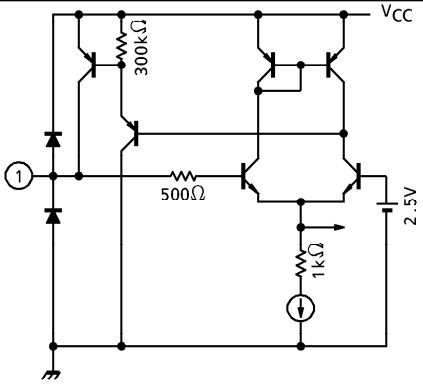
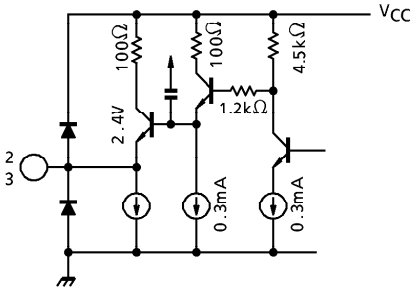
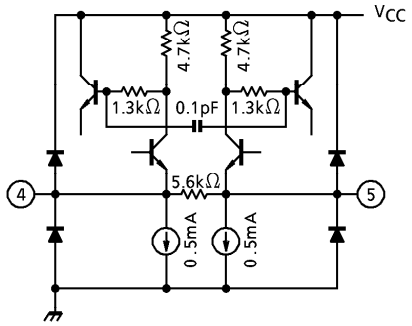
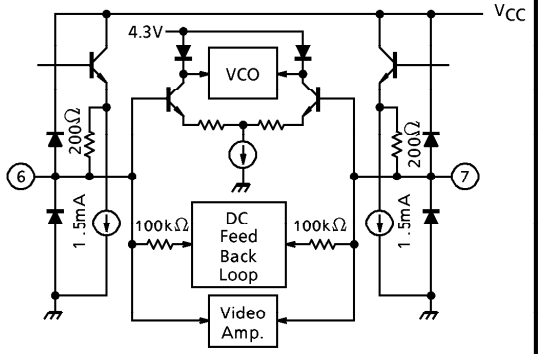
FEATURES

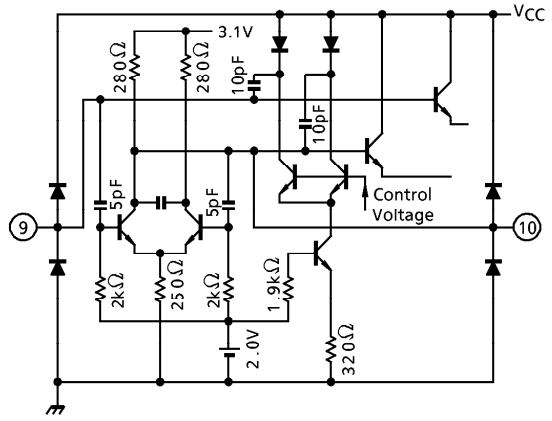
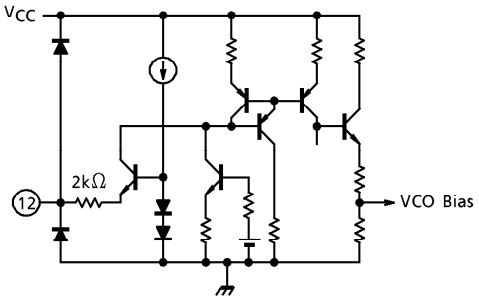
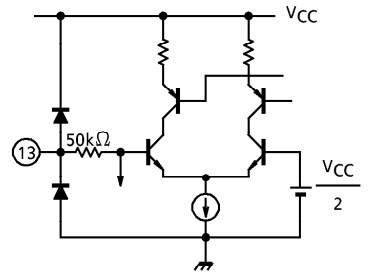
- 5V single power source
- 2nd IF AGC amplifier (AGC range 50dB or more)
- Logarithmic-linear type signal level amplifier
- PLL type FM detector (variable impedance built in)
- Adjustment free AFT circuit (IF frequency direct count type digital AFT) and also designed for keyed AFT system
- Output terminal of 1'st AGC control circuit

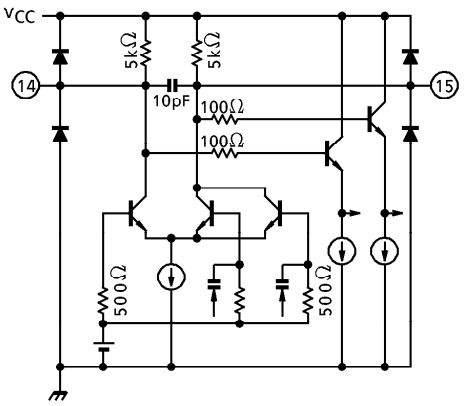
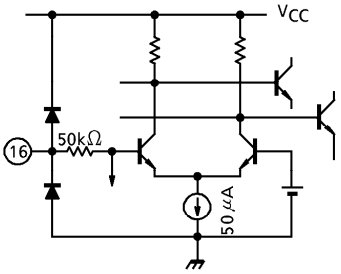
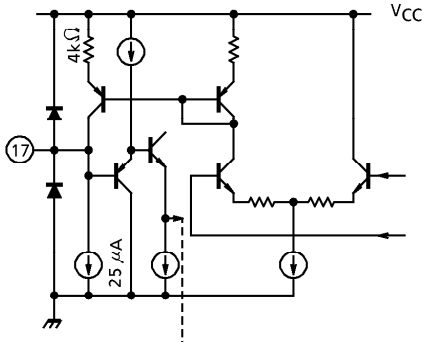
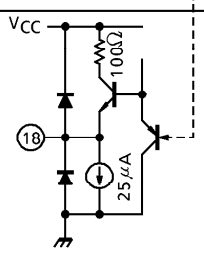
BLOCK DIAGRAM

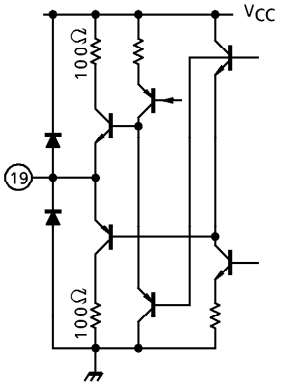
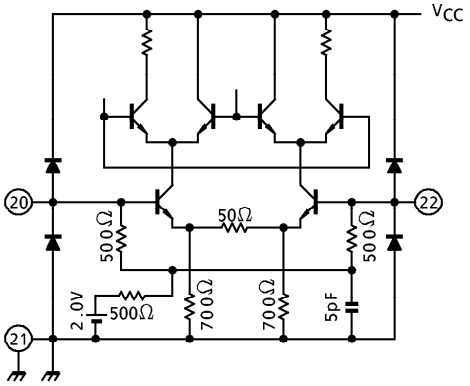
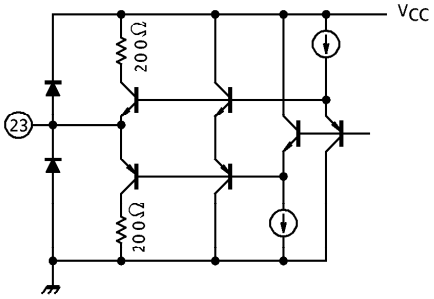


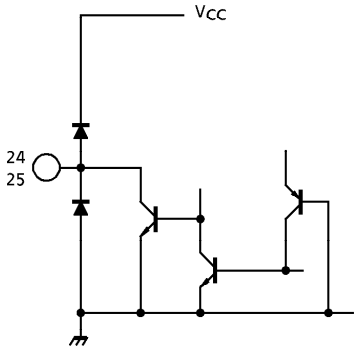
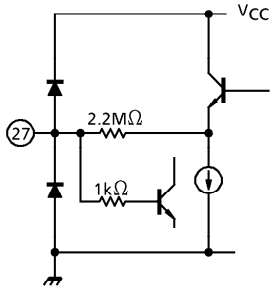
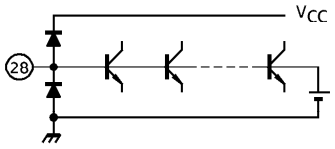
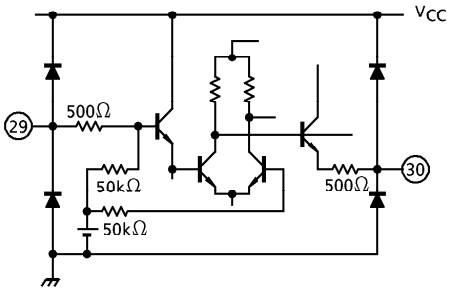
TERMINAL FUNCTION

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
1	Keyed Pulse Input	It clamps at the pulse peak and generates the reference level. The input impedance is 3kΩ.	
2 3	Detect Output	It outputs the detection output through a low-pass filter of 30MHz cut off frequency using an emitter follower.	
4 5	Video Amplifier Level Adjustment	It controls the level adjustment by varying the emitter resistor of a differential amplifier. If the resistor between pins 4 and 5 is reduced the output will be greater, however, since the output dynamic range is narrow the output level should be used in the range of lower than $0.7V_{p-p}$.	
6 7	Loop Filter	The output impedance is 200Ω.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
8	GND1	It is the GND of VCO circuit blocks that are VCO (pins 9, 10, 12), loop filter (pins 6, 7), video amplifier (pins 4, 5) AFT system (pins 1, 23, 24, 25, 26, 27, 28) and S/H (pins 29, 30).	—
9 10	VCO Coil	It is the VCO using variations in internal impedance of diode for control voltage from mixer. Use a UJ characteristic for the capacitor of the external tank circuit to correct the internal temperature drift.	
12	VCO Temperature Compensate Bias	The VCO bias is composed of a synthesis of bias in proportion to V_{BE} and V_T of transistor, and this terminal generates a bias proportioned to the V_{BE}. If the external resistor reduced, the VCO sensitivity will rise.	
13	2nd AGC Adjustment	It changes the input level for a AGC detector. It adjusts by adding the direct current off-set to pins 14 and 15. The variation width of about 8dB can be added. Internal bias is 2.5V.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
14 15	2nd AGC Filter	It generates the AGC voltage by filtering the 403MHz IF signal by means of an internal resistor and an external capacitor. If applying the V_{CC} to pin 15, the AGC will be minimum gain and the VCO oscillates at free-running frequency.	
16	1st AGC Slice Adjustment	It sets the input level threshold for generating the control signal to lower gain from the IC to the 2nd converter of front stage when excessive signal input. Even if the 2nd AGC adjustment varies, the 1st AGC adjustment point hardly changes. The internal bias is 2.5V.	
17	1st AGC Filter	It outputs by comparating with the AGC and 1st AGC slice level adjustment voltages. This comparator is constructed by the active load type high gain amplifier and determines its response by a capacitor connected to this terminal.	
18	1st AGC Control	It outputs the control voltage using an emitter follower (active low level). The internal current sink has only 25μA.	

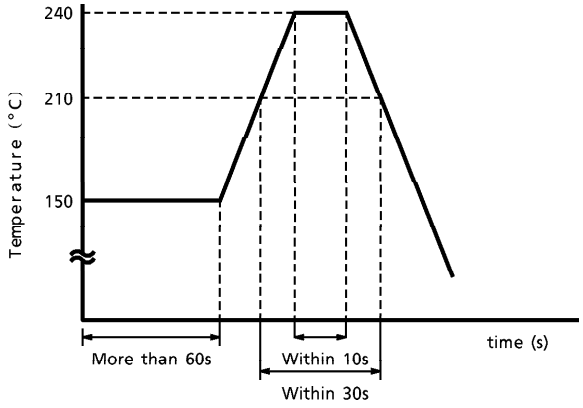
PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
19	Signal Level Voltage Output	It outputs the AGC voltage by doing logarithm <-> linear conversion. In the TA8899AF the level detection can be carried out even after the 1st AGC is effective and input is reduced using the 1st AGC output.	
20 22	2nd IF Input	The IF amplifier constructed by the 3-step series connection of variable gm type gain control, of which the maximum gain is 47dB and minimum gain −8dB. In order to prevent a sneak of radio frequency, all the circuits are balance-connected. Therefore, the differential combination is also desirable for the IC input. The internal bias is 2.0V and input impedance is 1kΩ.	
23	AFT Output (Analog)	This counts the IF frequency, averages the count data, carries out D/A conversion of the signal and outputs an AFT signal. X'tal is used for the reference signal of this AFT operation, so operation is stabilized against temperature fluctuation. Furthermore, an AFT signal is created from an IF signal, and so VCO oscillation is an independent operation.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
24 25	AFT Output (Digital)	These are high detection ("H" when the IF signal is high) and low detection ("H" when the IF signal is low). These shows both outputs is high when the input frequency is nearby 402.78MHz.	
26	V_{CC} (Logic Block)	To avoid interference of digital circuits and analog circuits connect to the power line through a 1μH inductor.	—
27	DC Feedback Filter	In order to correct the lag between the VCO's fo and the input's IF signal, the wave detection output's DC offset is used and a circuit installed which feeds this back to the VCO oscillation frequency. The low pass filter for detecting this DC offset is composed of an internal resistor and an external capacitor. (fc≒1Hz)	
28	Bias Monitor	This terminal monitors the bias of an internal logic circuit. Normally keep it open.	
29 30	X'tal Oscillation	This is the 4MHz X'tal oscillation terminal, the reference for internal digital operations. When supplying 4MHz OSC from other, please input to a 29 pin.	

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	$V_{CC\ MAX}$	6.0	V
Power Dissipation	$P_{D\ MAX}$	1000	mW
Operation Temperature	T_{opr}	−20~75	°C
Storage Temperature	T_{stg}	−55~150	°C
Lead Temperature	—	260°C, 10s	

Recommended assembly method : Recommended temperature profile of reflow soldering of far and medium infrared rays



RECOMMENDED POWER SUPPLY VOLTAGE

PIN No.	PIN NAME	MIN.	TYP.	MAX.	UNIT
11	V_{CC} (Analog)	4.75	5.0	5.25	V
26	V_{CC} (Logic)	4.75	5.0	5.25	V

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Unless otherwise specified, V_{CC} = 5.0V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current		I_{CC}	1	—	75	100	125	mA
Terminal Voltage	Pin 1	V_1	1	—	2.0	2.5	3.0	V
	Pin 2	V_2		—	1.5	2.0	2.5	
	Pin 3	V_3		—	1.5	2.0	2.5	
	Pin 4	V_4		—	0.8	1.3	1.8	
	Pin 5	V_5		—	0.8	1.3	1.8	
	Pin 6	V_6		—	2.2	2.7	3.2	
	Pin 7	V_7		—	2.2	2.7	3.2	
	Pin 9	V_9		—	2.2	2.7	3.2	
	Pin 10	V_{10}		—	2.2	2.7	3.2	
	Pin 12	V_{12}		1.8kΩ-GND	0.08	0.2	0.32	
	Pin 13	V_{13}		—	2.3	2.5	2.7	
	Pin 14	V_{14}		—	—	3.7	—	
	Pin 15	V_{15}		—	—	3.9	—	
	Pin 16	V_{16}		—	2.1	2.5	2.9	
	Pin 18	V_{18h}		Pin 17 : 1kΩ-GND	—	1.0	1.3	
		V_{18l}		Pin 17 : V_{CC}	3.9	4.3	4.7	
	Pin 20	V_{20}		—	1.5	2.0	2.5	
	Pin 22	V_{22}		—	1.5	2.0	2.5	
	Pin 28	V_{28}		—	1.8	2.2	2.6	
	Pin 29	V_{29}		—	2.3	2.7	3.0	
	Pin 30	V_{30}		—	2.3	2.7	3.0	
Pin 2, 3 Acceptable Output Current		I_2, I_3	1	—	−1.0	—	6.0	mA
1st AGC Output Current		I_{18}	1	—	−0.02	—	6.0	mA

AC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
IF Input Frequency Range	f_{in}	2	—	350	400	550	MHz
IF Input Level Range	v_{in}	2	—	– 50	—	– 10	dBmW
1st AGC Shoulder Level Range	AGC_{MAX}	2	Pin 16 = 2.5V	– 33	– 26	– 19	dBmW
1st AGC Control Sensitivity	ΔAGC	2	—	1.3	2.7	—	V / dB
Signal Level Sensitivity	$\Delta V / \Delta v$	2	—	50	100	150	mV / dB
VCO Conversion Sensitivity	β	2	—	60	80	110	MHz / V
VCO Temperature Drift	Δf_{Ta}	2	Ta = – 10~65°C	—	± 1.0	± 2.5	MHz
PLL Lock Range	f_L	2	—	± 20	± 30	—	MHz
PLL Capture Range	fc	2	—	± 20	± 30	—	MHz
Demodulation Output Level	V_{out}	2	$\Delta f = 10MHz_{p-p}$ Converting to output rate Pin 4, 5 : 2.4kΩ	0.35	0.50	0.65	V_{p-p}
Video Amplifier Variable Width	$v_{o\ S/5}$	2	Pin 4, 5 : short, 5kΩ	10	—	—	dB
Demodulation Output Amplitude Frequency Characteristics 1	$v_{o\ A1}$	2	f = 0.2~4MHz Reference : 100kHz	—	—	± 2	dB
Demodulation Output Amplitude Frequency Characteristics 2	$v_{o\ A2}$	2	f = 4~9MHz Reference : 100kHz	—	—	± 2	dB
Group Delay Characteristics 1	τ pd1	2	f = 0.2~4MHz Reference : 100kHz	—	—	± 10	ns
Group Delay Characteristics 2	τ pd2	2	f = 4~9MHz Reference : 100kHz	—	—	± 40	ns
Keyed AFT Input Range	v_1	2	—	0.35	0.5	0.65	V_{p-p}
Keyed AFT Input Frequency	T_1	2	—	8.0	16.7	50	ms
AFT Sensitivity	$\Delta f / \Delta V$	2	—	1.5	2.0	2.8	MHz / V
AFT Width of Dead Zone	V_{DEAD}	2	—	281	313	344	kHz
Digital AFT Voltage Low Level	V_{20L}	2	—	—	0.2	0.5	V
D G	DG	2	APL : 10~90%	—	± 2.0	± 3.0	%
D P	DP	2	APL : 10~90%	—	± 2.0	± 3.0	°
I M 2	IM2	2	2.15MHz beat level (*)	45	50	—	dB
I M 3	IM3	2	1.43MHz beat level (*)	45	50	—	dB
Video S / N	SN_{sat}	2	—	51	—	—	dB
External Input Level (4MHz Clock)	X_{in}	2	—	0.3	0.5	0.7	V_{p-p}
VCO Initial Drift	SWON	2	3~20s	0	—	850	kHz

(*) VCO coil must be adjusted to make IM2 / 3 best value

MEASUREMENT CONDITION

(Note 1) 1st AGC Shoulder Level Range : AGC_{MAX}

F = 402.78MHz input level v_{in} = 0 to − 40dBmW (50Ω) to pin 20. Measure v_{in} that pin 18 voltage is lower than 4V by opening pin 16 and raising v_{in}.

(Note 2) 1st AGC Control Sensitivity : ΔAGC

Input f = 402.78MHz v_{in} = 0 ~ − 40dBmW (50Ω) to pin 20. Calculate v_{in} that pin 18 voltage is 4V / 1V (as v_{in1}, v_{in2}), using the equation below.

$\Delta AGC = -3 / (v_{in1} - v_{in2})$ V / dB

(Note 3) Signal Level Sensitivity : ΔV / Δv

Measure each output voltage of pin 19 at v_{in} = − 40, − 60dBmW (50Ω)

$\Delta V / \Delta V = (V_{-60} - V_{-40}) / 20$ mV / dB

(Note 4) VCO Conversion Sensitivity : β

Input f = 402.78MHz and sweep ± 5MHz, v_{in} = − 30dBmW (50Ω) to pin 20.
Calculate $\beta = 10 / (Vdet_{+5} - Vdet_{-5})$ and multiply the gain portion (2.66) of video amplifier when outputting a direct current voltage to pin 3 at 407.78MHz, 397.78MHz as $Vdet_{+5}$ and $Vdet_{-5}$ each.

(Note 5) VCO Temperature Drift : Δf_{Ta}

Short pin 6 and 7, and connect pin 14 to GND.
Measure the VCO frequency at ambient temperature Ta = 25°C, − 10°C + 65°C and calculate how much frequency changes from at 25°C. (read out the VCO leakage output by spectrum analyzer.)

(Note 6) PLL Lock Range : f_L, Capture Range : fca

Measure the range that synchronizes with VCO by putting pin 20 input frequency away from the free-running frequency.

(Note 7) Demodulation Output Level : V_{out}

Input pin 20 f = 402.78MHz, f_m = 100kHz, $\Delta f = 10MHz_{p-p}$, v_{in} = − 30dBmW (50Ω)
Open pin 4 and 5 and measure the output level of pin 3.

(Note 8) Video Amplifier Variable Width : V_{outS}、V_{out5}

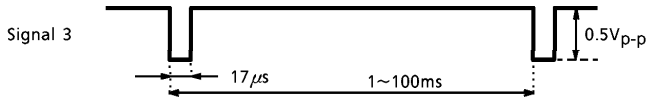
Input pin 20 f = 402.78MHz, f_m = 100kHz, $\Delta f = 10MHz_{p-p}$, v_{in} = − 30dBmW (50Ω)
Measure the variation of video output by shorting between pin 4 and 5 and connecting a 5kΩ resistance.

(Note 9) Demodulation Output level Width, Group Delay Characteristics : V_{outA}, τpd

Input pin 20 f = 402.78MHz, f_m = 100kHz, 60Hz to 4MHz to 9MHz, $\Delta f = 5MHz_{p-p}$,
v_{in} = − 30dBmW (50Ω)
Compare to the value at 100kHz by opening pin 4 and 5, and measuring the output level and group delay of pin 3.

(Note 10) Keyed Pulse Allowable Period : T_1

Input pin 20 f = 402.78MHz, f_m = 100kHz, Δf = 10MHz$_{p-p}$, v_{in} = −30dBmW (50Ω)
Input the signal below to pin 1 and open pin 27 and 28.



Observe the pin 23 output and change f so as to be 2.5V voltage.
Measure the frequency range in which a 2kHz sine wave does not output to pin 23, by changing the signal 3 period.
If the sample-hold circuit malfunctions, the 2kHz sine wave will be outputted from pin 23.

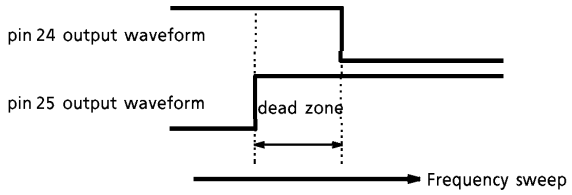
(Note 11) AFT Sensitivity : $\Delta f / \Delta V_{23}$

Input pin 20 f = 402.78MHz ± 1MHz, v_{in} = −30dBmW (50Ω)
Adjust f so that pin 23 output will be 2.5V. By moving f up. and down, calculate each frequency as f_H, f_L when pin 23 voltage varies 0.5V using the following equation.

$\Delta f / \Delta V_{23} = f_H - f_L$ (MHz / V)

(Note 12) AFT Digital Output Width of dead zone : f_{DEAD}

Input pin 20 f = 402.78MHz ± 5MHz, v_{in} = −30dBmW (50Ω)
Measure the input frequency range in which both pin 24 and 25 become high level, by sweeping f.



(Note 13) DG, DP

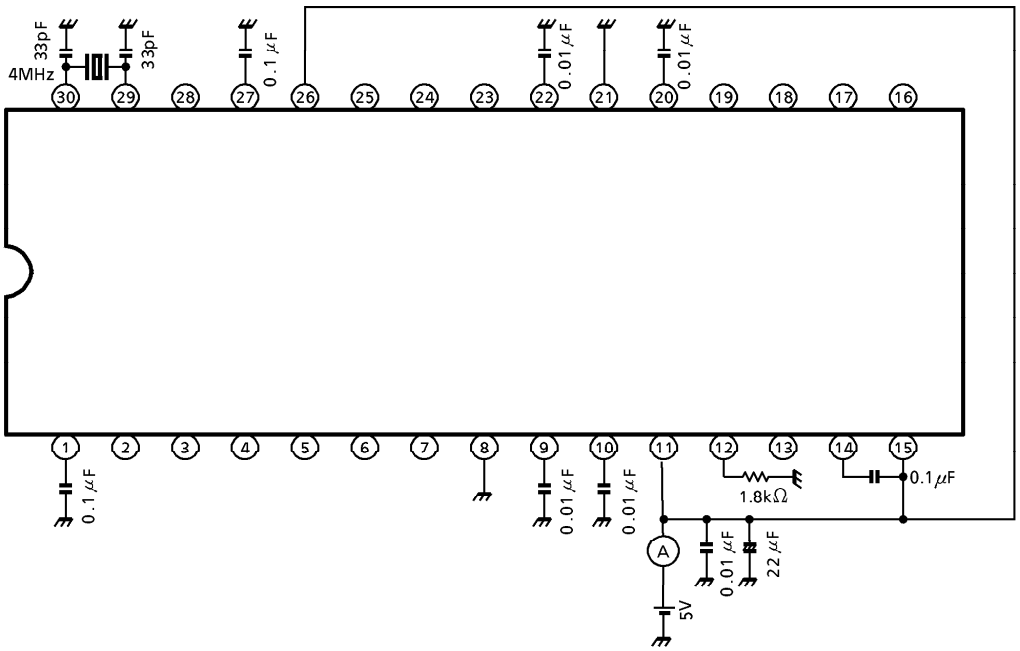
Input pin 20 f = 402.78MHz ± 5MHz, v_{in} = −30dBmW (50Ω), Δf = 17MHz$_{p-p}$, Gray level video signal (APL : 10~90%)··· Pre-emphasis-on

(Note 14) IM2, IM3

Input pin 20 f = 402.78MHz ± 5MHz, v_{in} = −30dBmW (50Ω), Δf = 17MHz$_{p-p}$, Color subcarrier (3.579MHz), Sound subcarrier (5.7272MHz) ···
Observe the frequency component outputting to the screen output pin (pin 3) through the video gate of a video noise meter by spectrum analyzer, and measure the level difference between 3.579MHz component and 2.15MHz, 1.43MHz components.

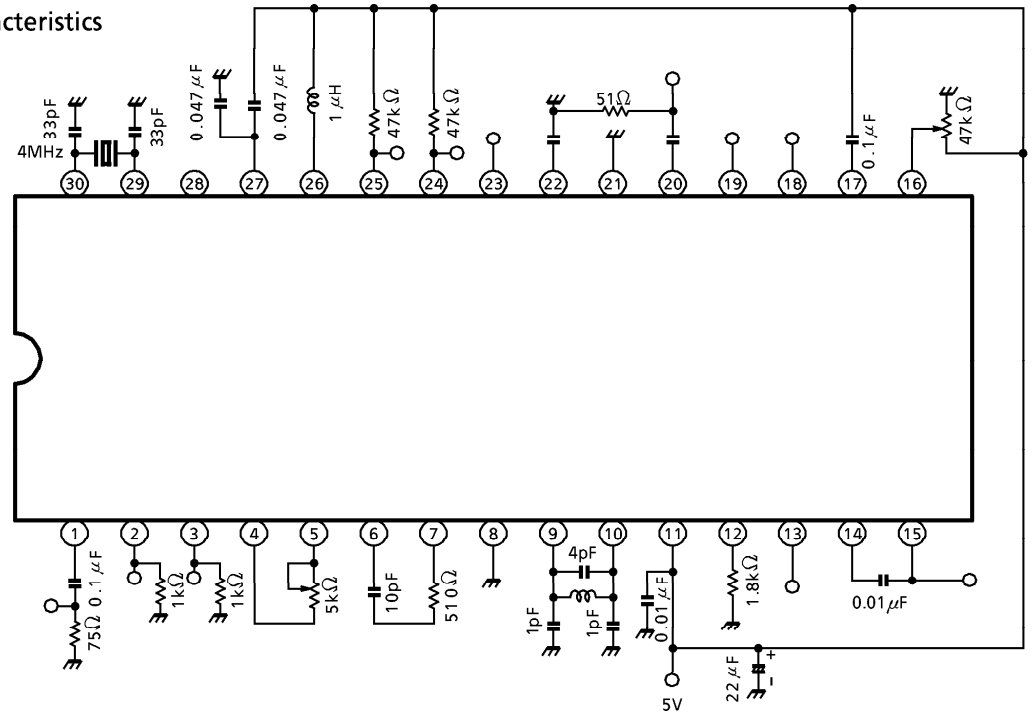
TEST CIRCUIT 1

DC characteristics



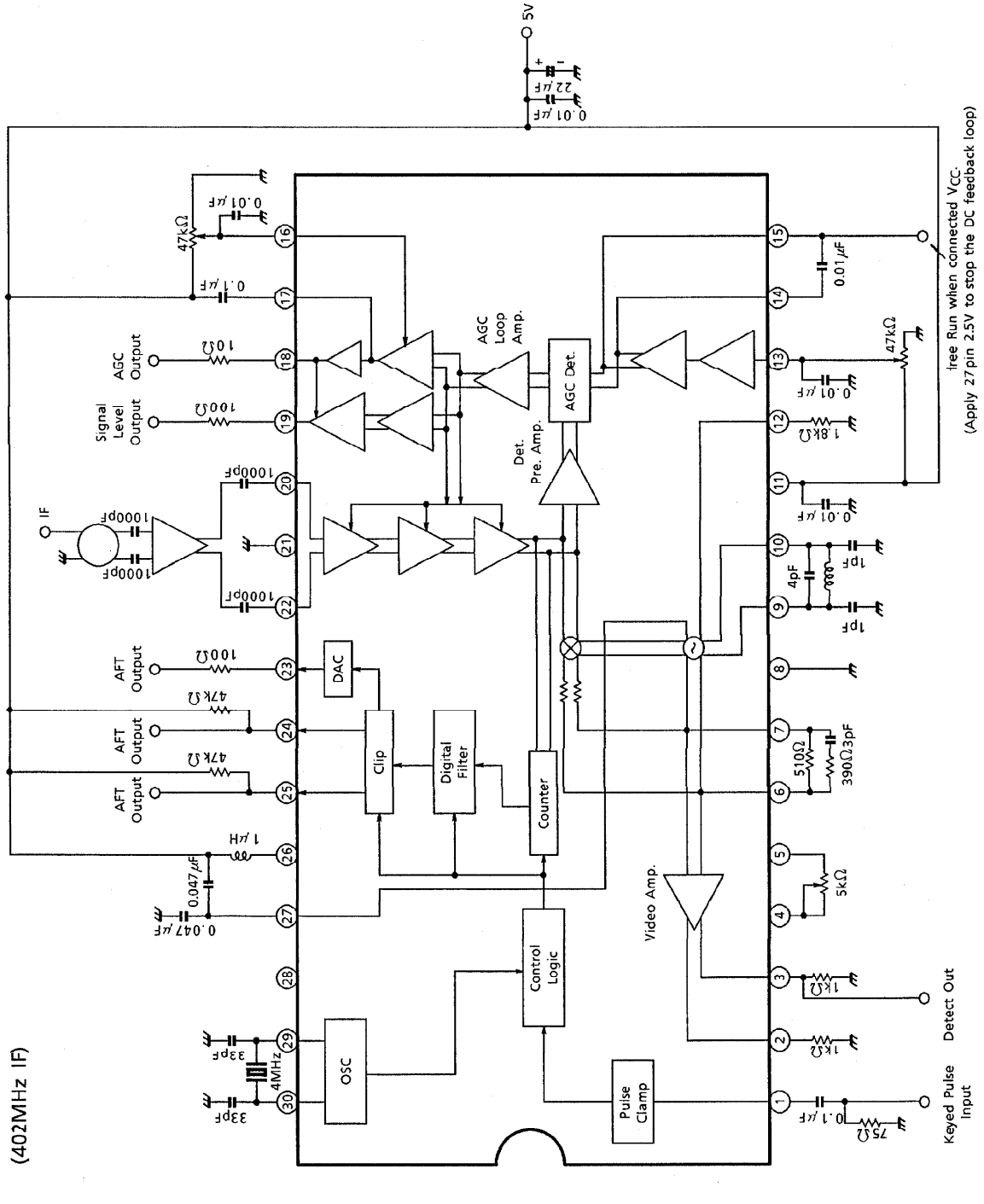
TEST CIRCUIT 2

AC characteristics



APPLICATION CIRCUIT

(402MHz IF)



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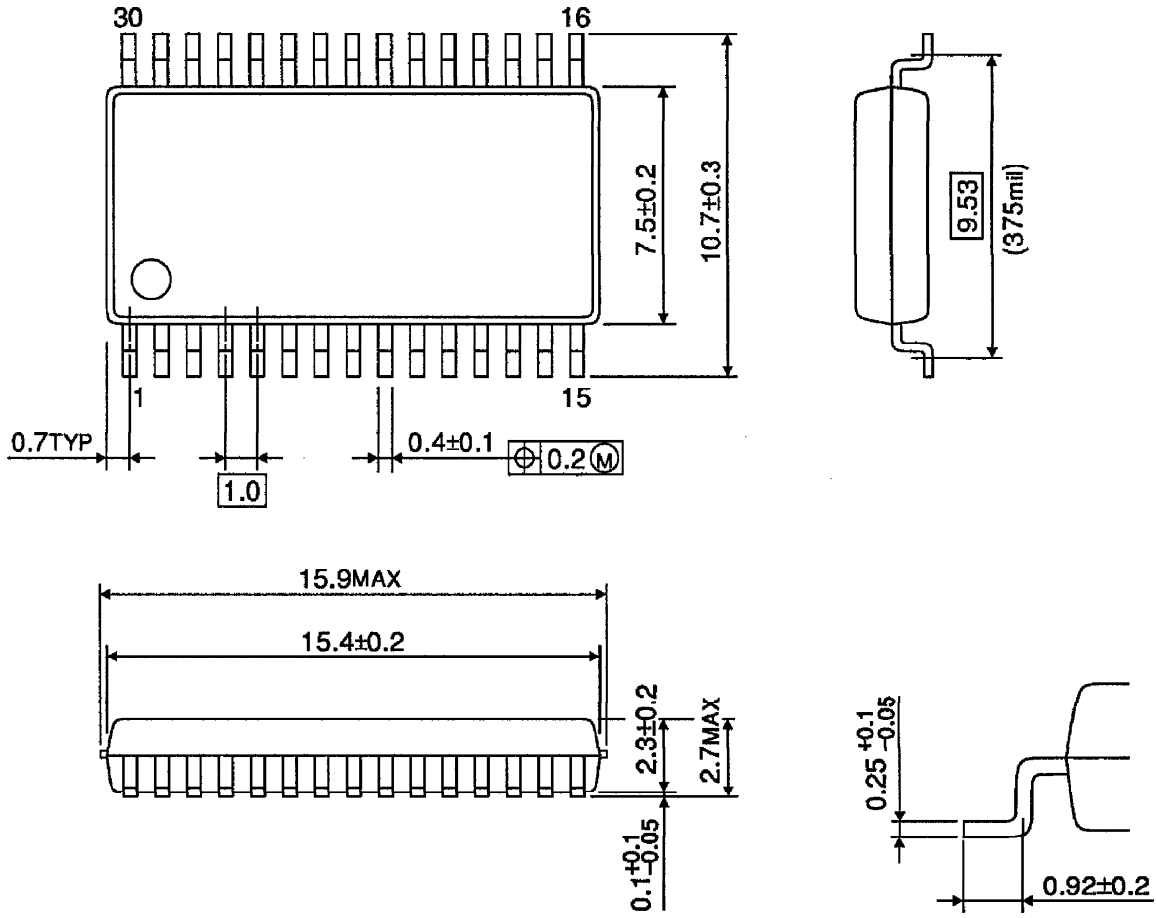
OUTLINE DRAWING

SSOP30-P-375-1.00

Unit : mm



Weight : 0.63g (Typ.)