TA7270P
TA7271P

T-74-05-01

5.8W DUAL AUDIO POWER AMPLIFIER.
19W BTL AUDIO POWER AMPLIFIER.

The TA7270P/TA7271P are dual audio power amplifier for consumer applications. It is designed for high power, low distortion and low noise.
It also contains various kind of protectors.
It is suitable for car-audio power amplifier with high performance.

- Two Kinds of Pin Configulation are Available:
  Normal (TA7270P) and Reverse (TA7271P) for Easier Layout Design of PC-board when Used in BTL-Stereo Application.
- Operating Supply Voltage Range:
  V_{CC} (opr)=9 ∿ 18V
- High Power
  V_{CC}=13.2V, f=1kHz, R_L=4Ω

BTL	19W (Typ.)	THD=10%
	15W (Typ.)	THD=1%
DUAL	5.8W (Typ.)	THD=10%

- Low Distortion
  V_{CC}=13.2V, f=1kHz, R_L=4Ω

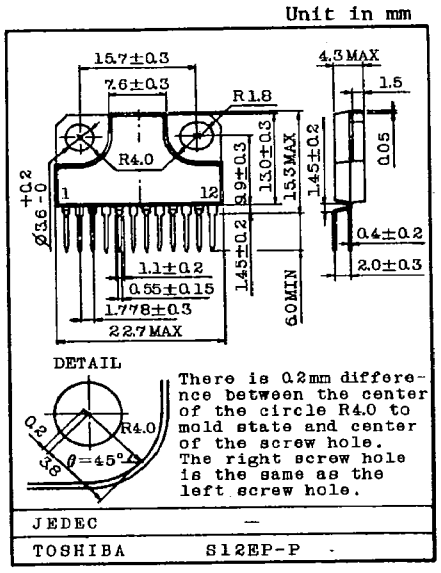
BTL	0.03% (Typ.)	P_{OUT}=4W, G_V=40dB
DUAL	0.06% (Typ.)	P_{OUT}=1W, G_V=52dB

- Low Noise
  V_{CC}=13.2V, R_L=4Ω

BTL	0.14mVrms (Typ.)	G_V=40dB, R_g=0, DIN NOISE: DIN 45405
DUAL	0.7 mVrms (Typ.)	G_V=52dB, R_g=10kΩ, BW=20Hz ∿ 20kHz

- Protector: Thermal Shut Down, Over Voltage Protection.
  BTL-OCL DC Short Protection.

Unit in mm



JEDEC	—
TOSHIBA	S12EP-P

Weight : 4.04g (TYP.)

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MAXIMUM RATINGS ($Ta=25^{\circ}C$)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Peak Supply Voltage (0.2 sec)	V_{CC} surge	45	V
DC Supply Voltage	V_{CC} DC	25	V
Operating Supply Voltage	V_{CC} opr	18	V
Output Current (peak)	$I_{O(peak)}$	4.5	A
Power Dissipation	P_D	25	W
Operating Temperature	T_{opr}	-30 ~ 75	$^{\circ}C$
Storage Temperature	T_{stg}	-55 ~ 150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, $V_{CC}=13.2V$, $R_L=4\Omega$, $R_g=600\Omega$, f=1kHz, $Ta=25^{\circ}C$)

	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
	Quiescent Current	I_{CCQ}	2	$V_{IN}=0$	-	80	145	mA
BTL CONNECTION MODE	Output Power	$P_{OUT(1)}$	1	THD=10%	16	19	-	W
		$P_{OUT(2)}$	1	THD=1%	12	15	-	W
	Total Harmonic Distortion	THD(1)	1	$P_{OUT}=4W$, Gv=40dB	-	0.03	0.25	%
	Output Offset Voltage	V_{OFF}	1	$V_{IN}=0$	-	0	0.35	V
	Voltage Gain	Gv(1)	1	$V_{OUT}=0dBm$	-	40	-	dB
	Output Noise Voltage	$V_{NO(1)}$	1	$R_g=0$ DIN45405 Noise Filter	-	0.14	-	mV_{rms}
	Ripple Rejection Ratio	R.R(1)	1	$f_{ripple}=100Hz$ $V_{ripple}=0dBm$	-	-52	-40	dB
DUAL MODE	Output Power	$P_{OUT(3)}$	2	THD=10%	5	5.8	-	W
	Total Harmonic Distortion	THD(2)	2	$P_{OUT}=1W$	-	0.06	0.30	%
	Voltage Gain	Gv(2)	2	$V_{OUT}=0dBm$	50	52	54	dB
	Voltage Gain Ratio	ΔGv	2	$V_{OUT}=0dBm$	-1	0	1	dB
	Output Noise Voltage	$V_{NO(2)}$	2	$R_g=10k\Omega$ BW=20Hz ~ 20kHz	-	0.7	1.5	mV_{rms}
	Ripple Rejection Ratio	R.R(2)	2	$f_{ripple}=100Hz$ $V_{ripple}=0dBm$	-	-52	-40	dB
	Cross Talk	C.T	2	$V_{OUT}=0dBm$	-	-57	-	dB
	Input Resistance	R_{IN}	2	f=1kHz	-	33	-	kΩ

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TEST CIRCUIT/APPLICATION CIRCUIT

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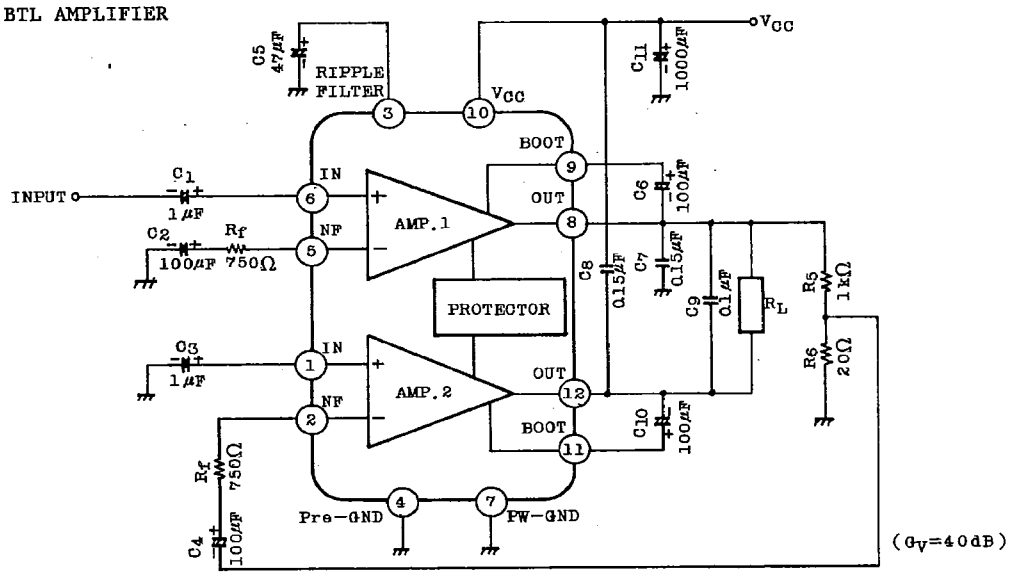
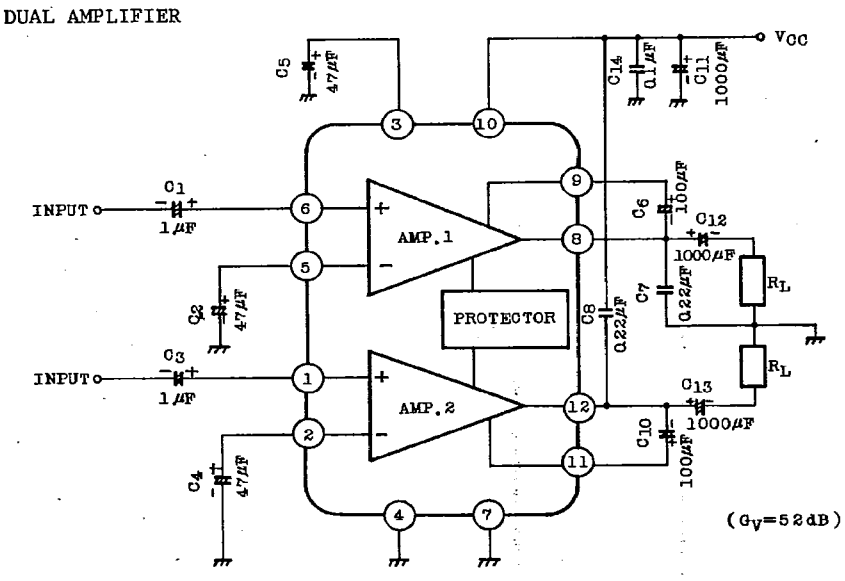
(1) BTL AMPLIFIER



(2) DUAL AMPLIFIER



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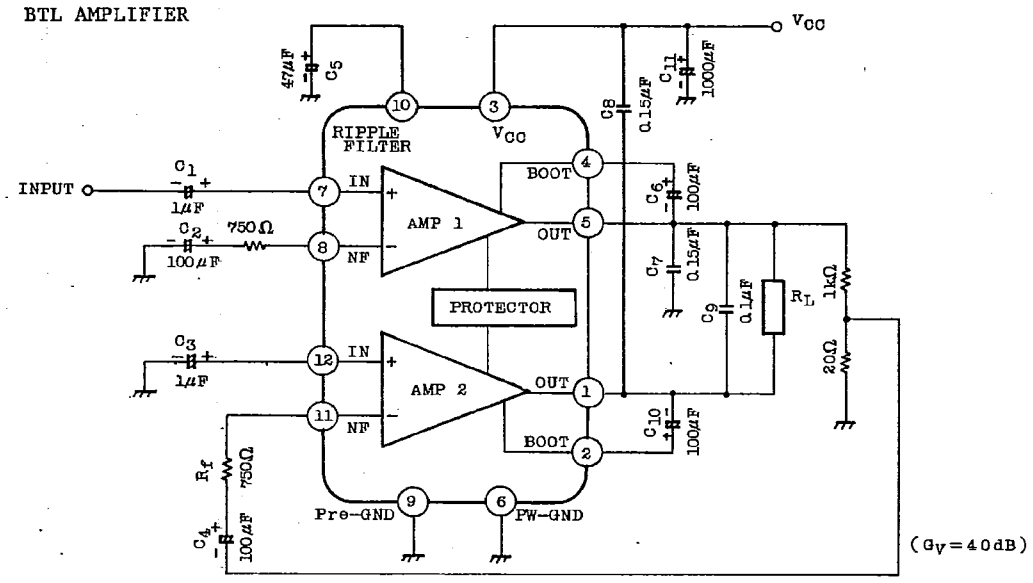
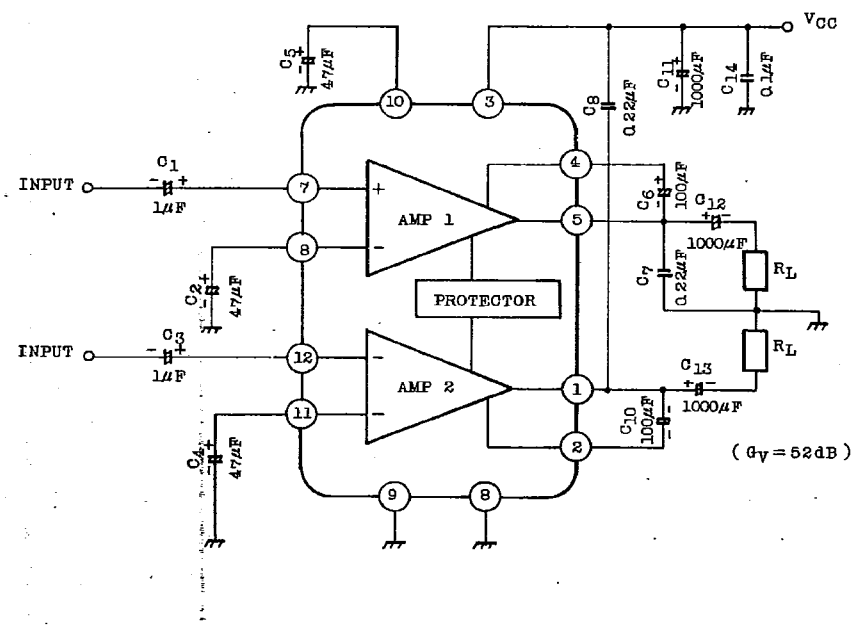


(2) DUAL AMPLIFIER



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TYPICAL DC VOLTAGE OF EACH TERMINAL

(V_{CC}=13.2V, Ta=25°C, DUAL MODE TEST CIRCUIT)

TERMINAL No.		1	2	3	4	5	6	7	8	9	10	11	12
DC Voltage (V)	TA7270P	1.5	1.5	4.4	GND	1.5	1.5	GND	6.6	12.7	V_{CC}	12.7	6.6
	TA7271P	6.6	12.7	V_{CC}	12.7	6.6	GND	1.5	1.5	GND	4.4	1.5	1.5

APPLICATION INFORMATION

(This explanatory terminal number is for TA7270P)

1. VOLTAGE GAIN

(1) Dual Mode

The closed loop voltage gain Gv is determined by R1, R2, R3, R4 and Rf.

$$Gv \fallingdotseq 20\ell og \frac{R2+Rf+R1}{Rf+R1} + 20\ell og \frac{R3+R4}{R4} \text{ [dB]}$$

when Rf=0, Gv=52dB(Typ.)

is given.

The recommended voltage gain is more than 40dB.

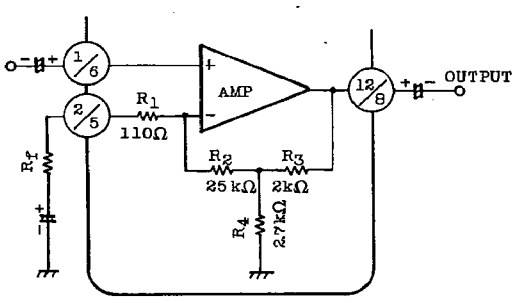

Fig 1

(2) BTL Mode

The recommended BTL connection amplifier is shown in Figure 2.

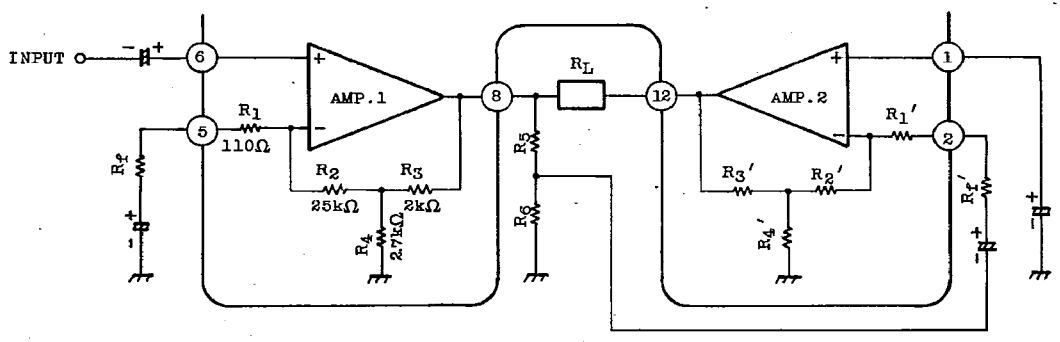

Fig. 2

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AMP.1 is noninverting amplifier and AMP.2 is inverting one. The output voltage is divided by resistors R_5 and R_6.
This divided voltage is applied to inverting input of AMP.2. R_5 and R_6 are determined in the following equation.

$$\frac{R_5+R_6}{R_5} = 20\,\ell og \frac{R_1'+R_f'+R_2'}{R_1'+R_f'} + 20\,\ell og \frac{R_3'+R_4'}{R_4'} \quad \text{..... Gv in Dual Mode}$$

The voltage gain in this circuit is 6dB higher than that in dual mode.

$$G_V = 20\,\ell og \frac{R_1+R_f+R_2}{R_1+R_f} + 20\,\ell og \frac{R_3+R_4}{R_4} + 6 \quad [dB]$$

In case of $R_f=0$

$G_V=52+6=58$[dB]

In case of $R_f=750\Omega$

$G_V=34+6=40$[dB]

2. MUTING

Audio muting can be accomplished by connecting pin ③ (ripple filter) to GND as shown in Fig.3. Then, the bias circuits are cut off.
Amount of muting attenuation is more than 60dB.
Precaution in muting operation is as follows.

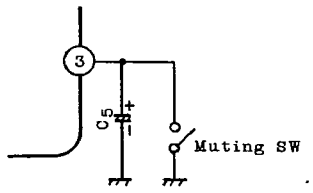

Fig.3

(1) The recovery time at muting off depends on Capacitance C_2, C_4 and C_5 in the test Circuti.

(2) As this muting system is operated by the shart-circuit of ripple filter : C_5, the ripple rejection ratio becomes warse in a muting mode.
Note that some "POP-Noise" occur when bias is shut off with mute-on.

3. CAPACITOR C_7, C_8

The purpose of capacitor C_7, C_8 is to prevent oscillation.
These capacitors need to be small temperature coefficient. So celamic capacitor is unsuitabel.
A voltage gain less than 40dB results occasionally in a parastic oscillation.
Stability for parastic oscillation is promoted by connecting capacitor of 500 ∿ 1000pF between pin ① and pin ② (pin ⑤ and pin ⑥).
The additional capacitors are recommended to be inserted.

4. PRECAUTION AT PRINT BOARD DESIGN

(1) Print Pattern board should be designed in consideration of stability for parastic oscillation.
The following parts-layout is recommended.
1st. Capacitors C_6 and C_{10} are spaced most close to the output pin.
2nd. Capacitor C_7 or C_8 is spaced close to the output pin next to C_6 and C_{10}.
3rd. Capacitor C_9 is spaced close to it next to C_7 and C_8.
4th. Capacitor C_{11} is spaced close to it next to C_9.

(2) Input line (pin ⑥) and PW-GND line (pin ⑦) should not be spaced in parallel. In the paralled layout, output current signal in PW-GND line is bed back to input line by electromagnetic coupling. Then it deteriorates the total harmonic distortion, especially at high audio frequency region.

(3) Undesirable terminating of capacitors deteriorates "pop" noise or THD. Capacitors C_2, C_4 and C_5 should be terminated to Pre-GND (pin ④). Capacitors C_7, C_{11}, and C_{14} should be terminated to PW-GND (pin ⑦).

(4) It is recommended to refer the standard print board.

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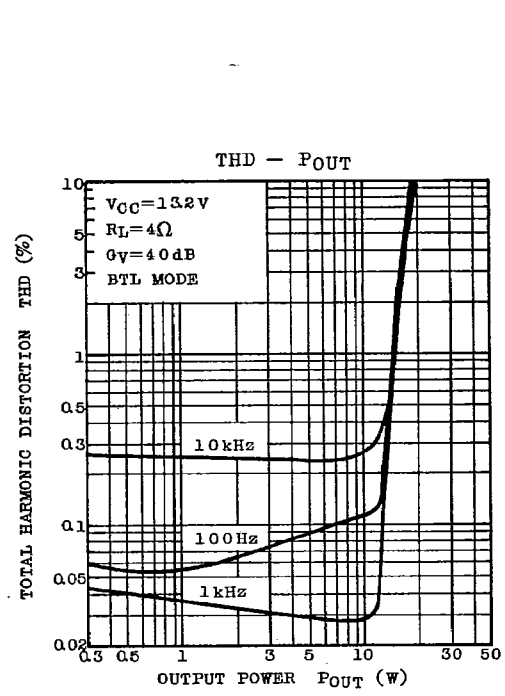
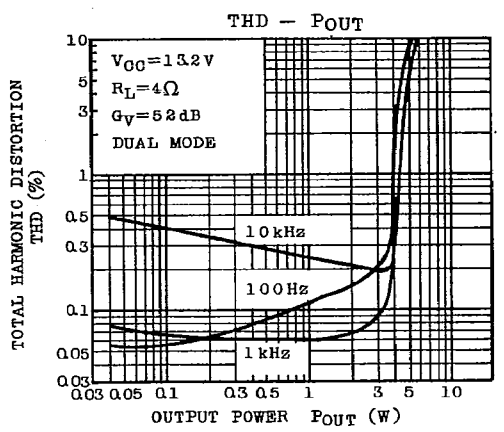
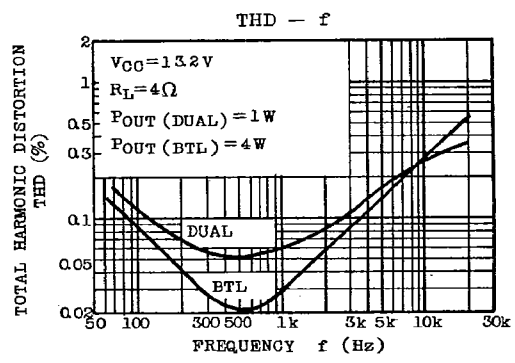
THD – POUT

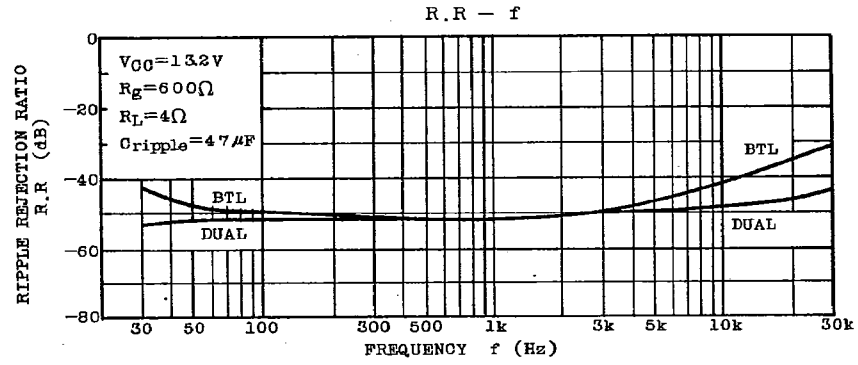




THD – f



R.R – f



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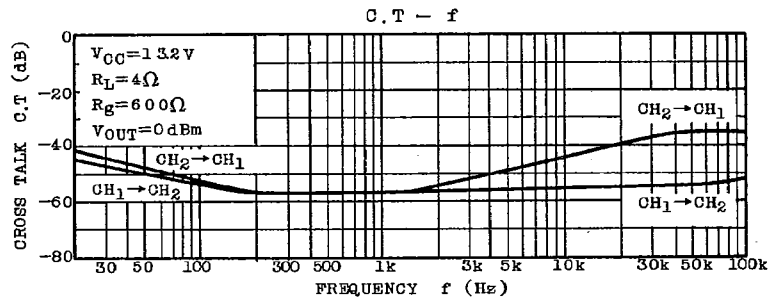
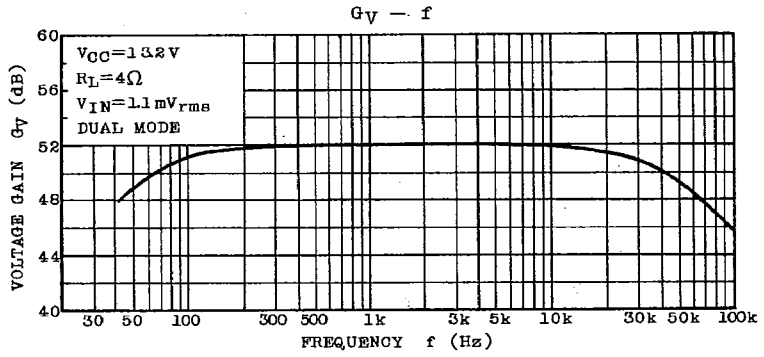
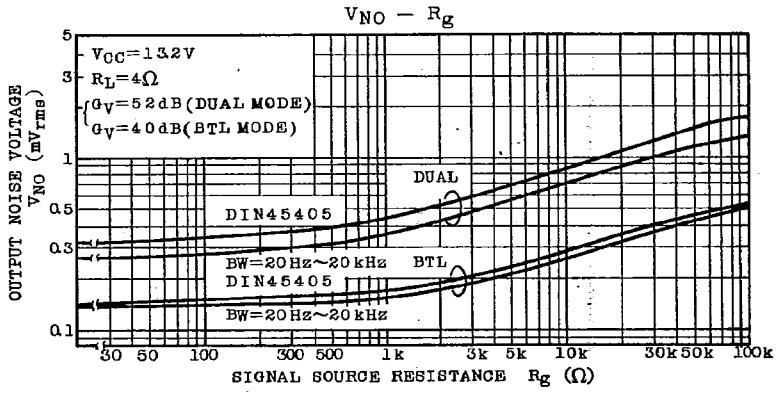
C.T — f



G_V — f



V_{NO} — R_g



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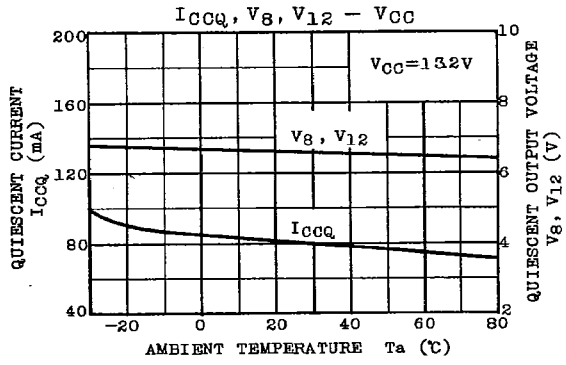
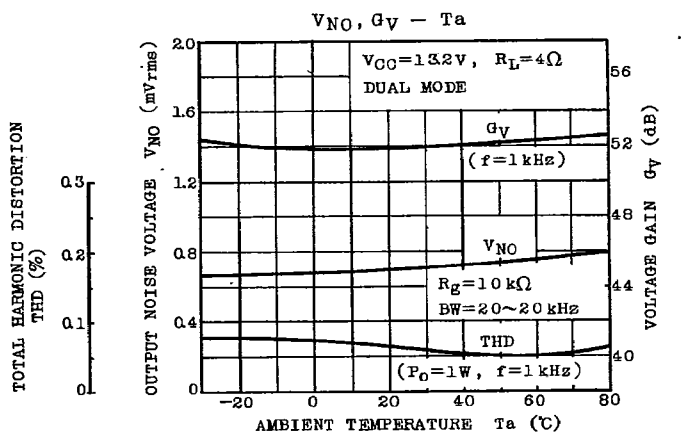
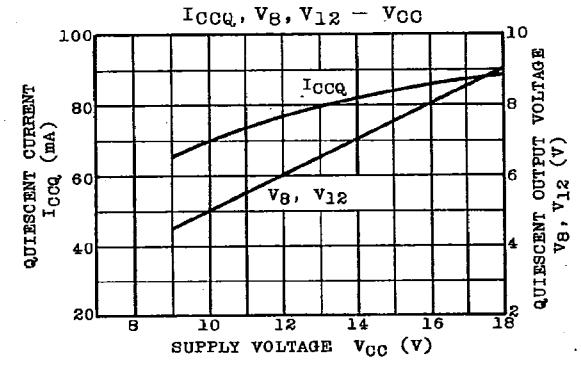
I_{CCQ}, V_8, V_{12} — V_{CC}



V_{NO}, G_V — Ta



I_{CCQ}, V_8, V_{12} — V_{CC}



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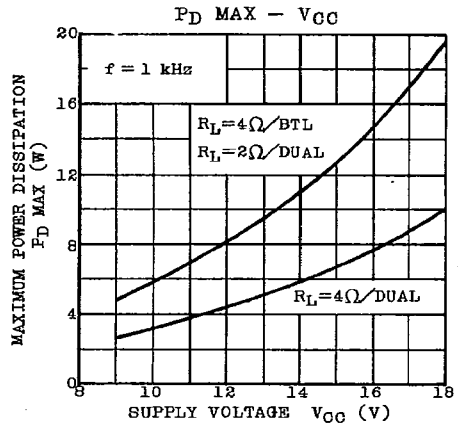
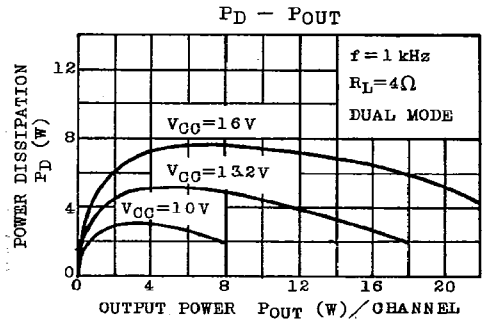
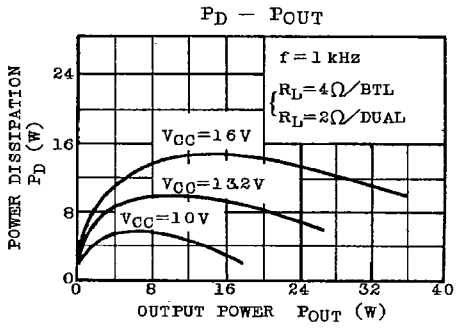
P_D MAX — V_{CC}



P_D — P_{OUT}



P_D — P_{OUT}



P_D MAX — Ta