Features

- **Single 3-V Supply Voltage**
- **High Power-added Efficient Power Amplifier (P_{out} Typically 23 dBm)**
- **Ramp-controlled Output Power**
- **Low-noise Preamplifier (NF Typically 2.1 dB)**
- **Biasing for External PIN Diode T/R Switch**
- **Current-saving Standby Mode**
- **Few External Components**
- **Packages:**
  - **PSSO20**
  - **HP-VFQFP-N20 with Extended Performance**

Electrostatic sensitive device.
Observe precautions for handling.

Bluetooth™/ISM 2.4-GHz Front-End IC

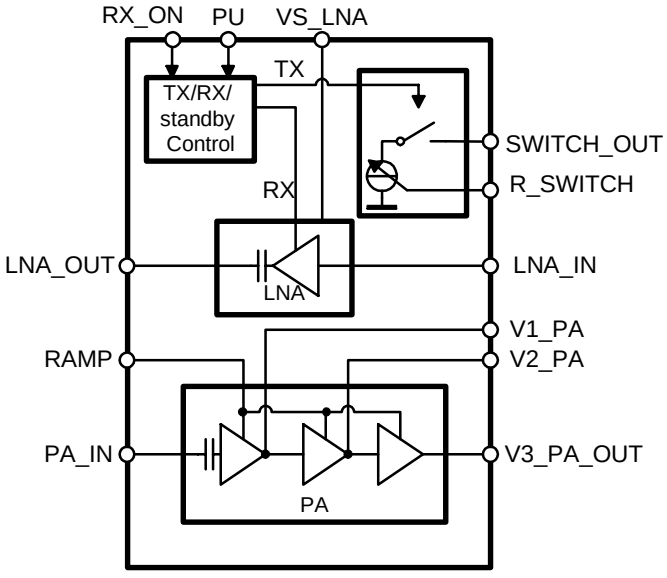
T7024

Description

The T7024 is a monolithic SiGe transmit/receive front-end IC with power amplifier, low-noise amplifier and T/R switch driver. It is especially designed for operation in TDMA systems like Bluetooth™ and WDCT

Due to the ramp-control feature and a very low quiescent current, an external switch transistor for V_S is not required.

Figure 1. Block Diagram



Rev. 4533B–BLURF–01/03

Pin Configuration

Figure 2. Pinning PSSO20

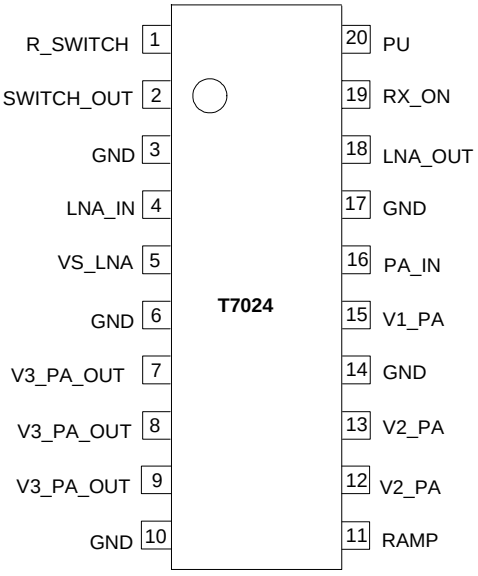
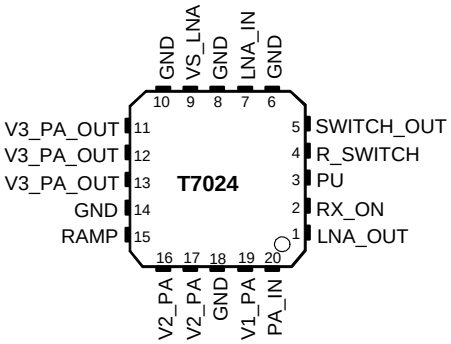


Figure 3. Pinning HP-VFQFP-N20



Pin Description

Pins PSSO20	Pins N20	Symbol	Function
1	4	R_SWITCH	Resistor to GND sets the PIN diode current
2	5	SWITCH_OUT	Switched current output for PIN diode
3	6	GND	Ground
4	7	LNA_IN	Low-noise amplifier input
5	9	VS_LNA	Supply voltage input for low-noise amplifier
6	8	GND	Ground
7	11	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
8	12	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
9	13	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
10	10	GND	Ground
11	15	RAMP	Power ramping control input
12	16	V2_PA	Inductor to power supply for power amplifier
13	17	V2_PA	Inductor to power supply for power amplifier
14	14	GND	Ground
15	19	V1_PA	Supply voltage for power amplifier
16	20	PA_IN	Power amplifier input
17	18	GND	Ground
18	1	LNA_OUT	Low-noise amplifier output
19	2	RX_ON	RX active high
20	3	PU	Power-up active high
Slug	Slug	GND	Ground

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage Pins VS_LNA, V1_PA, V2_PA, V3_PA_OUT	V_S	6	V
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-40 to +125	°C
RF input power LNA	P_{inLNA}	5	dBm
RF input power PA	P_{inPA}	10	dBm

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient PSSOP20, slug soldered on PCB	R_{thJA}	19	K/W
Junction ambient HP-VFQFP-N20, slug soldered on PCB	R_{thJA}	27	K/W

Operating Range

All voltages are referred to ground (Pins GND and slug). Power supply points are VS_LNA, V1_PA, V2_PA, V3_PA_OUT. The table represents the sum of all supply currents depending on the TX/RX mode.

Parameters		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pins V1_PA, V2_PA and V3_PA_OUT	V_S	2.7	3.0	4.6	V
Supply voltage	Pin VS_LNA	V_S	2.7	3.0	5.5	V
Supply current TX RX	PSSO20 N20	I_S I_S I_S		190 165 8		mA mA mA
Standby current	PU = 0	$I_{S\_standby}$		10		µA
Ambient temperature		T_{amb}	-25	+25	+70	°C

Electrical Characteristics

Test conditions (unless otherwise specified): V_S = 3.0 V, T_{amb} = 25°C

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Power Amplifier (1)						
Supply voltage	Pins V1_PA, V2_PA, V3_PA_OUT	V_S	2.7	3.0	4.6	V
Supply current	TX PSSO20 N20	I_{S_TX} I_{S_TX}		190 165		mA mA
	RX (PA off), $V_{RAMP} \leq 0.1$ V	I_{S_RX}			10	µA
Standby current	Standby	$I_{S\_standby}$			10	µA
Frequency range	TX	f	2.4		2.5	GHz
Gain-control range	TX	ΔGp	60	42		dB
Power gain maximum	TX, Pin PA_IN to V3_PA_OUT	Gp	28	30	33	dB
Power gain minimum	TX, Pin PA_IN to V3_PA_OUT	Gp	-40		-17	dB
Ramping voltage maximum	TX, power gain (maximum) Pin RAMP	$V_{RAMP\ max}$	1.7	1.75	1.83	V
Ramping voltage minimum	TX, power gain (minimum) Pin RAMP	$V_{RAMP\ min}$		0.1		V
Ramping current maximum	TX, V_{RAMP} = 1.75 V, Pin RAMP	$I_{RAMP\ max}$			0.5	mA
Power-added efficiency	TX PSSO20 N20	PAE PAE	30 35	35 40		% %
Saturated output power	TX, input power = 0 dBm referred to Pins V3_PA_OUT	P_{sat}	22	23	24	dBm
Input matching (2)	TX, Pin PA_IN	Load VSWR		<1.5:1		
Output matching (2)	TX, Pins V3_PA_OUT	Load VSWR		<1.5:1		
Harmonics at P_{sat} = 23 dBm	TX, Pins V3_PA_OUT	2 fo			-30	dBc
	TX, Pins V3_PA_OUT	3 fo			-30	dBc
T/R Switch Driver (Current Programming by External Resistor from R_SWITCH to GND)						
Switch-out current output	Standby, Pin SWITCH_OUT	$I_{S\_O\_standby}$			1	µA
	RX	$I_{S\_O\_RX}$			1	µA
	TX at 100 Ω	$I_{S\_O\_100}$		1.7		mA
	TX at 1.2 kΩ	$I_{S\_O\_1k2}$		7		mA
	TX at 33 kΩ	$I_{S\_O\_33k}$		17		mA
	TX at ∞	$I_{S\_O\_R}$		19		mA
Low-noise Amplifier (3)						
Supply voltage	All, Pin VS_LNA	V_S	2.7	3.0	5.5	V
Supply current	RX	I_S		8	9	mA
Supply current (LNA and control logic)	TX (control logic active) Pin VS_LNA	I_S			0.5	mA

Notes:
1. Power amplifier shall be unconditionally stable, maximum duty cycle 100%, true CW operation, maximum load mismatch and duration: load VSWR = 10:1 (all phases) 10 s, Z_G = 50 Ω.
2. With external matching network, load impedance 50 Ω.
3. Low-noise amplifier shall be unconditionally stable.
4. With external matching components.

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_S = 3.0 V, T_{amb} = 25°C

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Standby current	Standby, Pin VS_LNA	$I_{S\_standby}$		1	10	µA
Frequency range	RX	f	2.4		2.5	GHz
Power gain	RX, Pin LNA_IN to LNA_OUT	Gp	15	16	19	dB
Noise figure	RX, PSSO20 N20	NF NF		2.5 2.1	2.8 2.3	dB
Gain compression	RX, referred to Pin LNA_OUT	O1dB	-9	-7	-6	dBm
3rd-order input interception point	RX	IIP3	-16	-14	-13	dBm
Input matching (4)	RX, Pin LNA_IN	VSWRin			2:1	
Output matching (4)	RX Pin LNA_OUT	VSWRout			2:1	
Logic input levels (RX_ON, PU)						
High input level	= '1' Pins RX_ON and PU	V_{iH}	2.4		$V_{S, LNA}$	V
Low input level	= '0'	V_{iL}	0		0.5	V
High input current	= '1' V_{iH} = 2.4 V	I_{iH}		40	60	µA
Low input current	= '0'	I_{iL}			0.2	µA

Notes:
1. Power amplifier shall be unconditionally stable, maximum duty cycle 100%, true CW operation, maximum load mismatch and duration: load VSWR = 10:1 (all phases) 10 s, Z_G = 50 Ω.
2. With external matching network, load impedance 50 Ω.
3. Low-noise amplifier shall be unconditionally stable.
4. With external matching components.

Control Logic for LNA and T/R Switch Driver

Operation Mode	PU	RX_ON
Standby	0	0
TX	1	0
RX	1	1

Typical Operating Characteristics

Figure 4. LNA (PSSO20): Gain and Noise Figure versus Frequency

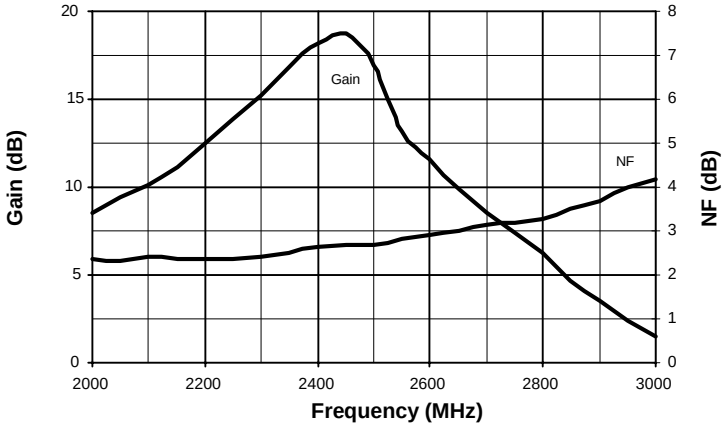


Figure 5. LNA (N20): Gain and Noise Figure versus Frequency

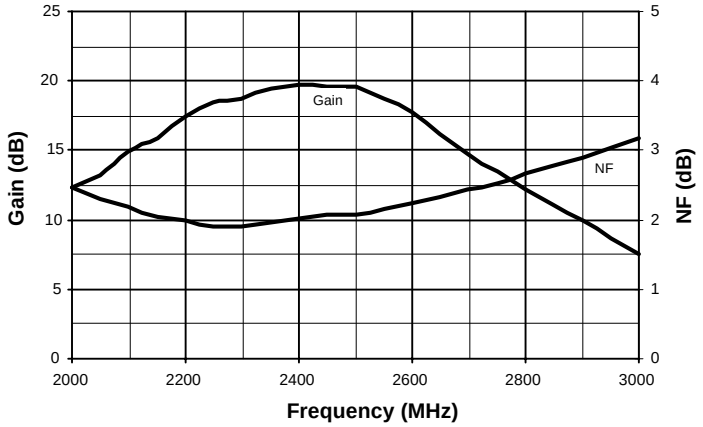


Figure 6. LNA: NF and Gain versus Temperature

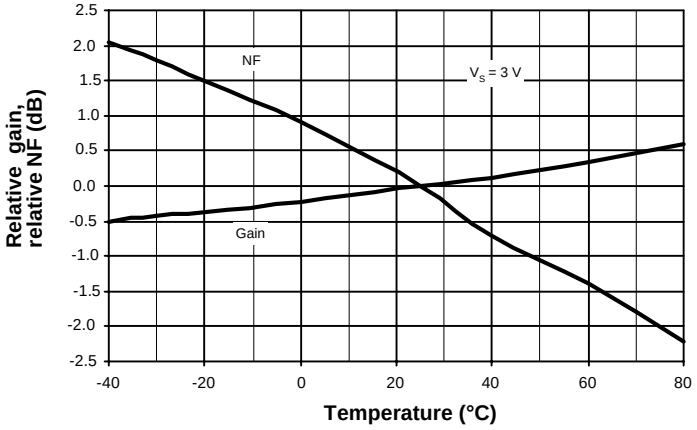


Figure 7. LNA: Typical Switch-out Current versus R_{switch}

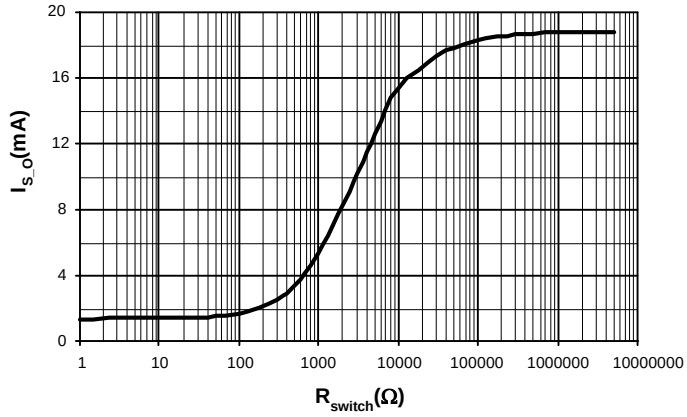


Figure 8. PA (PSSO20): Output Power and PAE versus Supply

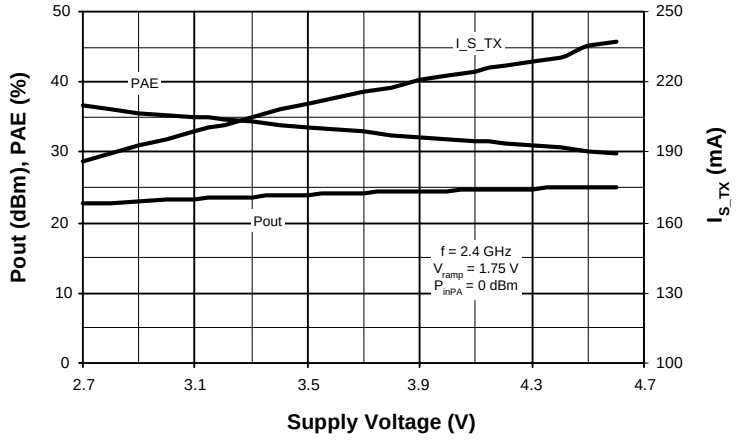


Figure 9. PA (PSSO20): Output Power and PAE versus Ramp Voltage

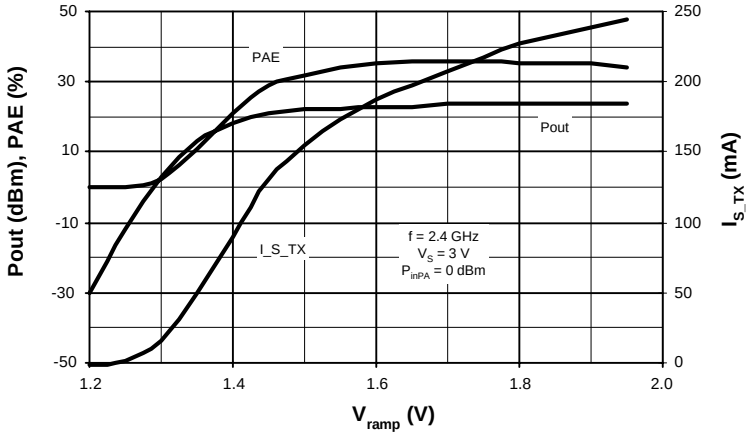


Figure 10. PA (PSSO20): Output Power and PAE versus Input Power

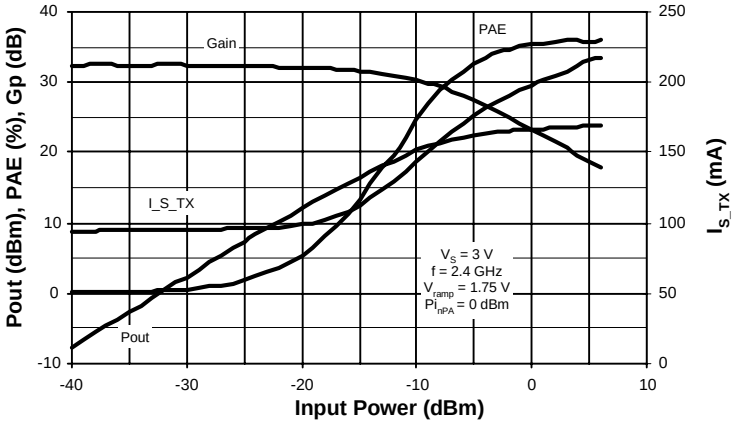


Figure 11. PA (PSSO20): Output Power and PAE versus Frequency

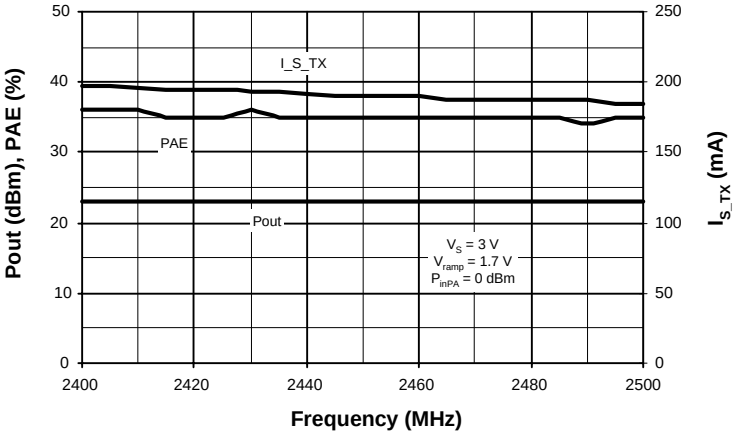


Figure 12. PA (N20): Output Power and PAE versus Supply Voltage

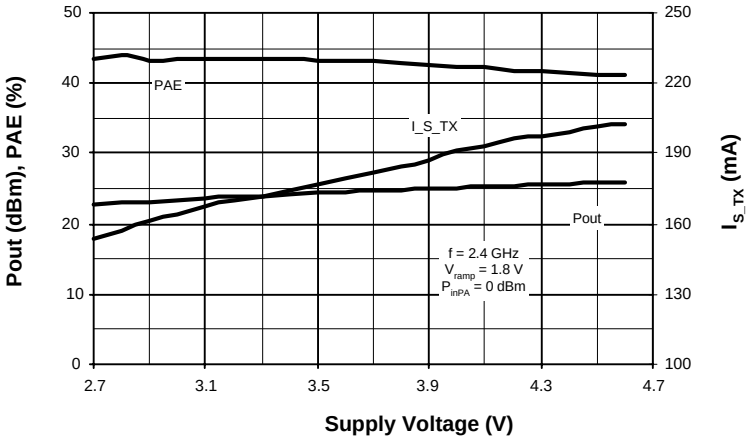


Figure 13. PA (N20) Output Power and PAE versus Ramp Voltage

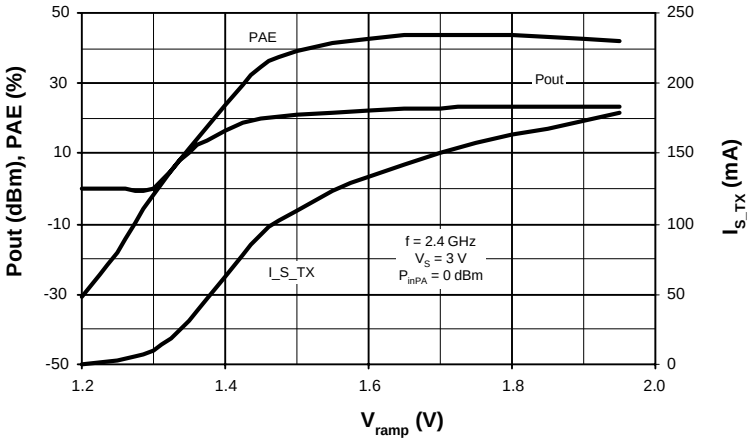


Figure 14. PA (N20): Output Power and PAE versus Input Power

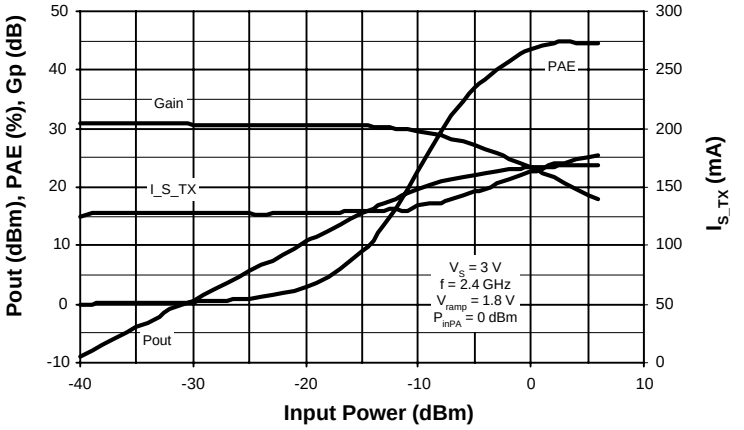


Figure 15. PA (N20): Output Power and PAE versus Frequency

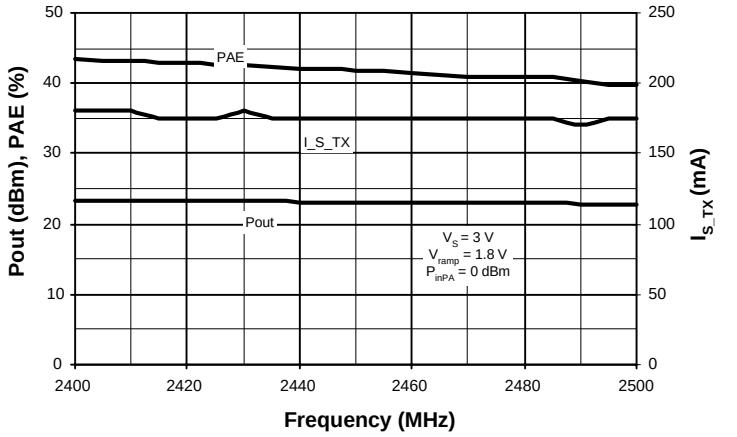


Figure 16. LNA: Supply Current versus Temperature

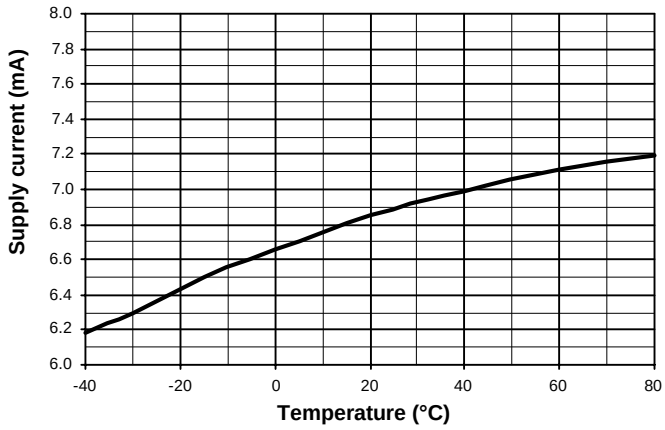


Figure 17. PA (PSSO20): Supply Current versus I_{ramp} and Temperature

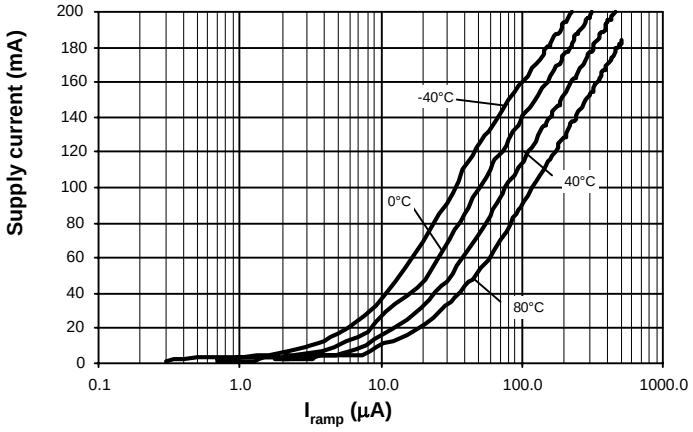
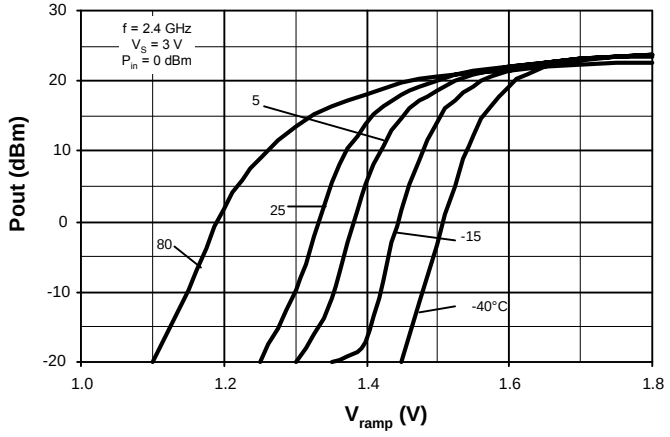


Figure 18. PA (PSSO20, N20): P_{out} versus V_{ramp} and Temperature



Input/Output Circuits

Figure 19. Input Circuit PA_IN/V1_PA

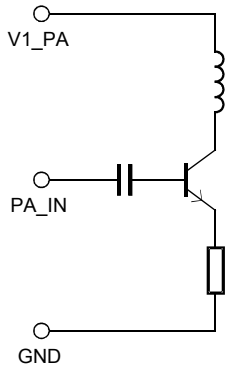


Figure 20. Input Circuit RAMP/V1_PA

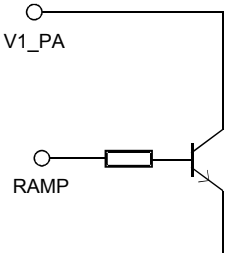


Figure 21. Input Circuit V2_PA

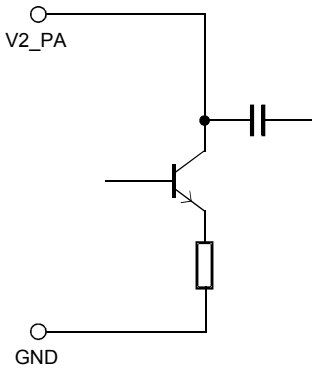


Figure 22. Input/Output Circuit V3_PA_OUT

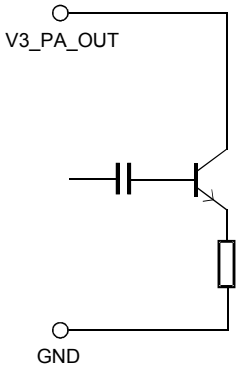


Figure 23. Input Circuit SWITCH_OUT/R_SWITCH

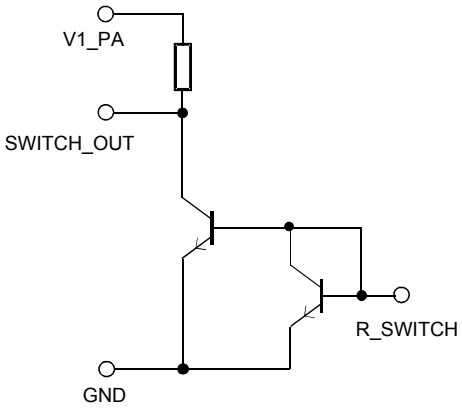


Figure 24. Input Circuit LNA_IN/VS_LNA

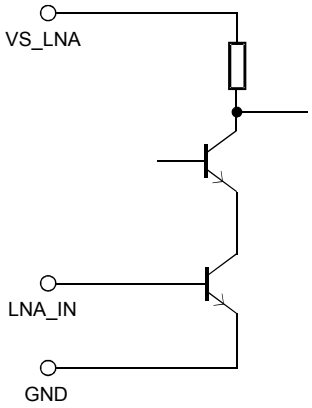


Figure 25. Input Circuit PU/RX_ON

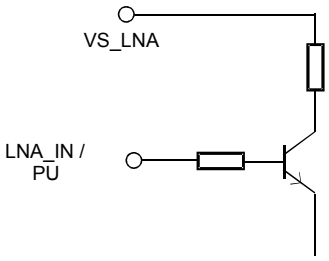


Figure 26. Output Circuit LNA_OUT

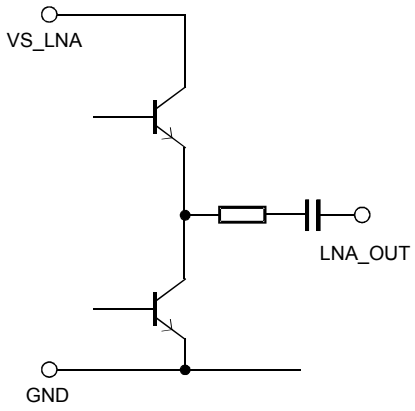


Figure 27. Typical Application T7024 (PSSO20 Package)

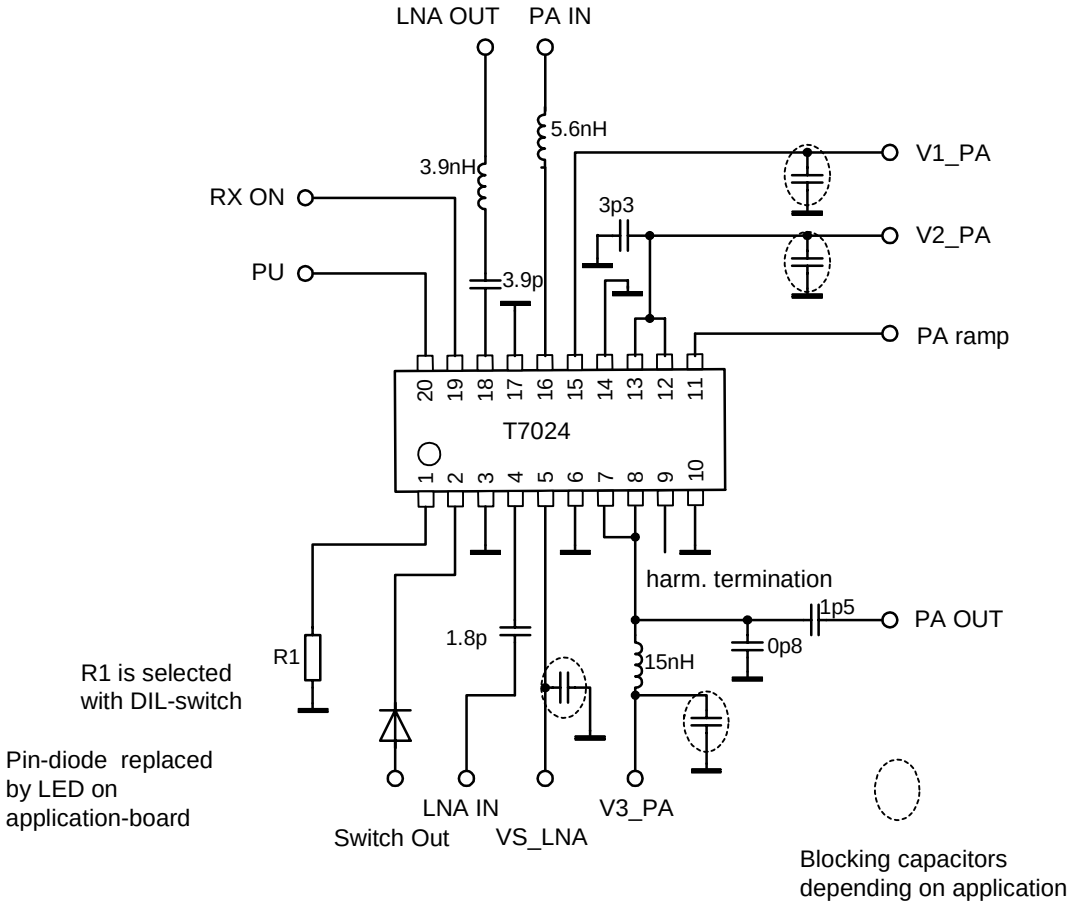
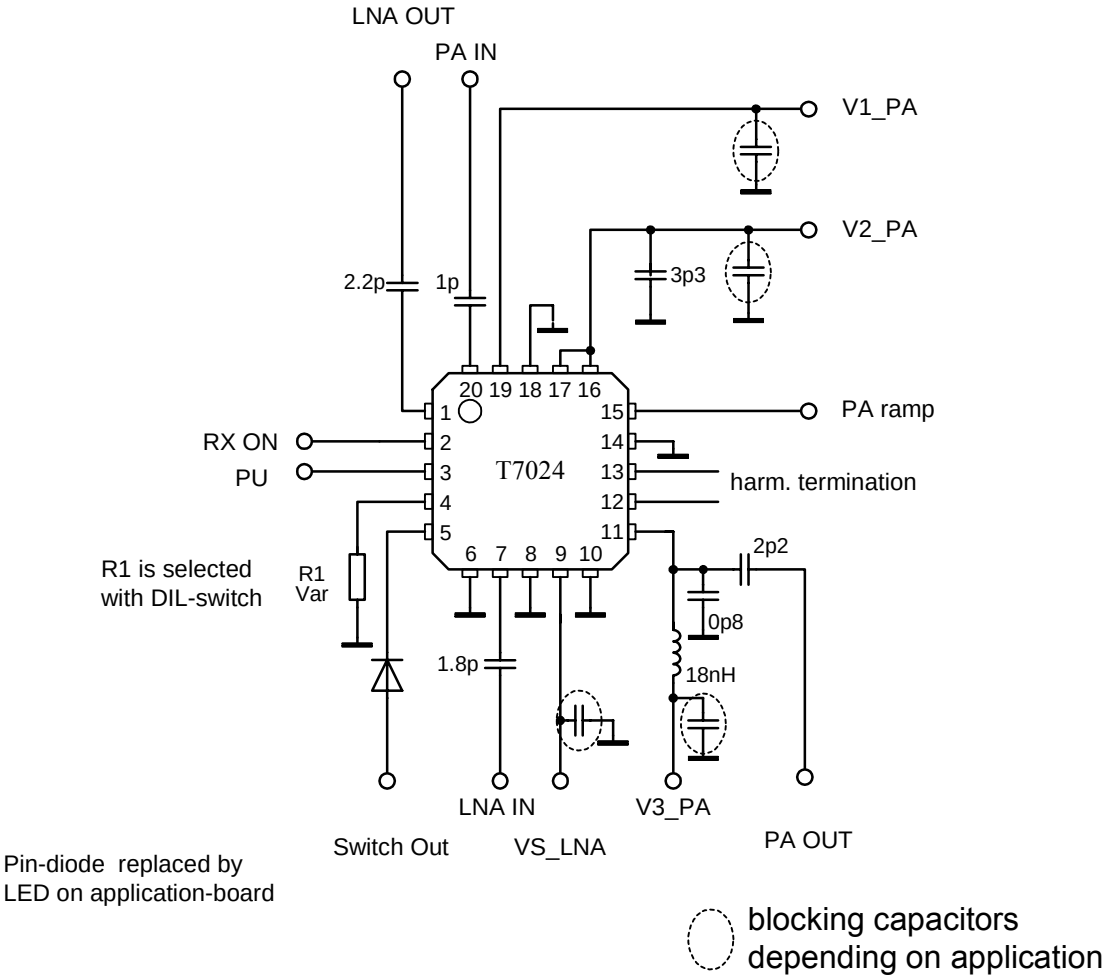


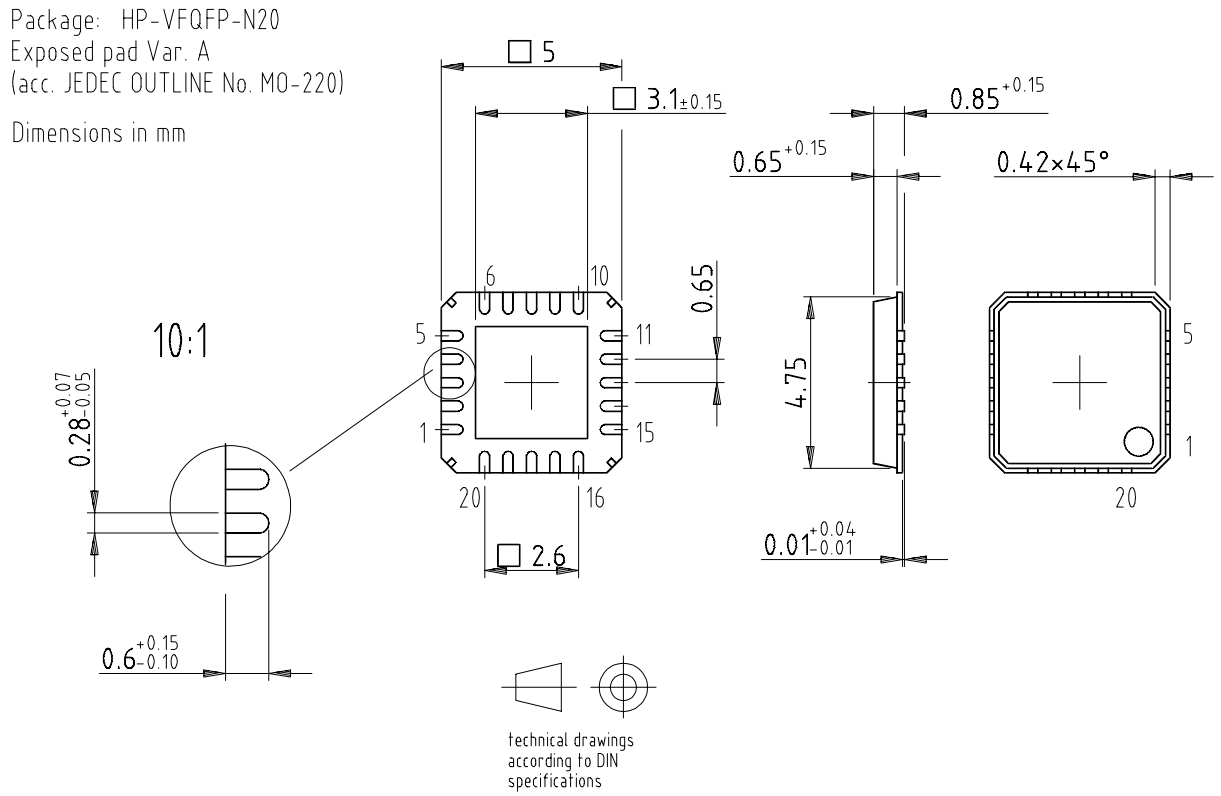
Figure 28. Typical Application T7024 (N20 Package)



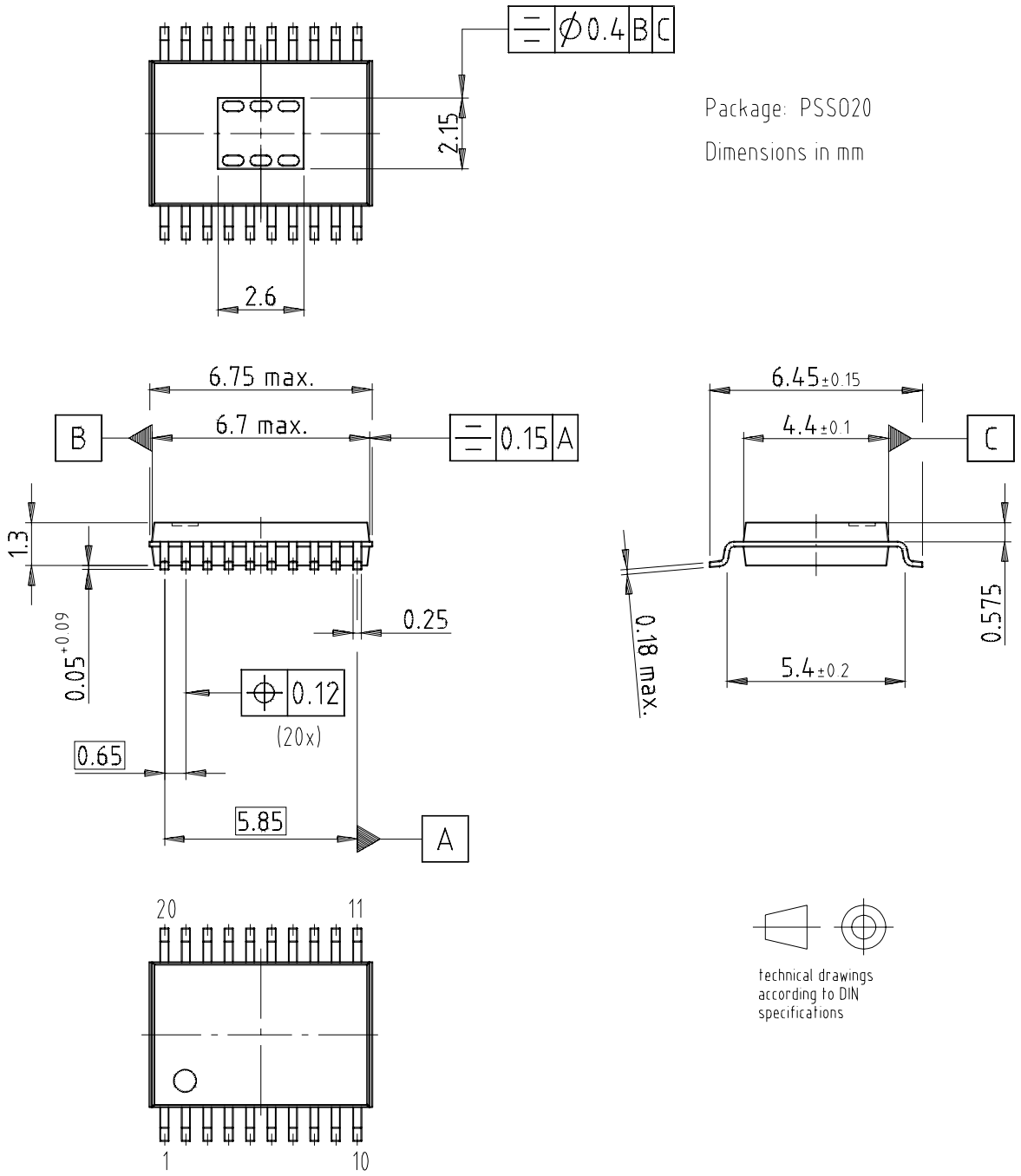
Ordering Information

Extended Type Number	Package	Remarks
T7024-TRS	PSSO20	Tube
T7024-TRQ	PSSO20	Taped and reeled
T7024-PGS	HP-VFQFP-N20	Tube
T7024-PGQ	HP-VFQFP-N20	Taped and reeled

Package Information



Drawing-No.: 6.543-5069.02-4
Issue: 1; 25.09.00



Drawing-No.: 6.543-5078.01-4
Issue: 1; 05.06.01

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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