TOSHIBA CMOS Digital Integrated Circuits Silicon Monolithic

T6L70

Gate Driver for TFT LCD Panel

The T6L70 is a 241-channel output gate driver for TFT LCD panels. In addition to three output voltage levels available. This feature make this device ideal for the UXGA and SXGA + -compatible TFT LCD panel drive systems.

The T6L70 offers high integration circuit due to CMOS technology.

Unit: mm

T6L70E	User-area Pitch	
	IN	OUT

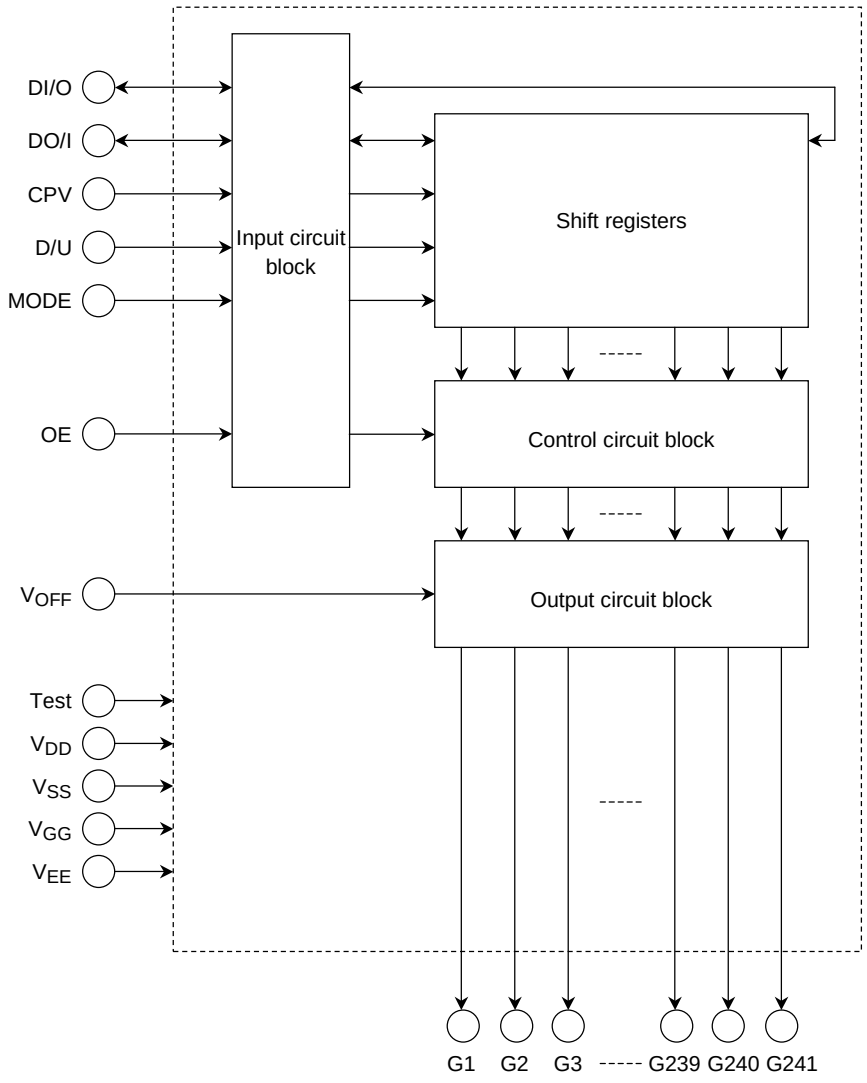
For the latest TCP specifications and lineup, contact your local sales office.

TCP (Tape Carrier Package)

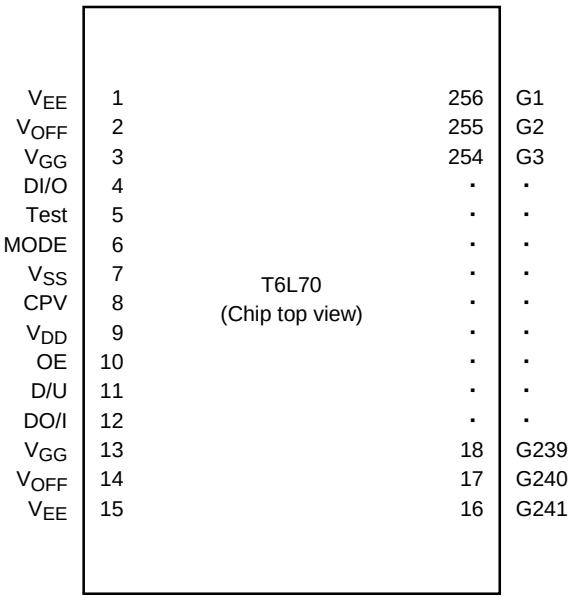
Features

- LCD drive output pins: Switchable between 241 and 211 pins
- Data transfer method : Bidirectional shift registers
- Built-in input signal level-shifting circuit

Block Diagram



Pin Assignment



* Pin assignment viewed from the bump side.

The above diagram does not specify the pad layout on the chip. It is an example of pin assignment on a TCP. For TCP specifications, contact your local sales office.

Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>DI/O
DO/I</td><td>I/O</td><td>Vertical shift data input/output pins
Input/output shift data. The pin function is switched between input and output by the D/U pin as follows:
<table>
<tr><th>D/U</th><th>DI/O</th><th>DO/I</th></tr>
<tr><td>L</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>Output</td><td>Input</td></tr>
</table>
At input
Data are latched into the shift registers in sync with the rising edge of CPV.
At output:
If the T6L70 is cascade-connected, data to be input at the next stage are output from the pin. The data state changes in sync with the falling edge of CPV.</td></tr>
<tr><td>D/U</td><td>I</td><td>Data transfer direction switching pin
Specifies the shift direction of the shift registers (Operation Description (1)).</td></tr>
<tr><td>CPV</td><td>I</td><td>Vertical shift clock
Shift clock for the shift registers. Data are shifted in sync with the rising edge of CPV.</td></tr>
<tr><td>OE</td><td>I</td><td>Output enable pin
When OE = High, outputs shift data and data input contents.
When OE = L, controls the LCD panel drive output to V_{OFF} level, regardless of shift data and data input contents. Note that the contents of the shift registers are not cleared. Those operations are performed asynchronously to CPV.</td></tr>
<tr><td>MODE</td><td>I</td><td>Output number switching pin
Determines mode (241 or 211 output pin mode) for the LCD panel drive output pins. The pin is pulled up to V_{DD}.
• MODE = Low, 241 output pin mode.
• MODE = High, 211 output pin mode. (G107 to G136 output V_{OFF} level.)
Use the pin at DC level. When High level = V_{DD}; when Low level = V_{SS}.</td></tr>
<tr><td>Test</td><td>I</td><td>Test pin.
Leave the pin open.
The pin is pulled down to V_{SS} in the T6L70.</td></tr>
<tr><td>G1 to G241</td><td>O</td><td>LCD panel drive pins.</td></tr>
<tr><td>V_{OFF}</td><td></td><td>LCD off level input pin.</td></tr>
<tr><td>V_{GG}</td><td></td><td>Power supply pin for controlling LCD.</td></tr>
<tr><td>V_{EE}</td><td></td><td>Power supply pin for controlling LCD.</td></tr>
<tr><td>V_{DD}</td><td></td><td>Power supply pin for internal logic.</td></tr>
<tr><td>V_{SS}</td><td></td><td>Power supply pin for internal logic.</td></tr>
</table>

Operation Description

(1) Shift data transfer method

MODE Pin	D/U Pin	Shift Data Input		Data Transfer Direction
		Input	Output	
H (211 output pin mode)	L	DI/O	DO/I	G1 → G2 → G3 → ··· → G105 → G106 → G137 → G138 → ··· → G239 → G240 → G241
H (211 output pin mode)	H	DO/I	DI/O	G241 → G240 → G239 → ··· → G138 → G137 → G106 → G105 → ··· → G3 → G2 → G1
L (241 output pin mode)	L	DI/O	DO/I	G1 → G2 → G3 → ··· → G239 → G240 → G241
L (241 output pin mode)	H	DO/I	DI/O	G241 → G240 → G239 → ··· → G3 → G2 → G1

Shift data are latched in sync with the rising edge of shift clock CPV.

Shift data are output in sync with the falling edge of CPV corresponding to G241 data at D/U = Low level, and with the falling edge of CPV corresponding to G1 data at D/U = High.

(See the timing chart.)

(2) LCD control pin

Output from the LCD panel drive output pins (Gn: n = 1 to 241) is controlled according to the shift data register data (An) and input pin D/U as follows:

- LCD panel drive output at D/U = Low: Gn (n = 1 to 241)

An	An + 1	An + 2	Output
0	0	×	V_{OFF}
0	1	×	V_{EE}
1	0	×	V_{GG}
1	1	0	V_{EE}
1	1	1	V_{GG}

×: Don't care

- LCD panel drive output at D/U = High: Gn (n = 1 to 241)

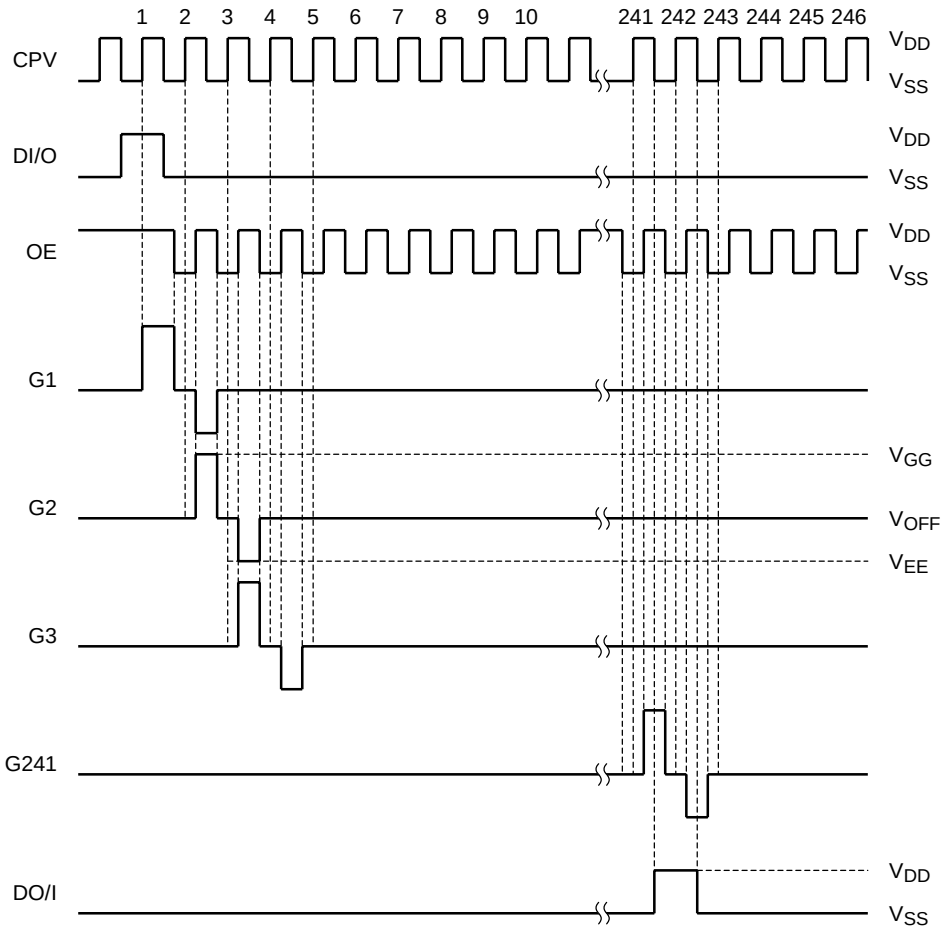
An	An – 1	An – 2	Output
0	0	×	V_{OFF}
0	1	×	V_{EE}
1	0	×	V_{GG}
1	1	0	V_{EE}
1	1	1	V_{GG}

×: Don't care

Note that in 211 output pin mode (MODE = High), LCD panel drive output pins G107 to G136 output V_{OFF} level regardless of the shift data.

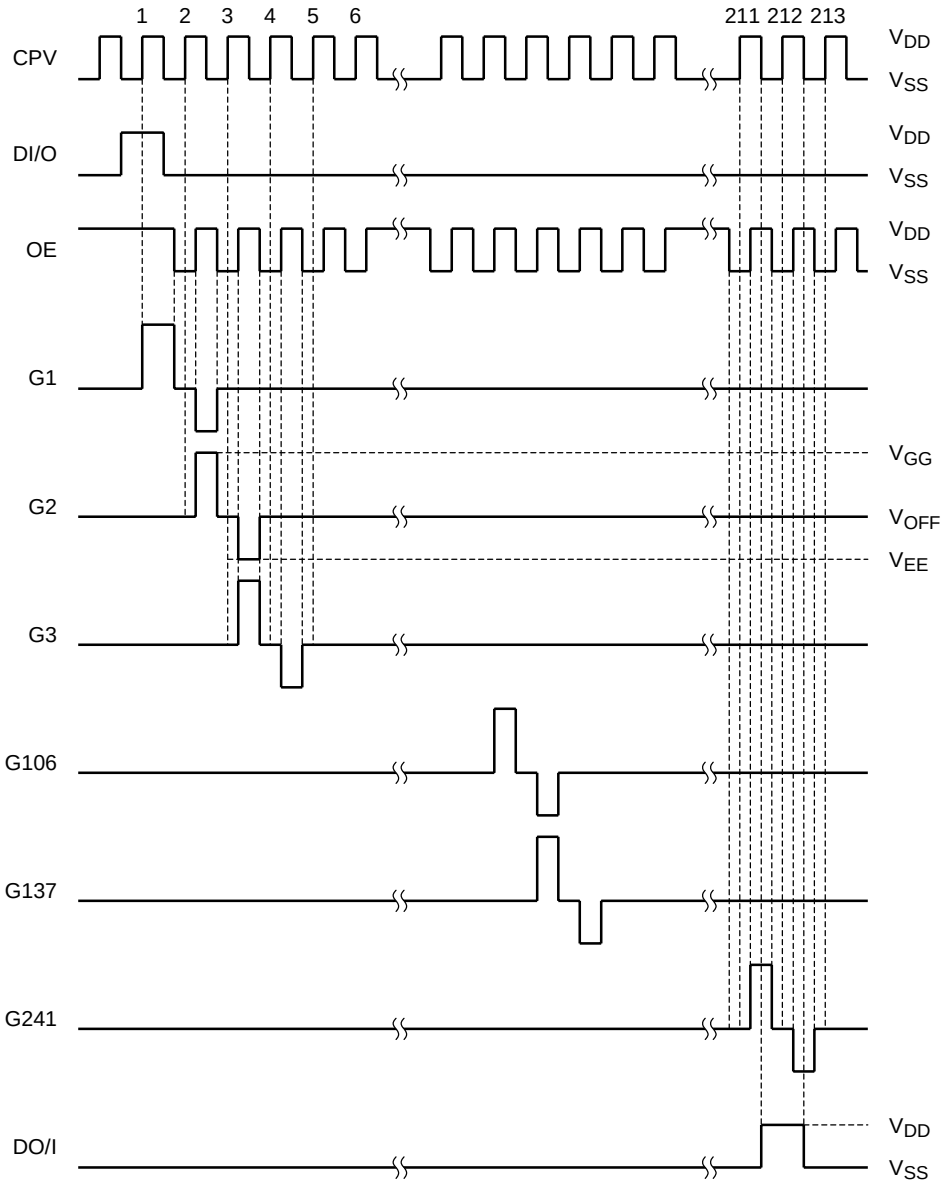
Timing Chart 1

- **1CPV input drive (D/U = Low level, MODE = High level)**



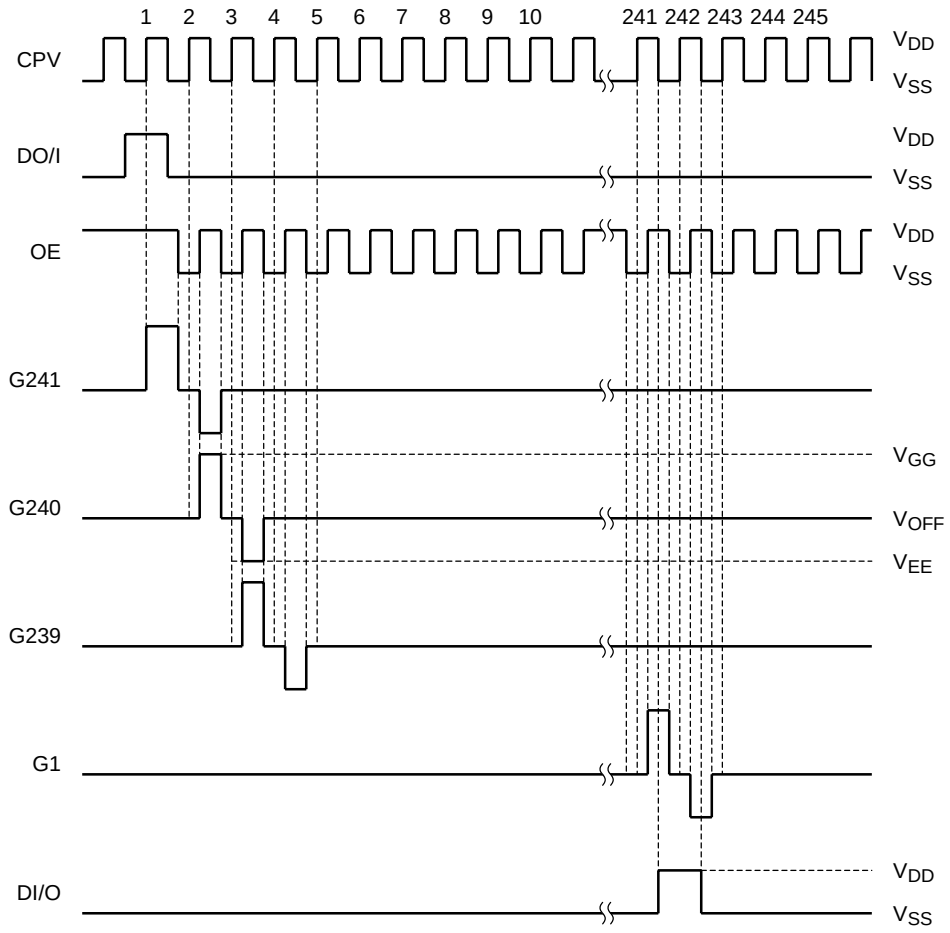
Timing Chart 2

- **1CPV input drive (D/U = Low level, MODE = High level)**



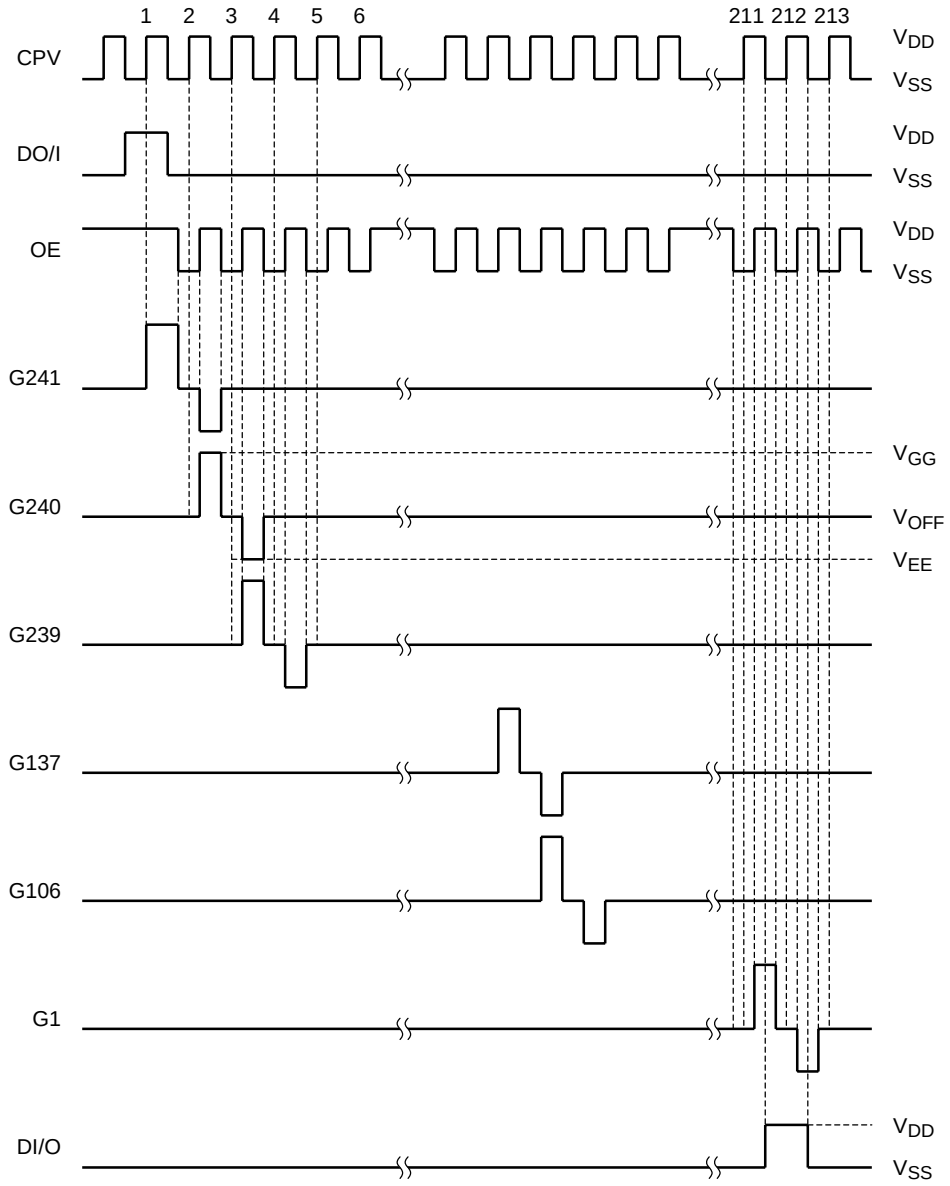
Timing Chart 3

- **1CPV input drive (D/U = High level, MODE = Low level)**



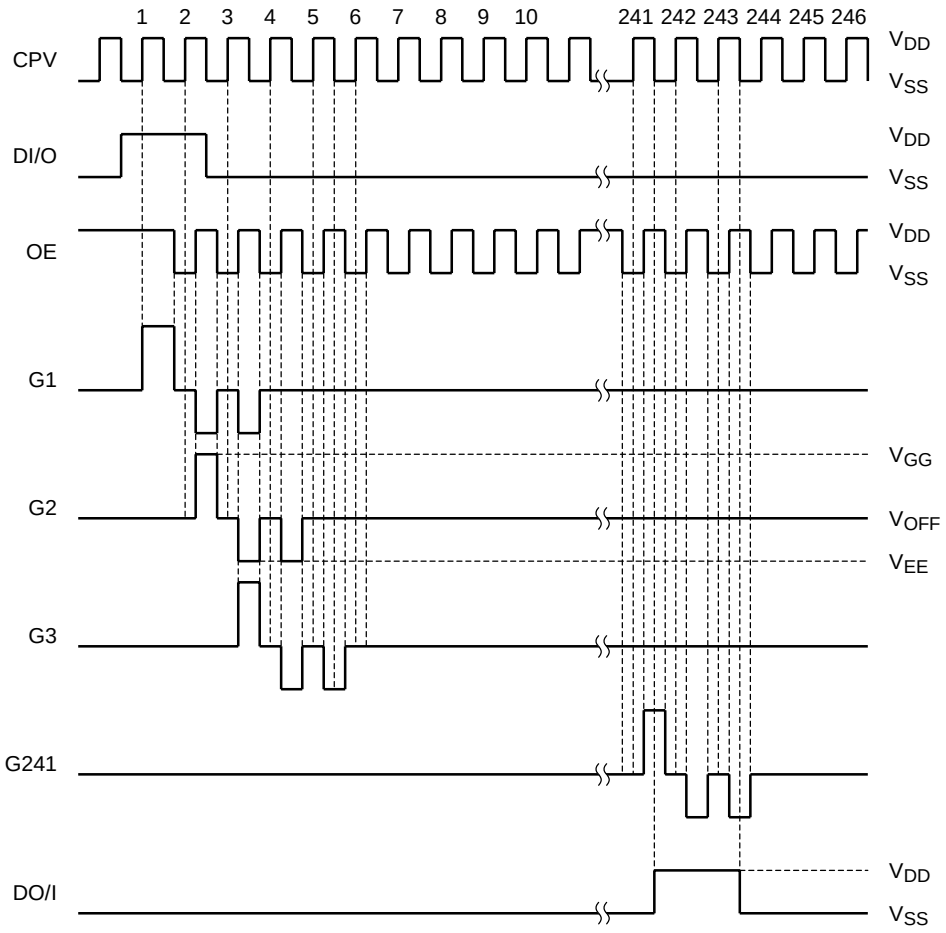
Timing Chart 4

- **1CPV input drive (D/U = High level, MODE = High level)**



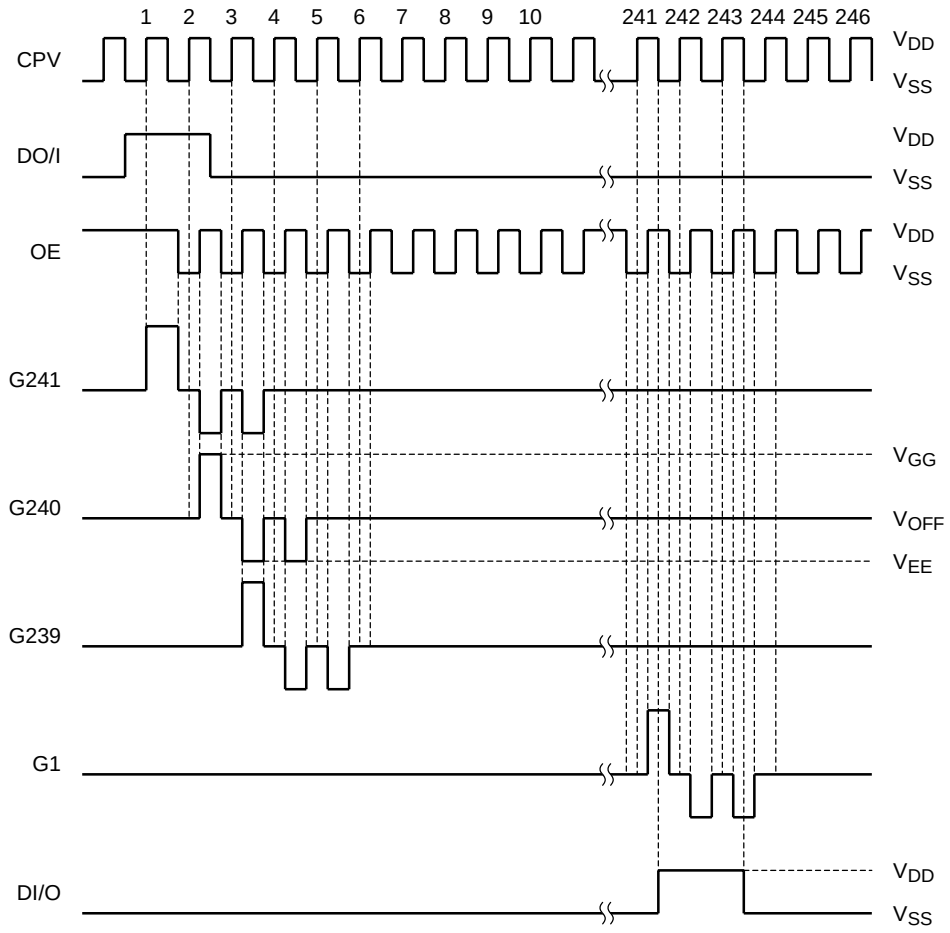
Timing Chart 5

- **2CPV input drive (D/U = Low level, MODE = Low level)**



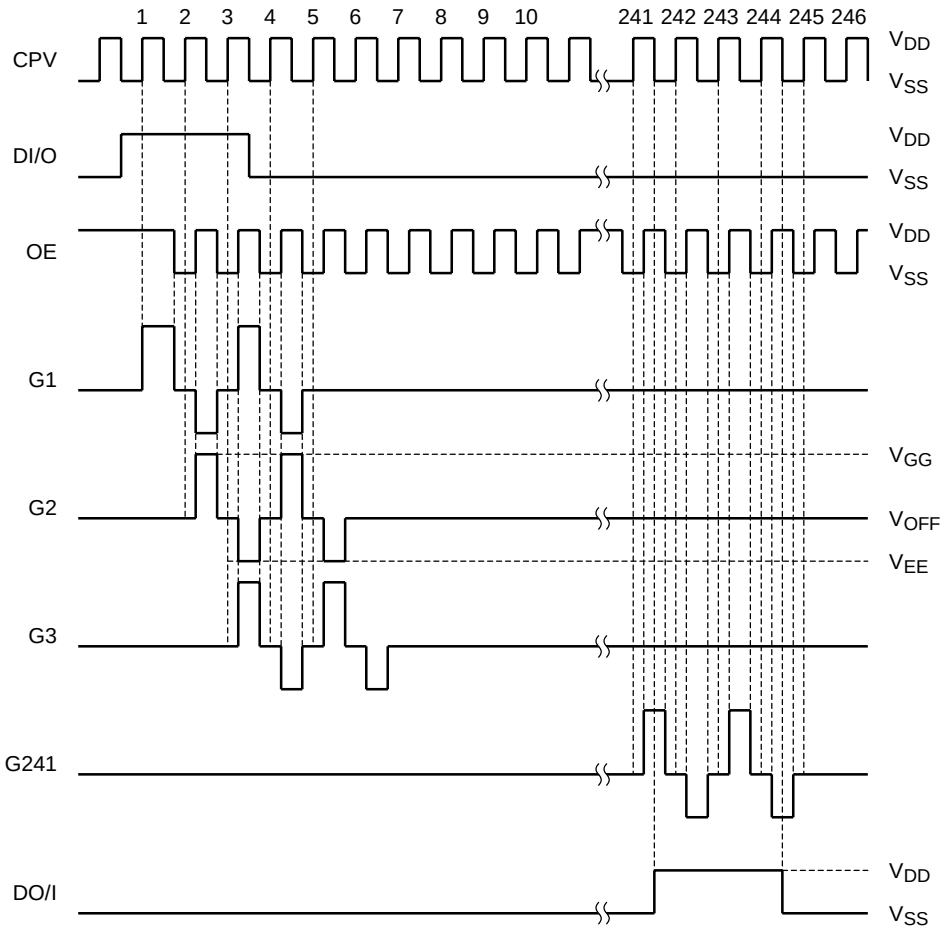
Timing Chart 6

- **2CPV input drive (D/U = High level, MODE = Low level)**



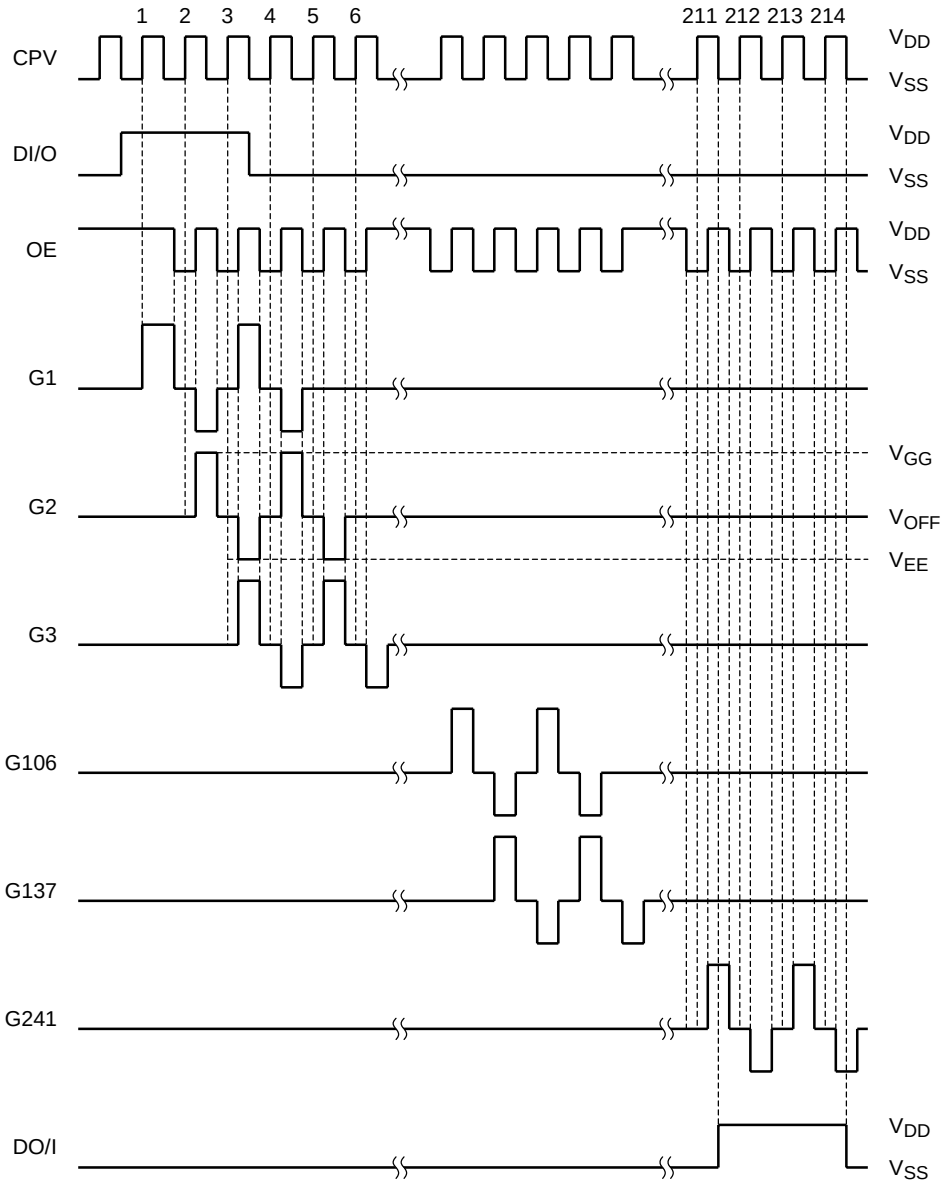
Timing Chart 7

- **3CPV input driver (D/U = Low level, MODE = Low level)**



Timing Chart 8

- **3CPV input driver (D/U = Low level, MODE = High level)**



Maximum Ratings (V_{SS} = 0 V)

Characteristics	Symbol	Rating	Unit	Relevant pin
Supply voltage (1)	$V_{GG} - V_{EE}$	−0.3 to 43.0	V	
Supply voltage (2)	V_{DD}	−0.3 to 6.0	V	
Supply voltage (3)	V_{EE}	−20.0 to 0.3	V	
Input voltage	V_{IN}	V_{SS} − 0.3 to V_{DD} + 0.3	V	DI/O, DO/I, CPV, OE, MODE
LCD off level input voltage	V_{OFF}	V_{EE} − 0.3 to V_{GG} + 0.3	V	
Storage temperature	T_{stg}	−55 to 125	°C	

Operating Range (V_{SS} = 0 V)

Characteristics	Symbol	Rating	Unit
Supply voltage (1)	V_{GG}	15 to 30	V
	$V_{GG} - V_{EE}$	20 to 40	
Supply voltage (2)	V_{DD}	2.7 to 3.6	V
Supply voltage (3)	V_{EE}	−15 to −5	V
Operating temperature	T_{opr}	−20 to 75	°C
Operating frequency	f_{CPV}	DC to 120	kHz
Output load capacitance	C_L	1000 (max)	pF/PIN
LCD OFF level input voltage	V_{OFF}	V_{EE} to V_{EE} + 10	V

Electrical Characteristics

DC Characteristics (V_{SS} = 0 V, V_{DD} = 2.7 to 3.6 V, Ta = –20 to 75°C)

Characteristics		Symbol	Test circuit	Test Condition	Min	Typ.	Max	Unit	Relevant Pin
Input voltage	Low level	V_{IL}	—	—	V_{SS}	—	0.3 × V_{DD}	V	(Note1)
	High level	V_{IH}	—	—	0.7 × V_{DD}	—	V_{DD}		
Output voltage	Low level	V_{OL}	—	I_{OL} = 40 μA	V_{SS}	—	V_{SS} + 0.3 V	V	DI/O, DO/I
	High level	V_{OH}	—	I_{OH} = –40 μA	V_{DD} – 0.3 V	—	V_{DD}		
Output resistance	V_{GG} level	R_{GG}	—	V_{OUT} = V_{GG} – 0.5 V (Note 2)	—	—	1.0	kΩ	G1~G241
	V_{OFF} level	R_{OFF}	—	V_{OUT} = V_{OFF} + 0.5 V(Note 2)					
	V_{EE} level	R_{EE}	—	V_{OUT} = V_{EE} + 0.5 V (Note 2)					
Pull-up resistance			—	—	—	400	—	kΩ	MODE
Input leakage current		I_{IN}	—	—	–1.0	—	1.0	μA	(Note1)
Current dissipation (1)		I_{GG}	—	(Note 3)	—	—	100	μA	V_{GG}
Current dissipation (2)		I_{DD}	—	(Note 3)	—	—	500	μA	V_{DD}
Current dissipation (3)		I_{SS}	—	(Note 3)	—	—	100	μA	V_{SS}

Note 1: DI/O, DO/I, CPV, OE, D/U, MODE

Note 2: V_{GG} – V_{EE} = 35 V or more

Note 3: f_{CPV} = 50 kHz, V_{DD} = 3.3 V, V_{GG} = 25 V, V_{OFF} = –5 V, V_{EE} = –10 V, no load

AC Characteristics (V_{SS} = 0 V, V_{DD} = 2.7 to 3.6 V, Ta = –20 to 75°C)

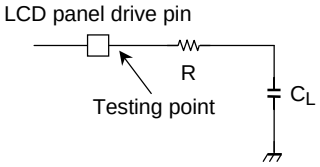
t_r/t_f = 6 ns/6 ns

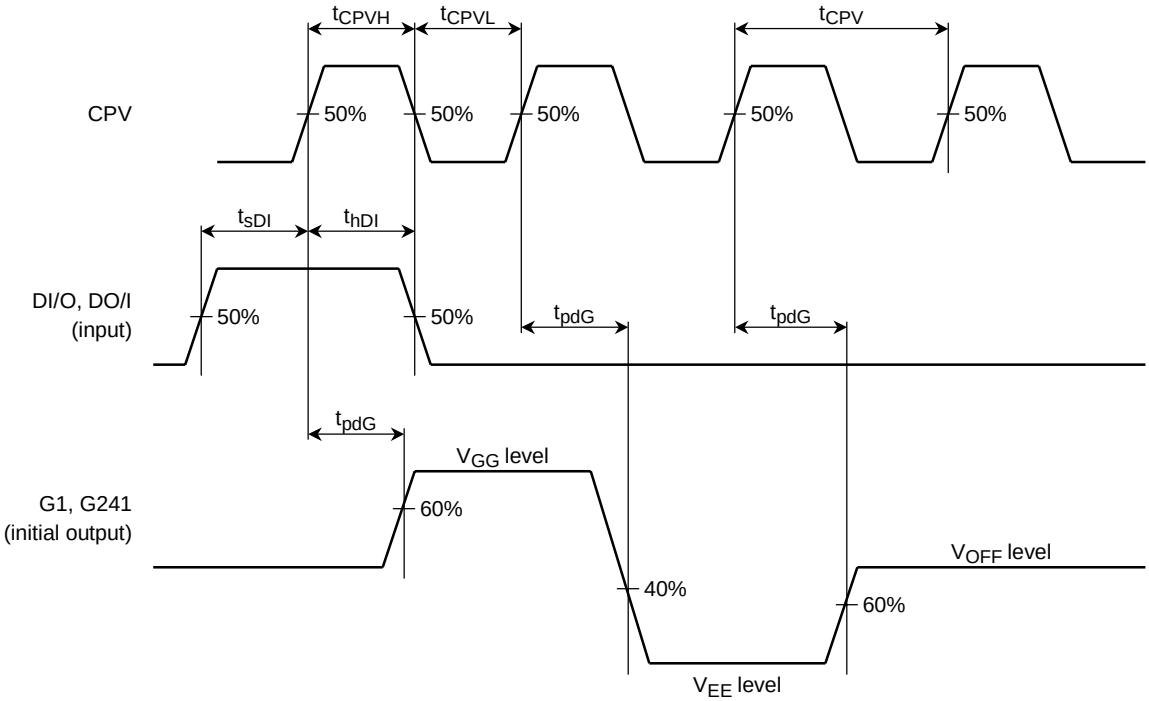
Characteristics	Symbol	Test circuit	Test Condition	Min	Max	Unit
Clock cycle	t_{CPV}	—	—	8.0	—	μs
Clock pulse width (L)	t_{CPVL}	—	—	2.0	—	μs
Clock pulse width (H)	t_{CPVH}	—	—	2.0	—	μs
OE enable time	t_{wOE}	—	Output control by OE = “L”	1.0	—	μs
Data setup time	t_{sDI}	—	—	0.5	—	μs
Data hold time	t_{hDI}	—	—	0.5	—	μs
Output delay time (1)	t_{pdDO}	—	C_L = 50pF	—	1.0	μs
Output delay time (2)	t_{pdG}	—	(Note 4)	—	1.0	μs
Output delay time (3)	t_{pdOE}	—	(Note 4)	—	1.0	μs

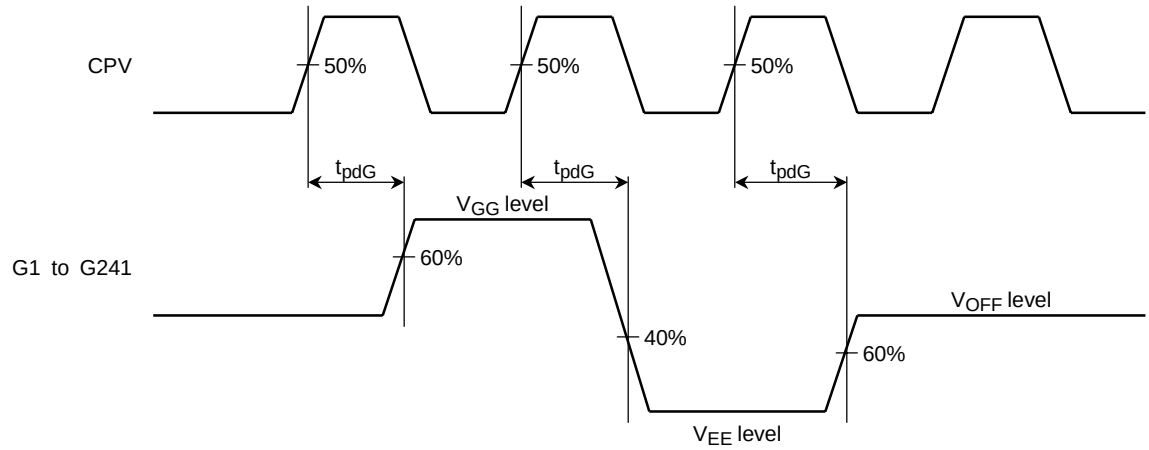
Note 4: Test condition: V_{GG} – V_{EE} = 35 V, V_{OFF} = V_{EE} to V_{EE} + 10 V

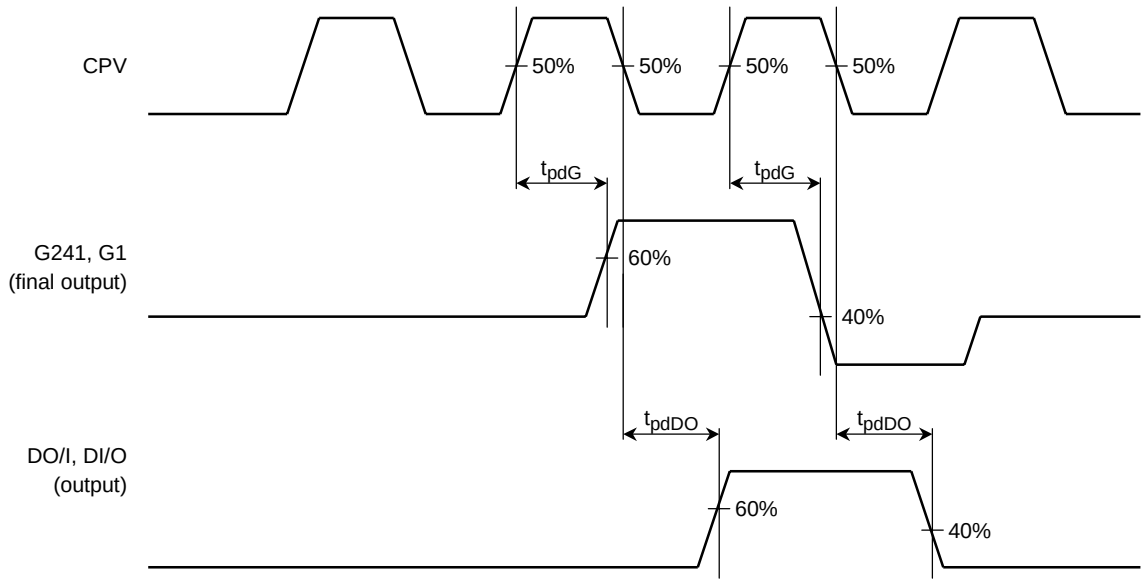
(1) C_L = 700 pF, R = 7 kΩ

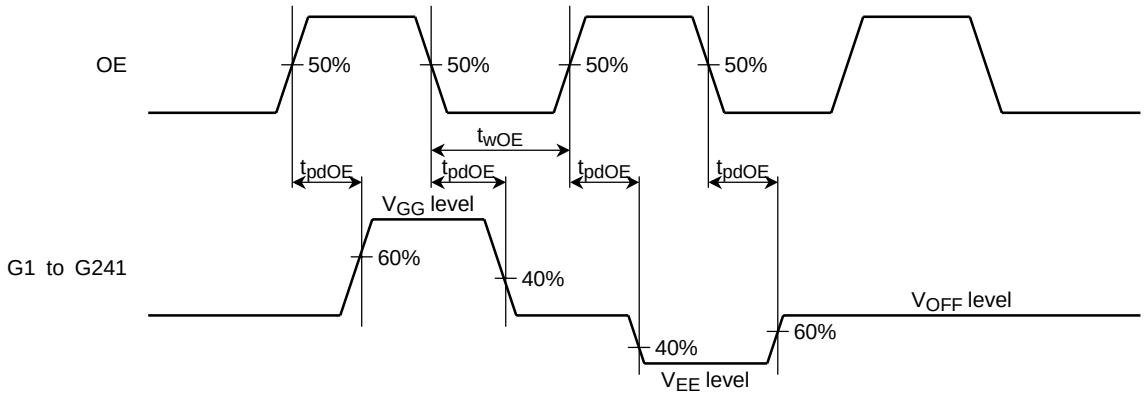
(2) C_L = 1000 pF, R = 3 kΩ




tCPVH
tCPVL
tCPV
CPV
50%
50%
50%
50%
50%
tsDI
thDI
DI/O, DO/I
(input)
50%
50%
tpdG
tpdG
tpdG
VGG level
G1, G241
(initial output)
60%
VOFF level
40%
60%
VEE level


CPV
50%
50%
50%
tpdG
tpdG
tpdG
VGG level
G1 to G241
60%
VOFF level
40%
60%
VEE level

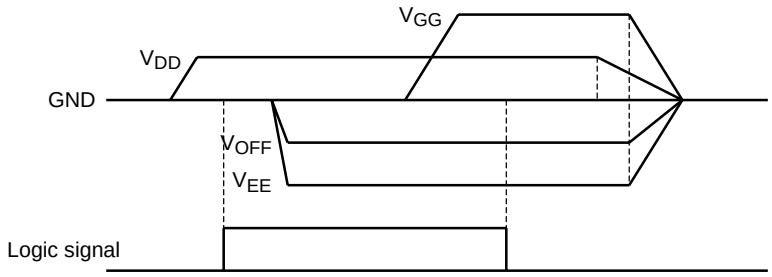

CPV
50%
50%
50%
50%
tpdG
tpdG
G241, G1
(final output)
60%
40%
tpdDO
tpdDO
DO/I, DI/O
(output)
60%
40%


OE
50%
50%
50%
50%
twOE
tpdOE
tpdOE
tpdOE
tpdOE
VGG level
G1 to G241
60%
40%
VOFF level
60%
40%
VEE level

Power Supply Sequence

At power on, supply power in order of V_{DD} → logic signal → V_{EE}, V_{OFF} → V_{GG}. At power off, turn off in order of logic signal, V_{DD} → V_{EE}, V_{OFF}, then V_{GG}.

At power off, $V_{GG} \geqq V_{DD} \geqq V_{OFF} \geqq V_{EE}$.



*Logic signal includes High and Low levels (DC voltage) as well as signal rise and fall.

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