TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T6L60

Gate Driver for TFT LCD Panels

The T6L60 is a 150/154-channel output gate driver for TFT LCD panels. This device accepts external input of the panel drive voltage, allowing you to change the low-level output voltage. Thus, this device can be used for various TFT LCD panel drive systems.

Unit: mm

T6L60	User area pitch	
	IN	OUT
(SAN, 3NS)	0.80000	0.14979

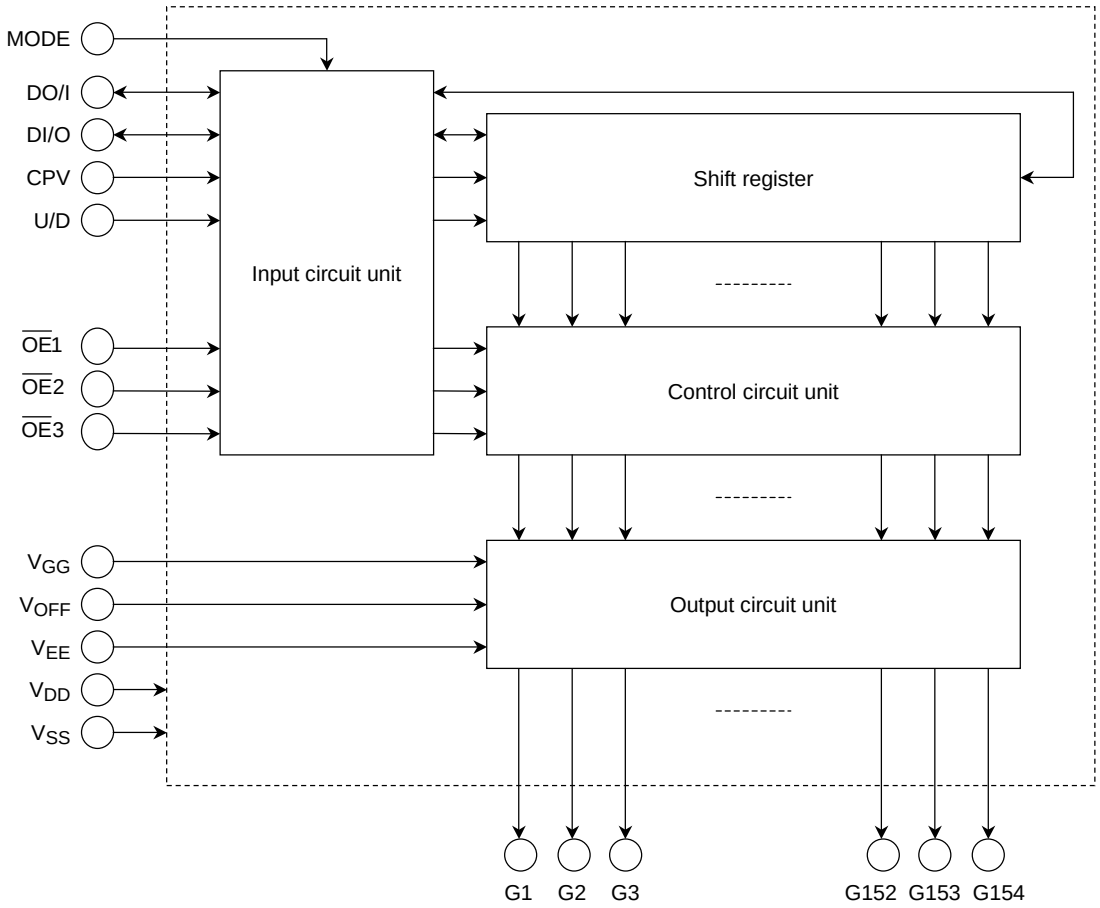
Please contact Toshiba or a distributor for the latest TCP specification and product line-up.

TCP (Tape Carrier Package)

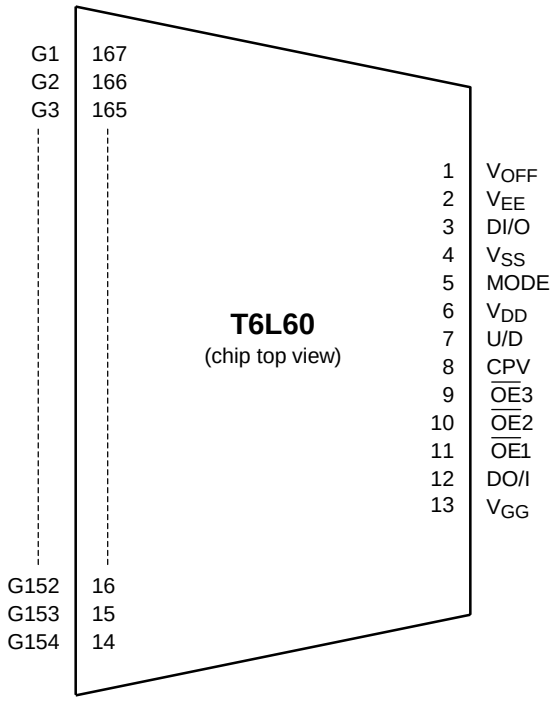
Features

- LCD drive output pins : Switchable between 150 and 154 pins
- LCD drive voltage : max V_{EE} + 40 V
- Data transfer method : Bidirectional shift register
- Operating temperature: −20 to 75°C
- Package : Tape carrier package (TCP)

Block Diagram



Pin Assignment



The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributors for the latest TCP specification.

Pin Function

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>DI/O
DO/I</td><td>I/O</td><td>Vertical shift data I/O pins
These pins are used to input and output shift data. These pins are switched between input and output by setting the U/D pin as shown below.
<table>
<tr><th>U/D</th><th>DI/O</th><th>DO/I</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table>
When set for input
This pin is used to feed data into the shift registers at the first stage of the LCD driver. The data is latched into the shift registers at the rising edge of CPV.

When set for output
When two or more T6L60s are cascaded, this pin outputs the data to be fed into the next stage. This data changes state synchronously with the falling edge of CPV.</td></tr>
<tr><td>U/D</td><td>I</td><td>Transfer direction select pin
This pin specifies the direction in which data is transferred through the shift registers. The shift register data is shifted synchronously with each rising edge of CPV as follows:
When U/D is high, data is shifted in the direction
G1 → G2 → G3 → G4 → ··· → G154
When U/D is low, the direction is reversed to give
G154 → G153 → G152 → G151 → ··· → G1
The voltage applied to this pin must be a DC-level voltage that is either high (V_{DD}) or low (V_{SS} or V_{EE})</td></tr>
<tr><td>CPV</td><td>I</td><td>Vertical shift clock
This is the shift clock for the shift registers. Data is shifted through the shift registers synchronously with the rising edge of CPV.</td></tr>
<tr><td>$\overline{OE}$1 to $\overline{OE}$3</td><td>I</td><td>Output enable pins
These signals control the data appearing at the LCD panel drive pins (G1 through G154).
$\overline{OE}$ doesn't synchronize with the CPU.
The V_{OFF} voltage is output when $\overline{OE}$1 to $\overline{OE}$ 3 are high; normal shift data is output when $\overline{OE}$ 1 to $\overline{OE}$ 3 are low.</td></tr>
<tr><td>MODE</td><td>I</td><td>Output channels select pin
This signal selects either 150-pin mode or 154-pin mode for the LCD panel driver.
When MODE = high, 150-pin mode is selected, in which case G76 through G79 are not used. (V_{OFF} level)
When MODE = low, 154-pin mode is selected.</td></tr>
<tr><td>G1 to G154</td><td>O</td><td>LCD panel drive pins
These pins output the shift register data or the voltage applied to V_{GG} or V_{OFF} depending on the control signals $\overline{OE}$1 to $\overline{OE}$ 3.</td></tr>
<tr><td>V_{GG}</td><td>—</td><td>Power supply for LCD drive</td></tr>
<tr><td>V_{OFF}</td><td>—</td><td>Analog reference voltage
These pins accept as their input the OFF level at the LCD panel drive pins (G1 through G154).</td></tr>
<tr><td>V_{EE}</td><td>—</td><td>Power supply for LCD drive</td></tr>
<tr><td>V_{DD}</td><td>—</td><td>Power supply for the internal logic</td></tr>
<tr><td>V_{SS}</td><td>—</td><td>Power supply for the internal logic</td></tr>
</table>

Device Operation

(1) Shift data transfer method

Mode Pin	U/D Pin	Shift Data		Data Transfer Method
		Input	Output	
H (150-out)	H	DI/O	DO/I	G1 → G2 → G3 → ··· → G75 → G80 → ··· → G154
	L	DO/I	DI/O	G154 → G153 → G152 → ··· → G80 → G75 → ··· → G1
L (154-out)	H	DI/O	DO/I	G1 → G2 → G3 → G4 → ··· → G154
	L	DO/I	DI/O	G154 → G153 → G152 → G151 → ··· → G1

The input data (DI/O or DO/I) is latched into the internal register synchronously with the rising edge of the shift clock CPV. At the same time that the data is shifted to the next register at the next rise of CPV, new vertical shift data is latched into.

In the output operation, the data in the last shift register (G154 or G1) is output synchronously with the falling edge of CPV. (The output high voltage is the V_{DD} level; the output low voltage is the V_{SS} level.)

Note: The outputs of G76 to G79 are V_{OFF} level in 150 output mode.

(2) LCD panel drive outputs

The LCD panel drive outputs are controlled by $\overline{OE}1$ to $\overline{OE}3$ as shown below.

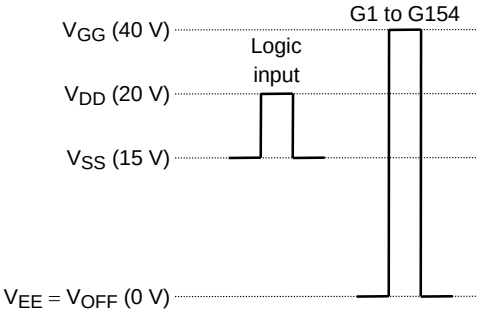
The following combinations of mode pins and output enable pins don´t depend on the polarity of U/D pins; hence, LCD panel drive outputs for LCD panel drive pins controlled by $\overline{OE}$ are the same when the U/D pins is High or Low.

Mode Pin	Output Enable Pin	LCD Panel Drive Outputs LCD Panel Drive Pins Controller by	Output
H (150-out)	$\overline{OE}1$ = "H"	G1, G4, G7, ···G73, G80 ··· G149, G152	V_{OFF} level
	$\overline{OE}2$ = "H"	G2, G5, G8, ···G74, G81 ··· G150, G153	
	$\overline{OE}3$ = "H"	G3, G6, G9, ···G75, G82 ··· G151, G154	
	$\overline{OE}1$ = "L"	G1, G4, G7, ···G73, G80 ··· G149, G152	Normal data output
	$\overline{OE}2$ = "L"	G2, G5, G8, ···G74, G81 ··· G150, G153	
	$\overline{OE}3$ = "L"	G3, G6, G9, ···G75, G82 ··· G151, G154	
L (154-out)	$\overline{OE}1$ = "H"	G1, G4, G7, ···G148, G151, G154	V_{OFF} level
	$\overline{OE}2$ = "H"	G2, G5, G8, ···G149, G152	
	$\overline{OE}3$ = "H"	G3, G6, G9, ···G150, G153	
	$\overline{OE}1$ = "L"	G1, G4, G7, ···G148, G151, G154	Normal data output
	$\overline{OE}2$ = "L"	G2, G5, G8, ···G149, G152	
	$\overline{OE}3$ = "L"	G3, G6, G9, ···G150, G153	

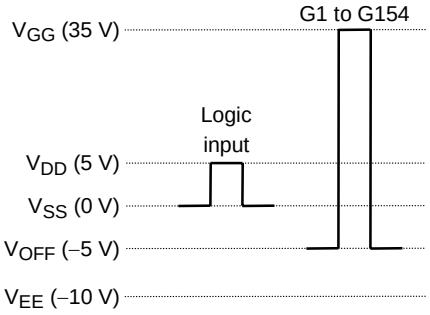
(3) Voltage setting

The V_{OFF} level, which sets the LCD panel drive's output low level, can take on any value between V_{EE} to V_{EE} + 6 V.

(Example 1) Positive voltage output
$V_{GG} - V_{OFF}$ = 40 V
$V_{OFF} - V_{EE}$ = 0 to 6 V
$V_{SS} - V_{EE}$ = 5 to 15 V



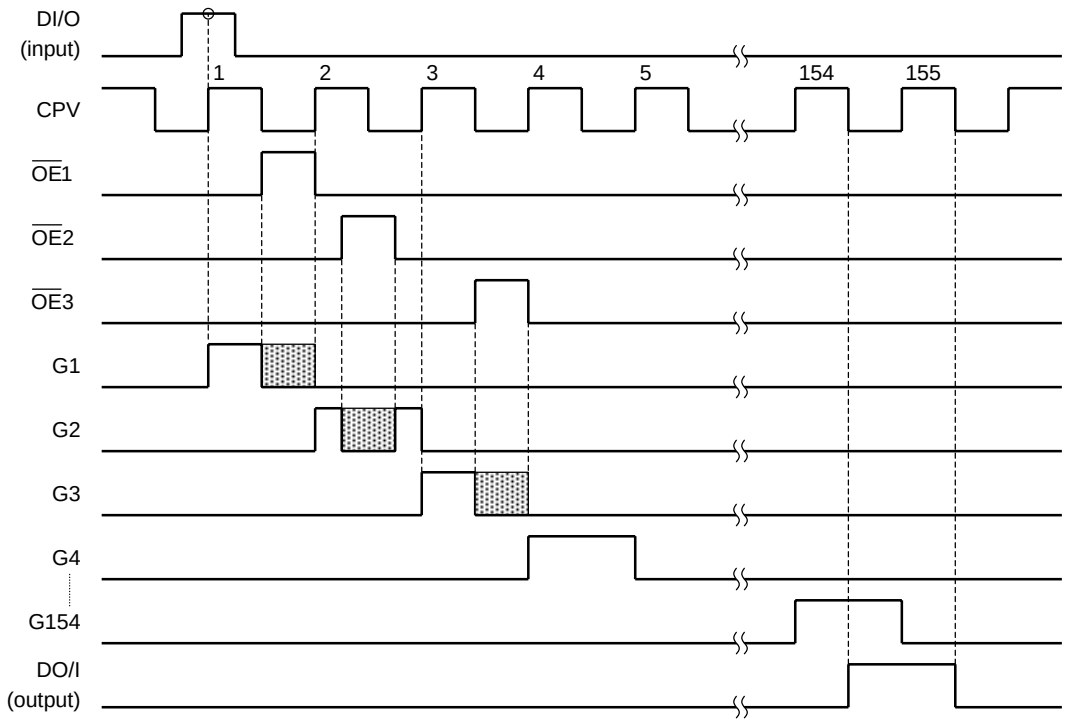
(Example 2) Negative voltage output
$V_{GG} - V_{OFF}$ = 40 V
$V_{OFF} - V_{EE}$ = –10 to –4 V
$V_{SS} - V_{EE}$ = –10 to 0 V



Note: The logic input here means input pins DI/O, DO/I, CPV, MODE and $\overline{OE}1$ to $\overline{OE}3$.
The amplitude between V_{SS} and V_{DD} is applied to above pins.
Make sure that the voltage applied to the U/D pin is a high (= V_{DD}) or low (= V_{SS} or V_{EE}) DC-level voltage.

Timing Diagram 1

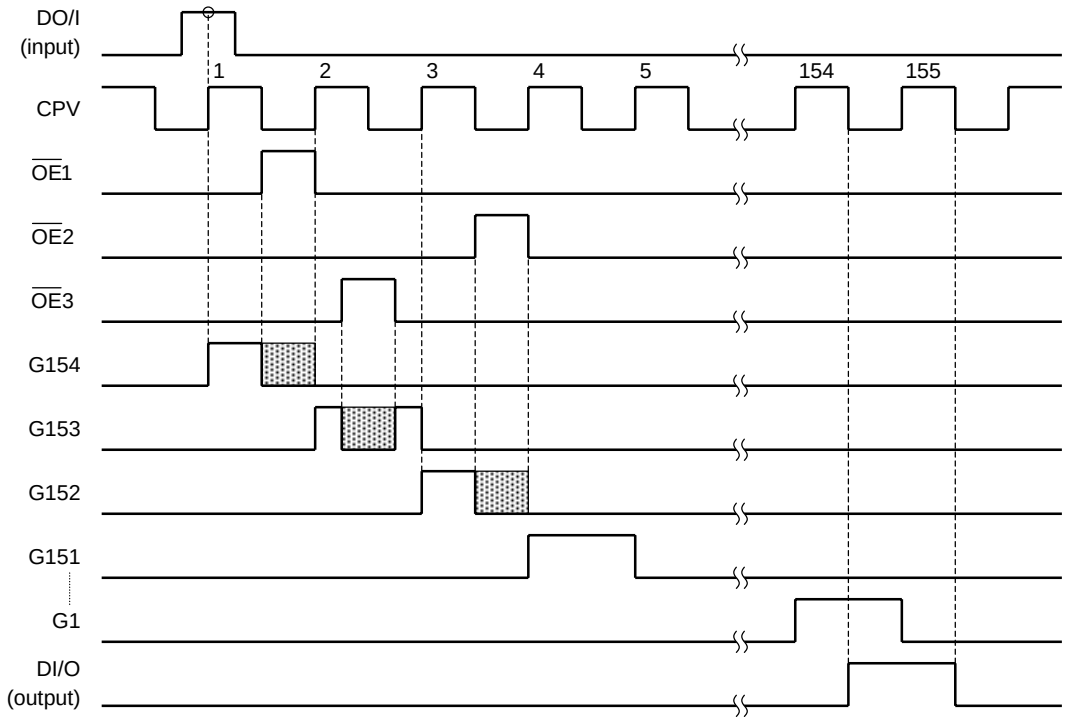
154-output-pin (MODE = low), UP mode (U/D = high)



: This part is output which is controlled (fixed to V_{OFF}) by $\overline{OE}$ pin.

Timing Diagram 2

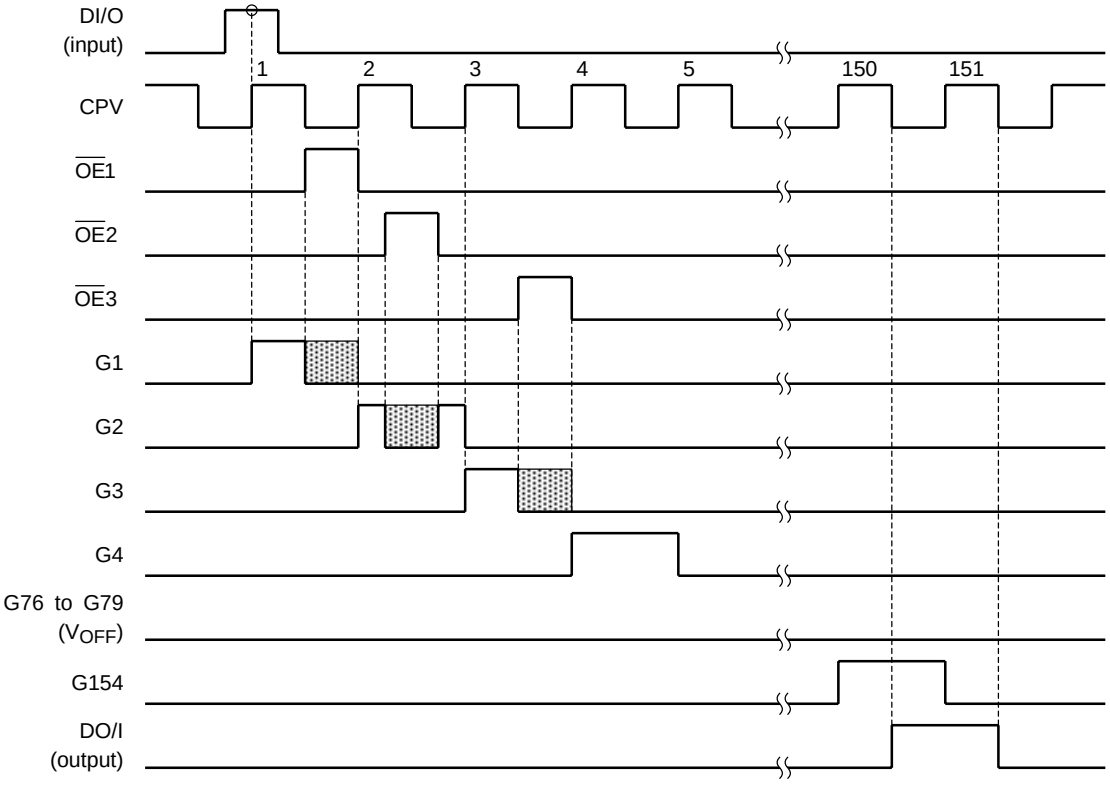
154-output-pin (MODE = low), DOWN mode (U/D = low)



: This part is output which is controlled (fixed to V_{OFF}) by $\overline{OE}$ pin.

Timing Diagram 3

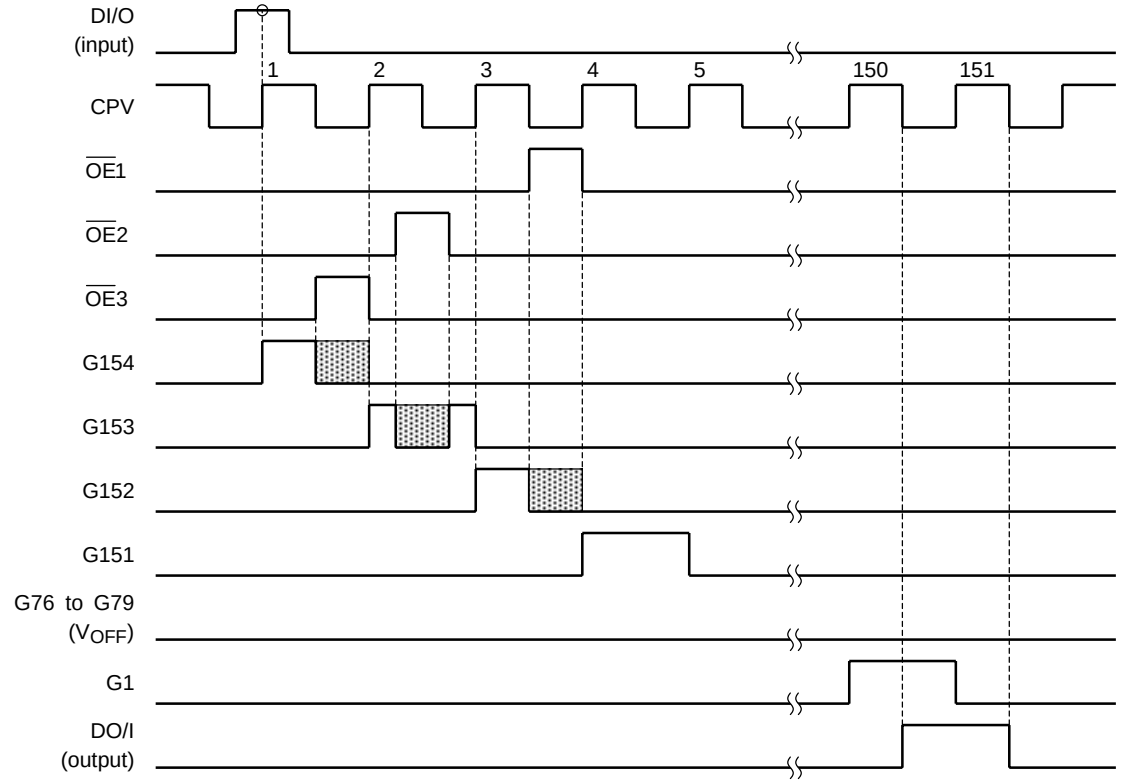
150-output-pin (MODE = high), UP mode (U/D = high)



: This part is output which is controlled (fixed to V_{OFF}) by $\overline{OE}$ pin.

Timing Diagram 4

150-output-pin (MODE = high), DOWN mode (U/D = low)



: This part is output which is controlled (fixed to V_{OFF}) by $\overline{OE}$ pin.

Absolute Maximum Ratings (V_{SS} = 0 V)

Characteristics	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	−0.3 to 22.0	V
Supply voltage (2)	V_{SS}	−0.3 to 16.5	
Supply voltage (3)	$V_{DD} - V_{SS}$	−0.3 to 7.0	
Supply voltage (4)	V_{OFF}	−0.3 to 7.0	
Supply voltage (5)	V_{GG}	−0.3 to 45.0	
Supply voltage (6)	$V_{GG} - V_{OFF}$	−0.3 to 45.0	
Input voltage	V_{IN}	V_{SS} − 0.3 to V_{DD} + 0.3	V
Storage temperature	T_{stg}	−55 to 125	°C

Recommended Operating Conditions (V_{SS} = 0 V)

Characteristics	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	5 to 15	V
Supply voltage (2)	V_{DD}	VSS + 3.0 to VSS + 5.5	
Supply voltage (3)	V_{OFF}	0 to 6	
Supply voltage (4)	$V_{GG} - V_{SS}$	17 to 25	
Operating temperature	T_{opr}	−20 to 75	°C
Operating frequency	f_{CPV}	DC to 100	kHz
Output load capacitance	C_L	300 (max)	pF/pin

Electrical Characteristics

DC Characteristics ($V_{GG} - V_{SS}$ = 17 to 25 V, V_{DD} = 3.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 75°C, V_{EE} = –15 to –5 V, V_{OFF} = V_{EE} to V_{EE} + 6 V)

Characteristics		Symbol	Test circuit	Test Condition	Min	Max	Unit	Relevant Pin
Input voltage	Low level	V_{IL}	—	—	V_{SS}	$0.1 \times (V_{DD} - V_{SS}) + V_{SS}$	V	(Note 1)
	High level	V_{IH}			$0.9 \times (V_{DD} - V_{SS}) + V_{SS}$	V_{DD}		
Output voltage	Low level	V_{OL}	—	I_{OL} = 40 μA	V_{SS}	V_{SS} + 0.4	V	DI/O, DO/I
	High level	V_{OH}		I_{OH} = –40 μA	V_{DD} – 0.4	V_{DD}		
Output resistance	Low level	R_{OL}	—	$V_{OUT} = V_{EE}$ + 0.5 V (Note 1)	—	1500	Ω	G1 to G154
	High level	R_{OH}		$V_{OUT} = V_{GG}$ – 0.5 V (Note 1)	—	1500		
Input leakage current		I_{IN}	—	—	–1	1	μA	(Note 2)
Current consumption (1)		I_{DD}	—	(Note 3)	—	1500	μA	
Current consumption (2)		I_{SS}			–200			
Current consumption (3)		I_{GG}			—	150		

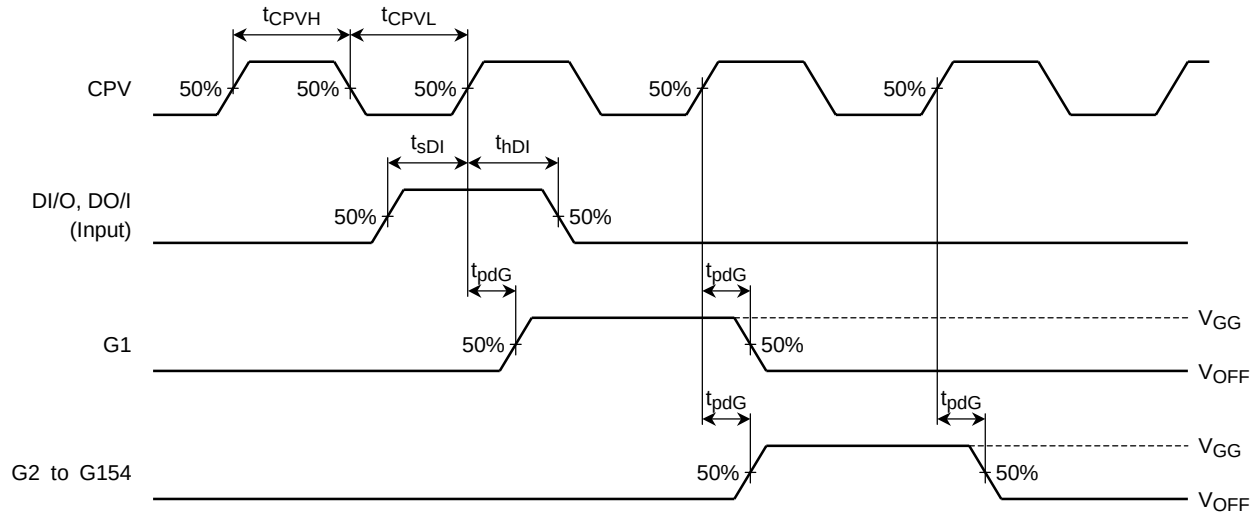
Note 1: $V_{GG} - V_{EE}$ = 25 to 35 V

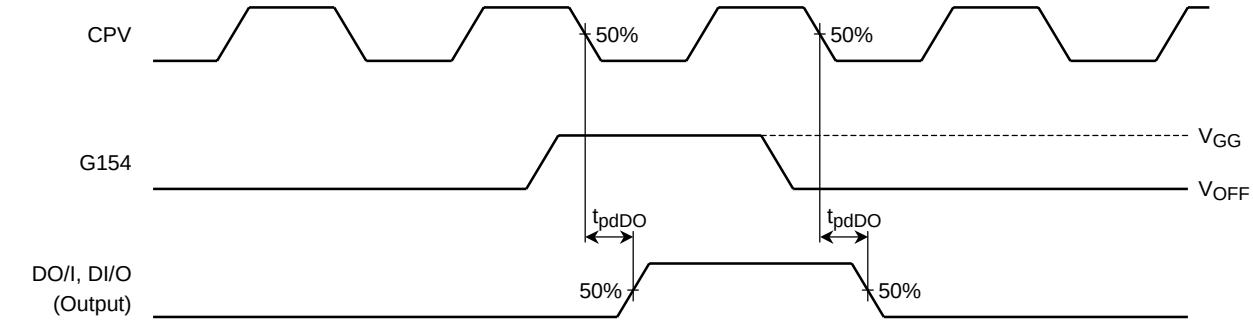
Note 2: Input pins ··· DI/O, DO/I, CPV, $\overline{OE}1$ to $\overline{OE}3$, MODE

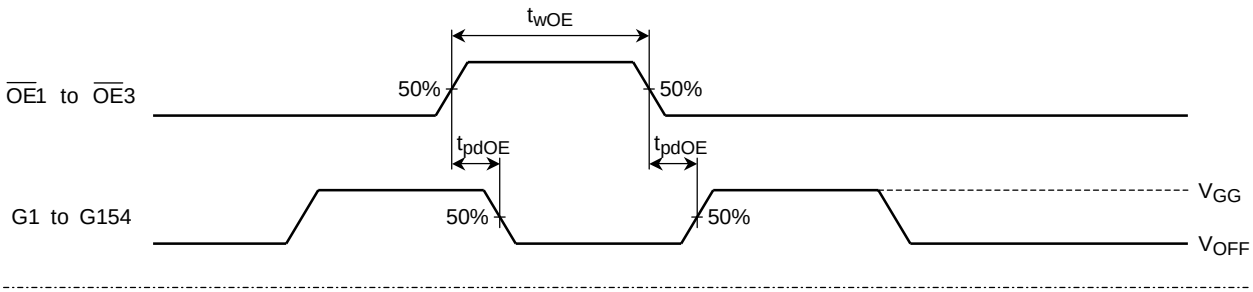
Note 3: Current consumption in 1/600-duty LCD.
Input $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, f_{CPV} = 100 kHz
Start pulse period = 104.2 Hz, $\overline{OE}1$ to $\overline{OE}3 = V_{SS}$, no load

AC Characteristics ($V_{GG} - V_{SS}$ = 17 to 25 V, V_{DD} = 3.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 75°C, V_{EE} = –15 to –5 V, V_{OFF} = V_{EE} to V_{EE} + 6 V)

Characteristics	Symbol	Test circuit	Test Condition	Min	Max	Unit
Clock period	t_{CPV}	—	—	—	100	kHz
CPV pulse width (H)	t_{CPVH}	—	—	5	—	μs
CPV pulse width (L)	t_{CPVL}	—	—	5	—	μs
Data set-up time	t_{sDI}	—	—	700	—	ns
Data hold time	t_{hDI}	—	—	700	—	ns
$\overline{OE}$ enable time	t_{wOE}	—	—	1	—	μs
Output delay time (1)	t_{pdDO}	—	C_L = 30 pF	—	1000	ns
Output delay time (2)	t_{pdG}	—	C_L = 300 pF	—	800	ns
Output delay time (3)	t_{pdOE}	—	C_L = 300 pF	—	800	ns
Input rising time	t_r	—	C_L = 300 pF	—	30	ns
Input falling time	t_f	—	C_L = 300 pF	—	30	ns
Output rising time	r-OUT	—	C_L = 300 pF	—	500	ns
Output falling time	f-OUT	—	C_L = 300 pF, $V_{OFF} = V_{EE}$ = 0 V	—	500	ns


tCPVH
tCPVL
CPV
50%
tsDI
thDI
DI/O, DO/I
(Input)
tpdG
G1
VGG
VOFF
G2 to G154

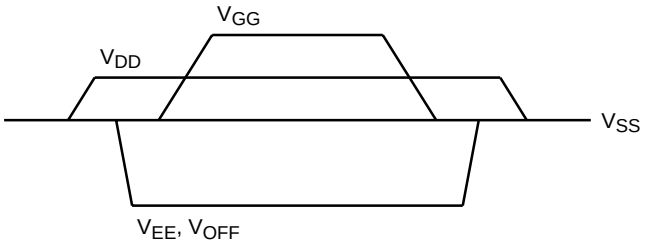

CPV
50%
G154
VGG
VOFF
tpdDO
DO/I, DI/O
(Output)


twOE
OE1 to OE3
50%
tpdOE
G1 to G154
VGG
VOFF


tr
tf
CPV,
DI/O, DO/I,
OE1 to OE3
10%
90%
r-OUT
f-OUT
G1 to G154

Power Supply Sequence

Turn power on in the order $V_{SS} \rightarrow V_{DD} \rightarrow$ Input signal $\rightarrow V_{EE} \rightarrow V_{OFF} \rightarrow V_{GG}$.
Turn power off in th reverse order.



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