TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T6L58

Gate Driver for TFT LCD Panels

The T6L58 is a 256-channel output gate driver for TFT LCD panels. This device accepts external input of the panel drive voltage, allowing you to change the low-level output voltage. Thus, this device can be used for various TFT LCD panel drive systems.

Features

- LCD drive output pins : 256 pins
- LCD drive voltage : max V_{EE} + 42 V
- Data transfer method : Bidirectional shift register
- Operating temperature : −20 to 75°C
- Package : Tape carrier package (TCP)

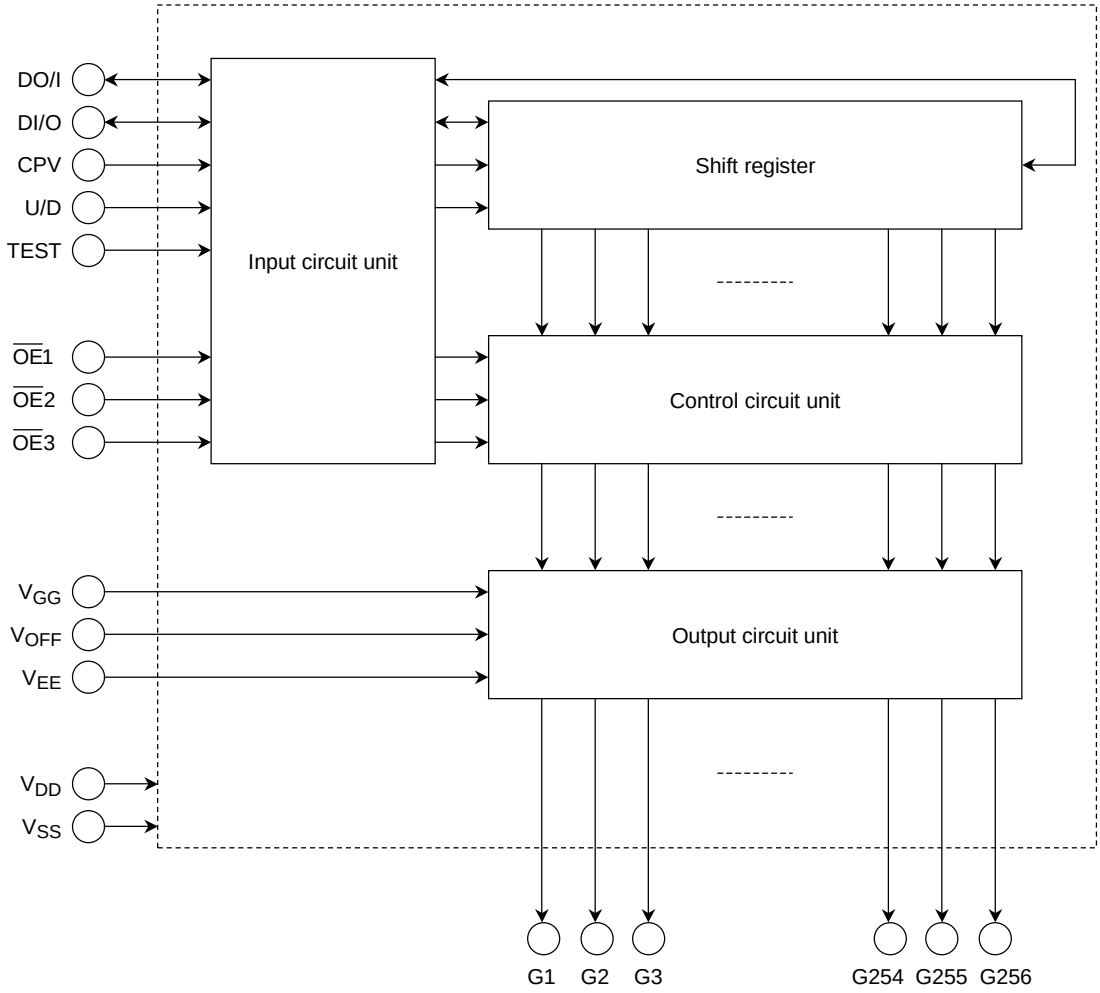
Unit: mm

T6L58	User Area Pitch	
	IN	OUT

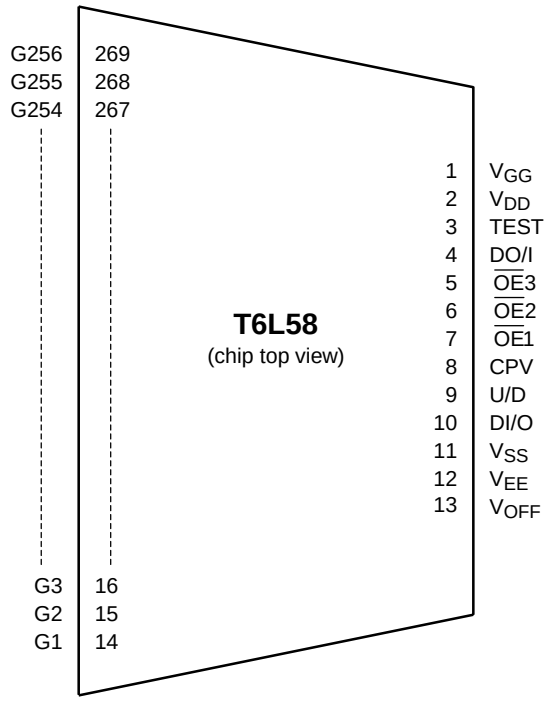
Please contact Toshiba or a distributor for the latest TCP specification and product line-up.

TCP (Tape Carrier Package)

Block Diagram



Pin Assignment



The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributors for the latest TCP specification.

Pin Function

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>DI/O
DO/I</td><td>I/O</td><td>Vertical shift data I/O pins
These pins are used to input and output shift data. These pins are switched between input and output by setting the U/D pin as shown below.
<table>
<tr><th>U/D</th><th>DI/O</th><th>DO/I</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table>
When set for input
This pin is used to feed data into the shift registers at the first stage of the LCD driver. The data is latched into the shift registers at the rising edge of CPV.
When set for output
When two or more T6L58s are cascaded, this pin outputs the data to be fed into the next stage. This data changes state synchronously with the falling edge of CPV.</td></tr>
<tr><td>U/D</td><td>I</td><td>Transfer direction select pin
This pin specifies the direction in which data is transferred through the shift registers.
The shift register data is shifted synchronously with each rising edge of CPV as follows:
When U/D is high, data is shifted in the direction
U/D = “H”: G1 → G2 → G3 → G4 → ··· → G256
When U / D is low, the direction is reversed to give
U/D = “L”: G256 → G255 → G254 → G253 → ··· → G1
The voltage applied to this pin must be a DC-level voltage that is either high (V_{DD} or low (V_{SS} V_{EE})</td></tr>
<tr><td>CPV</td><td>I</td><td>Vertical shift clock
This is the shift clock for the shift registers. Data is shifted through the shift registers synchronously with the rising edge of CPV.</td></tr>
<tr><td>$\overline{OE}$1 to $\overline{OE}$3</td><td>I</td><td>Output enable pins
These signals control the data appearing at the LCD panel drive pins (G1 through G256). $\overline{OE}$ doesn’t synchronize with the CPU.
The V_{OFF} voltage is output when $\overline{OE}$ 1 to $\overline{OE}$ 3 are high; normal shift data is output when $\overline{OE}$ 1 to $\overline{OE}$ 3 are low.</td></tr>
<tr><td>TEST</td><td>I</td><td>Test pin
This pin has been pull down; hence keep it to V_{EE} level or open.</td></tr>
<tr><td>G1 to G256</td><td>O</td><td>LCD panel drive pins
These pins output the shift register data or the voltage applied to V_{GG} or V_{OFF} depending on the control signals $\overline{OE}$ 1 to $\overline{OE}$ 3.</td></tr>
<tr><td>V_{GG}</td><td>—</td><td>Power supply for LCD drive</td></tr>
<tr><td>V_{OFF}</td><td>—</td><td>Analog reference voltage
These pins accept as their input the OFF level at the LCD panel drive pins (G1 through G256).</td></tr>
<tr><td>V_{EE}</td><td>—</td><td>Power supply for LCD drive</td></tr>
<tr><td>V_{DD}</td><td>—</td><td>Power supply for the internal logic</td></tr>
<tr><td>V_{SS}</td><td>—</td><td>Power supply for the internal logic</td></tr>
</table>

Device Operation (see timing diagram)

(1) Shift data transfer method

U/D Pin	Shift Data		Data Transfer Method
	Input	Output	
H	DI/O	DO/I	G1 → G2 → G3 → G4 → ··· → G256
L	DO/I	DI/O	G256 → G255 → G254 → ··· → G1

The input data (DI/O or DO/I) is latched into the internal register synchronously with the rising edge of the shift clock CPV. At the same time that the data is shifted to the next register at the next rise of CPV, new vertical shift data is latched into.

In the output operation, the data in the last shift register (G256 or G1) is output synchronously with the falling edge of CPV. (The output high voltage is the V_{DD} level; the output low voltage is the V_{SS} level.)

(2) LCD panel drive outputs

The LCD panel drive outputs are controlled by $\overline{OE}1$ to $\overline{OE}3$ as shown below.

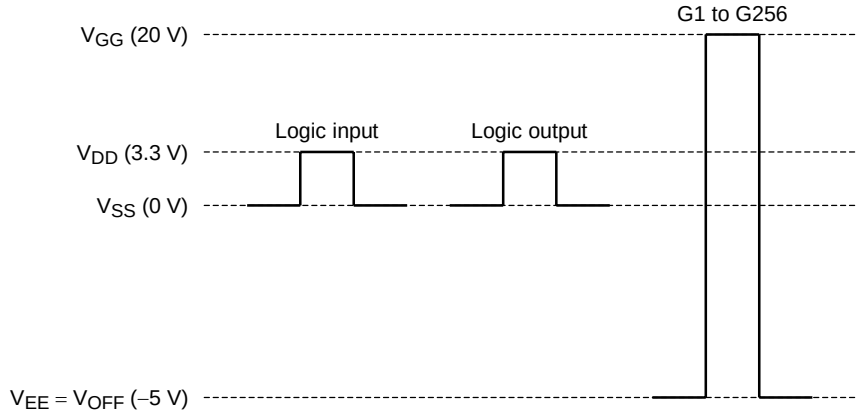
Output Enable Pin	LCD Panel Drive Outputs	Output
	LCD Panel Drive Pins Controller by $\overline{OE}$	
$\overline{OE}1$ = "H"	G1, G4, G7, ···G250, G253, G256	V_{OFF}
$\overline{OE}2$ = "H"	G2, G5, G8, ···G251, G254	
$\overline{OE}3$ = "H"	G3, G6, G9, ···G252, G255	
$\overline{OE}1$ = "L"	G1, G4, G7, ···G250, G253, G256	Normal data output
$\overline{OE}2$ = "L"	G2, G5, G8, ···G251, G254	
$\overline{OE}3$ = "L"	G3, G6, G9, ···G252, G255	

(3) Voltage setting

The V_{OFF} level, which sets the LCD panel drive's output low level, can take on any value between V_{EE} to V_{EE} + 6 V. Negative voltage output is also the same as the above.

$V_{GG} - V_{OFF} = 35$ V
$V_{OFF} - V_{EE} = 0$ to 6 V
$V_{GG} - V_{SS} = 10$ to 25 V

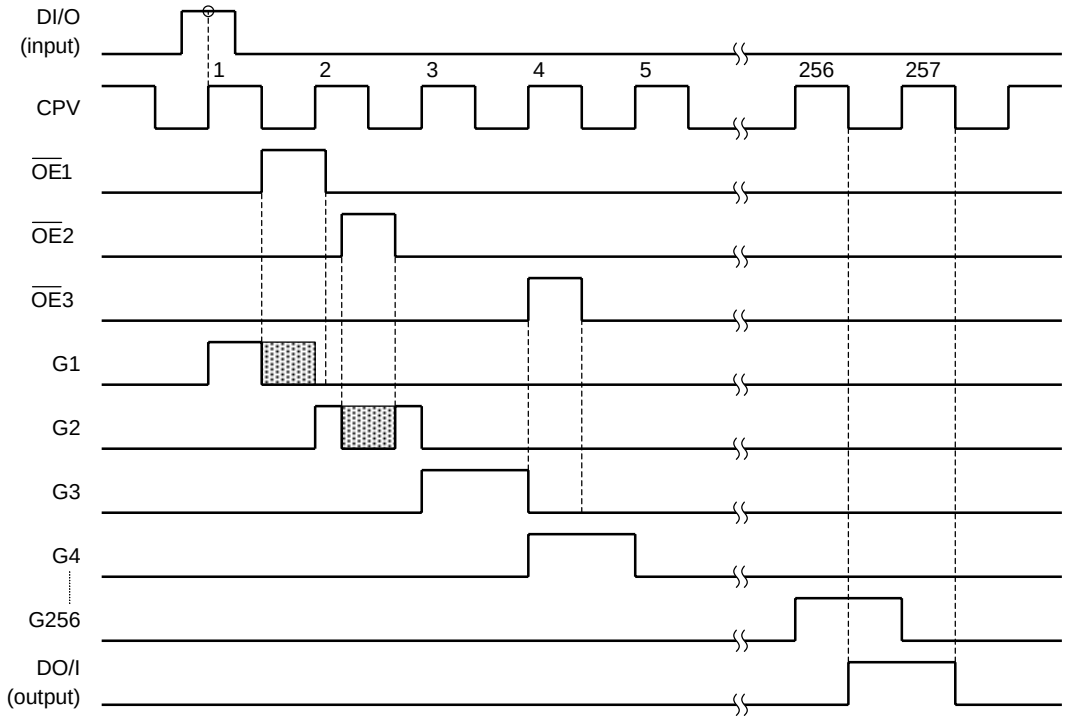
(Example)



The logic input here means input pins DI/O, DO/I, CPV and $\overline{OE}1$ to $\overline{OE}3$.
Make sure that the voltage applied to the U/D pin is a high (= V_{DD}) or low (= V_{SS} or V_{EE}) DC-level voltage.

Timing Diagram 1

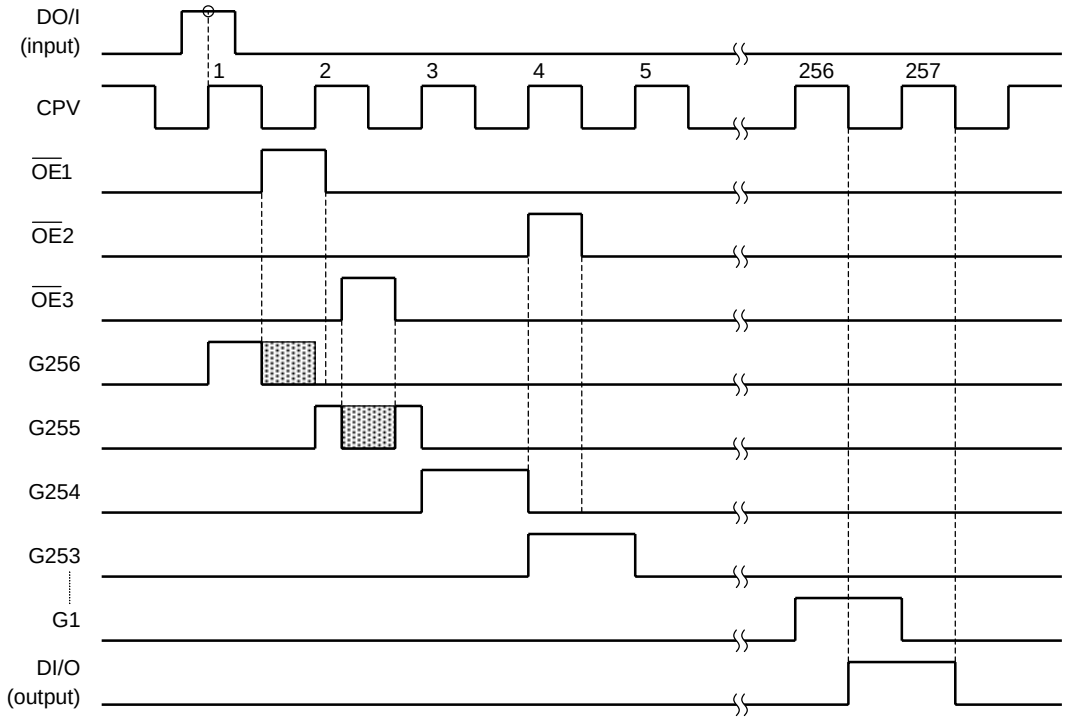
● **UP mode (U/D = high)**



: This part is output which is controlled (fixed to V_{OFF}) by $\overline{OE}$ pin.

Timing Diagram 2

● **DOWN mode (U/D = low)**



: This part is output which is controlled (fixed to V_{OFF}) by $\overline{OE}$ pin.

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	−0.3 to 6.0	V
Supply voltage (2)	V_{GG}	−0.3 to 45.0	
Supply voltage (3)	V_{EE}	−20.0 to 0.3	
Supply voltage (4)	V_{OFF}	V_{EE} − 0.3 ~V_{GG} + 0.3	
Supply voltage (5)	$V_{GG} - V_{EE}$	−0.3 to 45.0	
Input voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V
Storage temperature	T_{stg}	−55 to 125	°C

Recommended Operating Conditions (V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	2.7 to 3.6	V
Supply voltage (2)	V_{GG}	10 to 37	
Supply voltage (3)	V_{EE}	−15 to −5	
Supply voltage (4)	$V_{OFF} - V_{EE}$	0 to 6	
Supply voltage (5)	$V_{GG} - V_{EE}$	17 to 42	
Operating temperature	T_{opr}	−20 to 75	°C
Operating frequency	f_{CPV}	DC to 100	kHz
Output Load capacitance	C_L	300 (max)	pF/PIN

Note 1: $V_{OFF} = V_{EE}$

Electrical Characteristics

DC Characteristics

($V_{GG} - V_{EE}$ = 30 to 42 V, V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, Ta = −20 to 75°C)

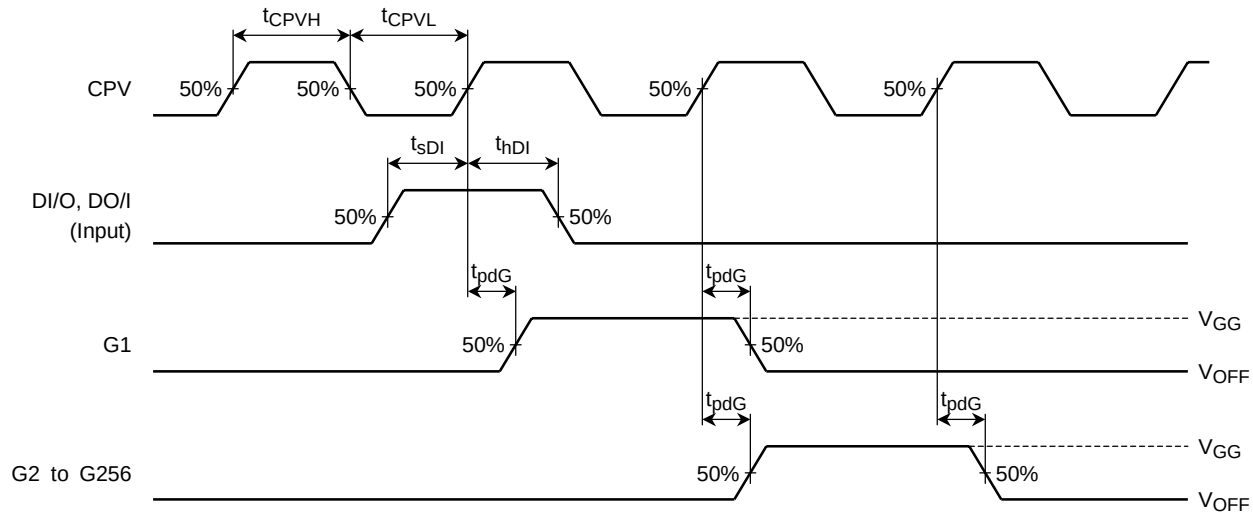
Parameter		Symbol	Test circuit	Test Condition	Min	Typ.	Unit	Relevant
Input voltage	Low Level	V_{IL}	—	—	V_{SS}	0.2 × V_{DD}	V	(Note 2)
	High Level	V_{IH}		—	0.8 × V_{DD}	V_{DD}		
Output voltage	Low Level	V_{OL}	—	I_{OL} = 40 μA	V_{SS}	V_{SS} + 0.4	V	DI/O, DO/I
	High Level	V_{OH}		I_{OH} = −40 μA	V_{DD} − 0.4	V_{DD}		
Output resistance	Low Level	R_{OL}	—	$V_{OUT} = V_{EE}$ + 0.5 V	—	1000	Ω	G1 to G256
	High Level	R_{OH}		$V_{OUT} = V_{GG}$ − 0.5 V				
Input leakage current		I_{IN}	—	—	−5	5	μA	(Note 2)
Current consumption (1)		I_{GG}	—	$\overline{OE}$ = "L", non-load	—	100	μA	
Current consumption (2)		I_{DD}		$\overline{OE}$ = "L"	—	700		

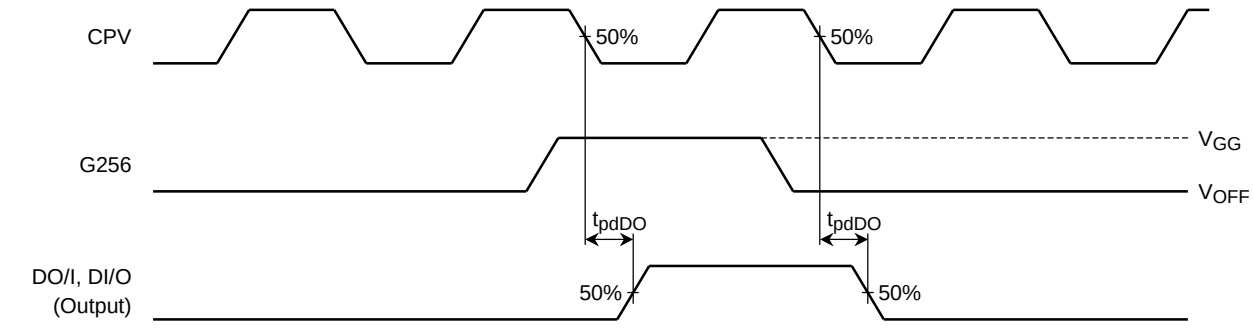
Note 2: These input pins include DI/O, DO/I, CPV, $\overline{OE}$1 to $\overline{OE}$3

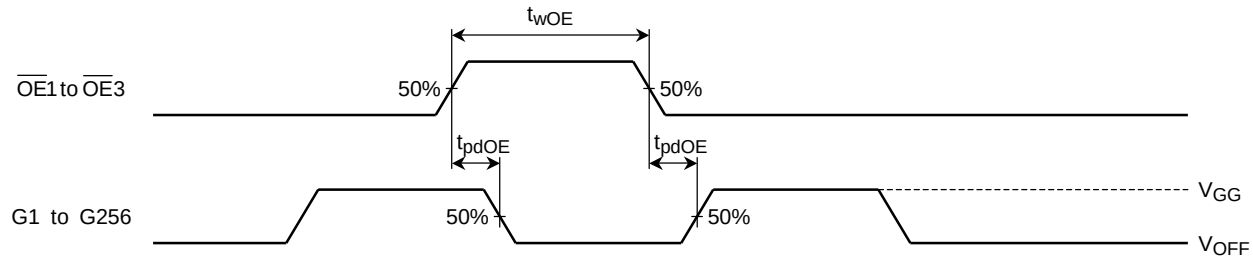
AC Characteristics

(V_{GG} − V_{EE} = 30 to 42 V, V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, Ta = −20 to 75°C)

Parameter	Symbol	Test circuit	Test Condition	Min	Typ.	Unit
Clock period	t_{CPV}	—	—	—	100	kHz
CPV pulse width (H)	t_{CPVH}	—	—	500	—	ns
CPV pulse width (L)	t_{CPVL}	—	—	500	—	ns
Data set-up time	t_{sDI}	—	—	200	—	ns
Data hold time	t_{hDI}	—	—	200	—	ns
$\overline{OE}$ enable time	t_{wOE}	—	—	1	—	μs
Output delay time (1)	t_{pdDO}	—	C_L = 50 pF	—	800	ns
Output delay time (2)	t_{pdG}	—	C_L = 300 pF	—	800	
Output delay time (3)	t_{pdOE}	—	C_L = 300 pF	—	800	

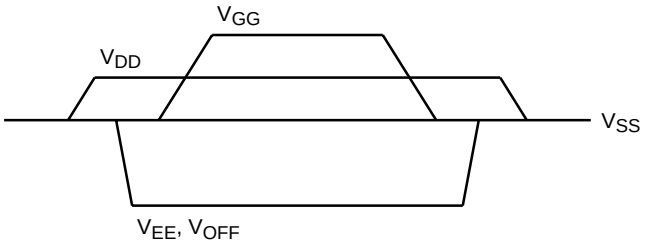






Power Supply Sequence

Turn power on in the order $V_{DD} \rightarrow V_{EE}$、$V_{OFF} \rightarrow$ Input signal $\rightarrow V_{GG}$ Turn power off in th reverse order.



RESTRICTIONS ON PRODUCT USE

000707EBE

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer’s own risk.
- Polyimide base film is hard and thin. Be careful not to injure yourself on the film or to scratch any other parts with the film. Try to design and manufacture products so that there is no chance of users touching the film after assembly, or if they do , that there is no chance of them injuring themselves. When cutting out the film, try to ensure that the film shavings do not cause accidents. After use, treat the leftover film and reel spacers as industrial waste.
- Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.
  This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.