TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T6K04

Column and Row Driver LSI for a Dot Matrix Graphic LCD

The T6K04 is a driver for a small-to-medium-sized dot matrix graphic LCD. It has an 8-bit interface circuit and can be operated with an 80-series MPU. It generates all the timing signals for the display with an on-chip oscillator. It receives 8-bit data from an MPU, latches the data to an on-chip RAM, and displays the image on LCD (the data in the display RAM correspond to the dots on the display). The device has 128 column driver outputs and 64 row driver outputs enabling it to drive an 128- dot by 64-dot LCD. In addition, there are resistors to divide bias voltage, a power supply op-amp, DC-DC converter (doubler, tripler, quadrupler) and contrast control circuit, enabling the LCD to be driven by a single power supply. The device can be connected to another T6K04 to drive a 256-dot by 64-dot LCD.

Unit: mm

T6K04	Lead Pitch	
	IN	OUT
(UAW, 5NS)	0.6	0.23

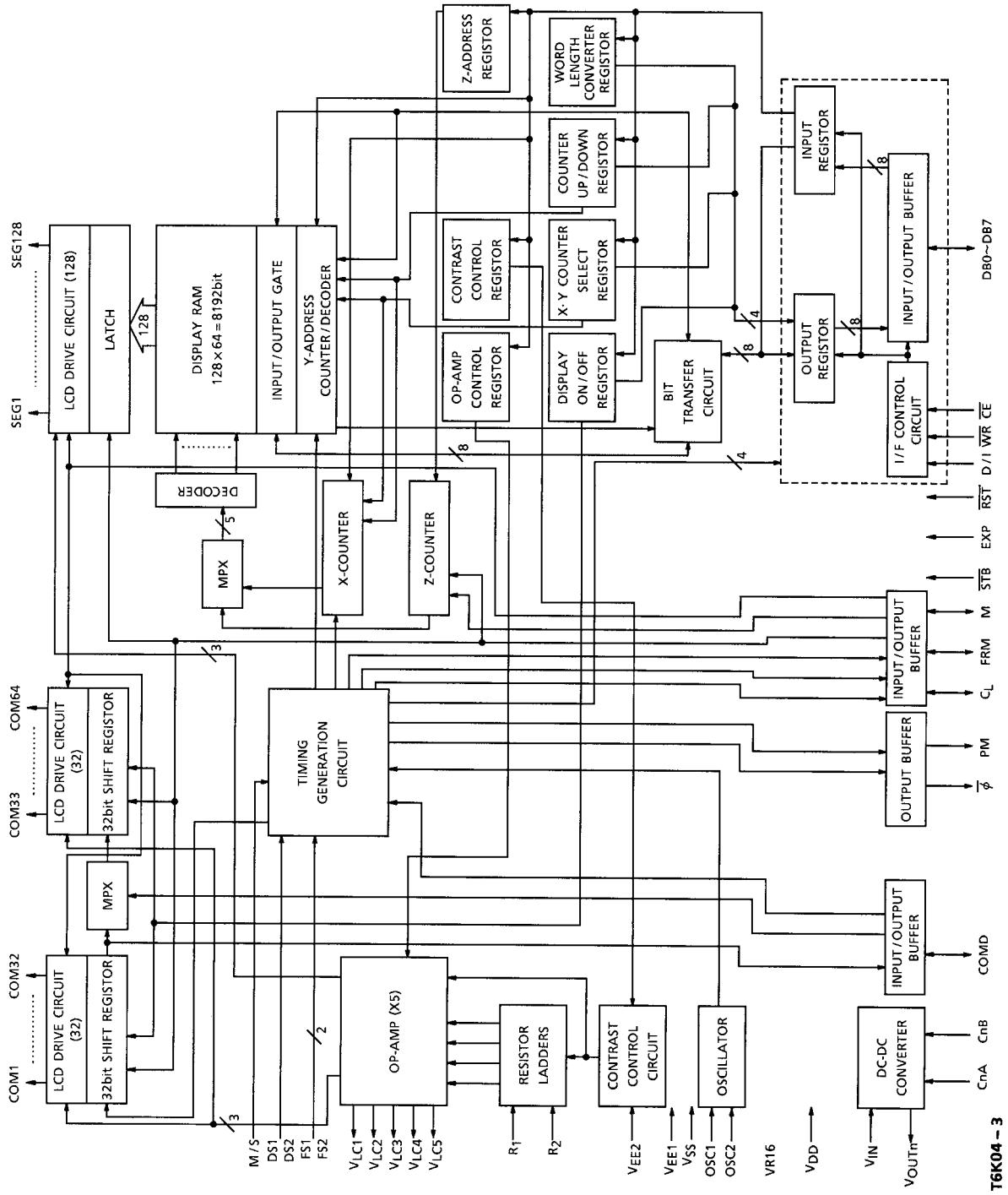
Please contact with Toshiba agents for each packaging outline dimensions.

TCP (Tape Carrier Package)

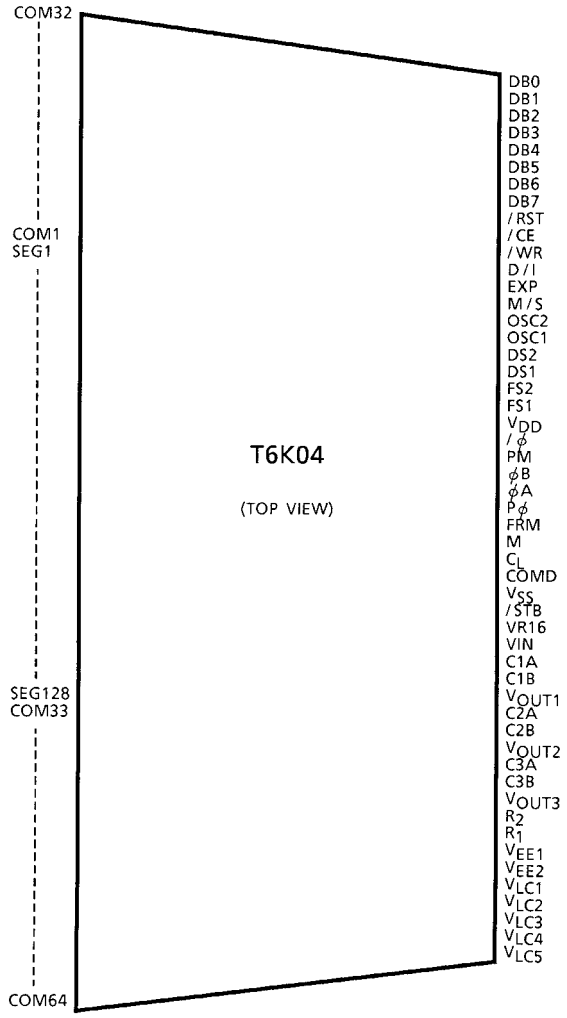
Features

- On-chip display RAM Capacity: 128 × 64 = 8192 bits
- Display RAM data
  (1) Display data = 1 …… LCD turns on.
  (2) Display data = 0 …… LCD turns off.
- 1/32, 1/48, 1/56 or 1/64 duty cycle
- Word length of display data can be switched between 8 bits and 6 bits according to the character font.
- LCD driver outputs: 128 column driver outputs and 64 row driver outputs
- Interface with 80 series MPU
- On-chip oscillator with one external resistor
- Low power consumption
- On-chip resistors to divide bias voltage, on-chip op-amp for LCD supply, on-chip DC-DC converter, on-chip contrast control circuit
- CMOS process
- Operating voltage: 2.7 to 5.5 V
- Operating voltage LCD drive signal: $V_{DD} - V_{EE1}$ = 16.5 V (max), $V_{DD} - V_{EE2}$ = 16.5 V(max), $V_{EE1} \leq V_{EE2}$
- Package: TCP (tape carrier package)

Block Diagram



Pin Assignment



Note: The above diagram shows the pin configuration of the LSI Chip, it doesn't show the configuration of the tape carrier package.

Pin Function

Pin Name	I/O	Function
SEG1 to SEG128	Output	Column driver output
COM1 to COM64	Output	Row driver output ● Disable expansion mode (EXP = L, M/S = H) → COM1 to COM64 are enabled ● Enable expansion mode/master mode (EXP = L, M/S = H) → COM1 to COM32 are enabled and COM33 to COM64 are disabled. ● Enable expansion mode/slave mode (EXP = H, M/S = L) → COM1 to COM32 are disabled and COM33 to COM64 are enabled.
C_L	I/O	Input/Output for shift clock pulse ● Master mode (M/S = H) → Output ● Slave mode (M/S = L) → Input
M	I/O	Input/Output for frame signal ● Master mode (M/S = H) → Output ● Slave mode (M/S = L) → Input
FRM	I/O	Input/Output for display synchronous signal ● Master mode (M/S = H) → Output ● Slave mode (M/S = L) → Input
Pφ, φA, φB	I/O	Input/Output system clock signal ● Master mode (M/S = H) → Output ● Slave mode (M/S = L) → Input
COMD	I/O	Input/Output row signal data ● Master mode (M/S = H) → Output ● Slave mode (M/S = L) → Input
DB0 to DB7	I/O	Data bus
D/I	Input	Input for Data/Instruction select signal ● D/I = H → Indicates that the data on DB0 to DB7 is the display data ● D/I = L → Indicates that the data on DB0 to DB7 is the control data
/WR	Input	Input for write select signal ● /WR = H → Read selected ● /WR = L → Write selected
/CE	Input	Input for chip enable signal ● /WR = L → Data of DB0 to DB7 is latched on the rising edge of /CE. ● /WR = H → Data appears at DB0 to DB7 while /CE is LOW.
/RST	Input	Input for reset signal ● /RST = L →Reset state
/STB	Input	Input for standby signal ● Usually connect to V_{DD} ● /STB = L → T6K04 is in stand-by state and cannot accept any commands or data. Column driver signal and row driver signal are at the V_{DD} level.
FS1, FS2	Input	Input for frequency selections

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>EXP</td><td>Input</td><td>Input for expansion mode selection
● M/S = H → Enables expansion mode. Two chips can be used together.
● M/S = L → Disables expansion mode.</td></tr>
<tr><td>M/S</td><td>Input</td><td>Input for Master/Slave selection
● M/S = H → T6K04 is master chip.
● M/S = L → T6K04 is slave chip.</td></tr>
<tr><td>OSC1, OSC2</td><td>—</td><td>When using the internal clock oscillator, connect a resistor between OSC1 and OSC2.
When using an external clock, connect the clock as input to OSC1 and leave OSC2 open.</td></tr>
<tr><td>R_1, R_2</td><td>—</td><td>Input for LCD drive bias selection
● LCD drive bias selection is shown in the following table.
<table>
<tr><th>R2</th><th>R1</th><th>Bias</th></tr>
<tr><td>0</td><td>0</td><td>1/6</td></tr>
<tr><td>0</td><td>1</td><td>1/7</td></tr>
<tr><td>1</td><td>0</td><td>1/8</td></tr>
<tr><td>1</td><td>1</td><td>1/9</td></tr>
</table></td></tr>
<tr><td>DS1, DS2</td><td>Input</td><td>Input for duty selection
● LCD drive duty selection is shown in the following table.
<table>
<tr><th>DS1</th><th>DS2</th><th>Duty</th></tr>
<tr><td>0</td><td>0</td><td>1/32 duty</td></tr>
<tr><td>0</td><td>1</td><td>1/48 duty</td></tr>
<tr><td>1</td><td>0</td><td>1/56 duty</td></tr>
<tr><td>1</td><td>1</td><td>1/64 duty</td></tr>
</table></td></tr>
<tr><td>V_{IN}</td><td>—</td><td>Power supply for DC-DC converter. Normally connect to V_{SS}.</td></tr>
<tr><td>C1A, C1B</td><td>—</td><td>External capacitor connecting pin for doubler</td></tr>
<tr><td>V_{OUT1}</td><td>—</td><td>DC-DC converter output (×2 level)</td></tr>
<tr><td>C2A, C2B</td><td>—</td><td>External capacitor connecting pin for tripler</td></tr>
<tr><td>V_{OUT2}</td><td>—</td><td>DC-DC converter output (×3 level)</td></tr>
<tr><td>C3A, C3B</td><td>—</td><td>External capacitor connecting pin for quadrupler</td></tr>
<tr><td>V_{OUT3}</td><td>—</td><td>DC-DC converter output (×4 level)</td></tr>
<tr><td>V_{EE1}, V_{EE2}</td><td>—</td><td>Power supply for LCD driver circuit
● When using on-chip DC-DC converter, connect $V_{EE}1$, 2 to V_{OUT}</td></tr>
<tr><td>V_{LC1} to V_{LC5}</td><td>—</td><td>Power supply for LCD driver circuit
● M/S = H → bias voltage output
● M/S = L → bias voltage input (Note 1)</td></tr>
<tr><td>VR16</td><td>Output</td><td>Don’t connect it.</td></tr>
<tr><td>V_{DD}</td><td>—</td><td>Power supply for logic circuit.</td></tr>
<tr><td>V_{SS}</td><td>—</td><td>Ground: Reference</td></tr>
<tr><td>PM</td><td>Output</td><td>Pre-frame signal</td></tr>
<tr><td>/φ</td><td>Output</td><td>Output system clock</td></tr>
</table>

(Note 1): Connect the capacitor between this pin and V_{DD}.

Function of Each Block

● Interface logic

The T6K04 can be operated with an 80-series MPU.
Fig. 1 shows an example of interface.

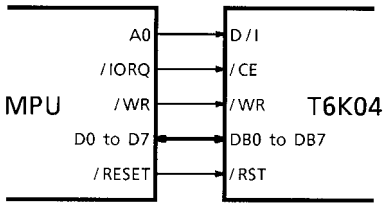


Fig. 1

● Input register

The register stores 8-bit data from the MPU. The D/I signal distinguishes between command data and display data.

● Output register

This register stores 8-bit data from the display RAM. When display data is read, the display data specified by the address in the address counter is stored in this register. After that, the address is automatically incremented or decremented. Therefore, when an address is set, the correct data does not appear at the first data item that is read. The data in the specified address location appears as the second data item that is read.

● X-address counter

X-address counter is a 64-up/down counter. It holds the row address of a location in the display RAM. Writing data to or reading data from the display RAM causes the X-address to be automatically incremented or decremented.

● Y- (Page) address counter

The Y- (Page) address counter is either a 16-up/down counter, when the word length is 8 bits, or a 22-up/down counter, when the word length is 6 bits. It holds the column address of a location in the display RAM. Writing data to or reading data from the display RAM causes the Y-address to be automatically incremented or decremented.

● Z-address counter

The Z-address counter is a 64-up counter that provides the display RAM data for the LCD drive circuit. The data stored in the Z-Address Register is send to Z-Address counter as Z start address.
For instance, when Z start address is 16, the counter increment as follows: 16, 17, 18···, 62, 63, 0, 1, 2···14, 15, 16. Therefore, the display start line is 16-line of the display RAM.

● Up/Down register

The 1-bit datum stored in this register selects either Up or Down mode for the X-and Y- (Page) address counters.

- **Counter select resister**

The 1-bit datum stored in this register selects the X-address counter or Y- (Page) address counter.

- **Display ON/OFF register**

This 1-bit register holds the display ON or OFF state. In the OFF state, the output data turn to V_{DD} level. In the On state, the display data corresponding to those in the display RAM are output to the LCD. The display ON or OFF state does not affect the data in the display RAM.

- **Z-address register**

This 6-bit register holds the data which specifies the display start line.

- **Word length register**

The 1-bit datum stored in this register selects the word length; 8 bits per word or 6 bits per word.

- **Word length change circuit**

This circuit is controlled by the word length register. When the word length is 8 bits, data is transferred 8 bits at a time. When the word length is 6 bits, the data transfer method is show in Fig. 2 as follows.

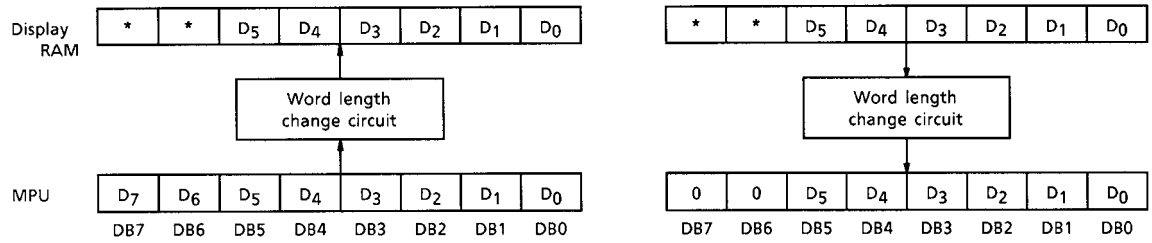


Fig. 2

- **Oscillator**

The T6K04 has an on-chip oscillator. When using this oscillator, connect an external resistor between OSC1 and OSC2. When using an external clock, connect the clock input to OSC1 and leave OSC2 open, as shown in Fig. 3.

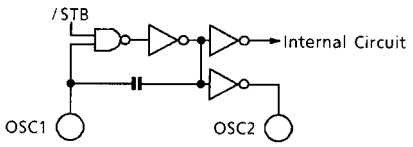


Fig. 3

- **Timing generation circuit**

The circuit divides the signals from the oscillator and generates display timing signals and operating clock.

- **Shift register**

The T6K04 has two 32-bit shift registers. In disable expansion mode, both the shift registers are enabled. These two 32-bit shift registers can be combined to form a 64-bit shift register. In enable expansion mode, the 32-bit shift register of master chip for COM1 to COM32 is enabled, and the 32-bit shift register of slave chip for COM33 to COM64 is enabled.

- **Latch circuit**

This latch circuit latches the data from the display RAM on the rising edge of the C_L signal.

- **Column driver circuit**

The column driver circuit consists of 128 driver circuits. One of the four LCD driving levels is selected by the combination of M signal and the display data transferred from the latch circuit. Details of the column driver circuit are shown in Fig. 4.

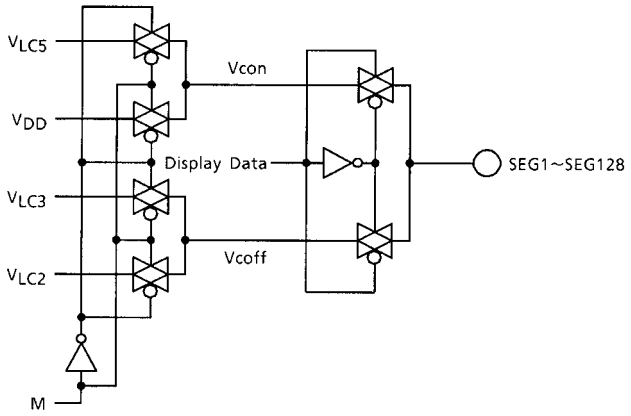


Fig. 4

- **Row driver circuit**

The row driver circuit consists of 64 drive circuits. One of the four LCD driving levels is selected by the combination of M signal and the data from the sift register. Details of the row driver circuit are shown in Fig. 5.

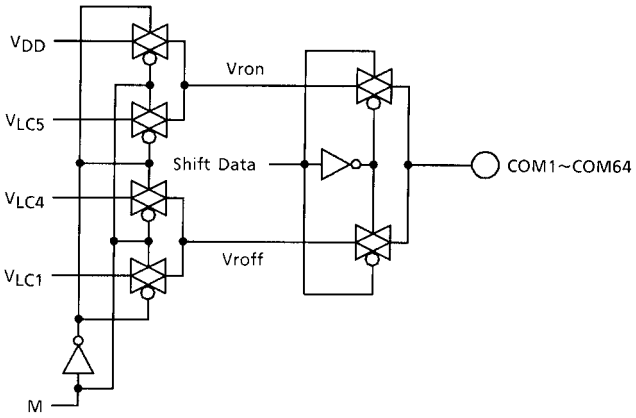


Fig. 5

- **DC-DC converter**

The T6K04 has an on-chip DC-DC converter. The DC-DC converter generates ×2 (V_{IN} × 2) level, ×3 (V_{IN} × 3) level and ×4 (V_{IN} × 4) level. See Fig. 6
When /STB = L, V_{OUT1}, V_{OUT2} and V_{OUT3} = 0 (V).
Normally the value of external capacitors are 2.2 μF; this value may need some adjustment according to the application.

Doubler (×2) mode

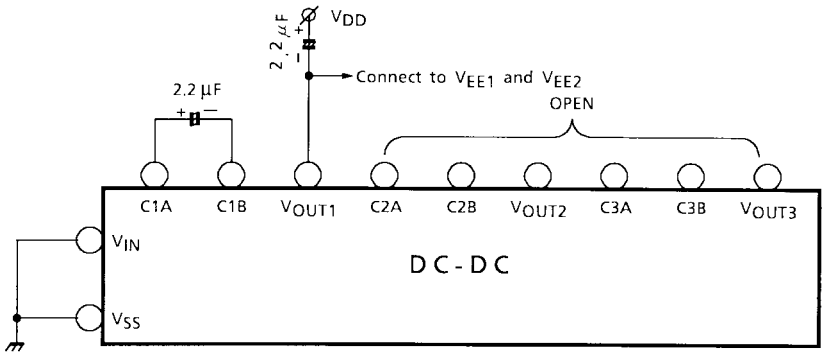


Fig. 6 (1)

Tripler (×3) mode

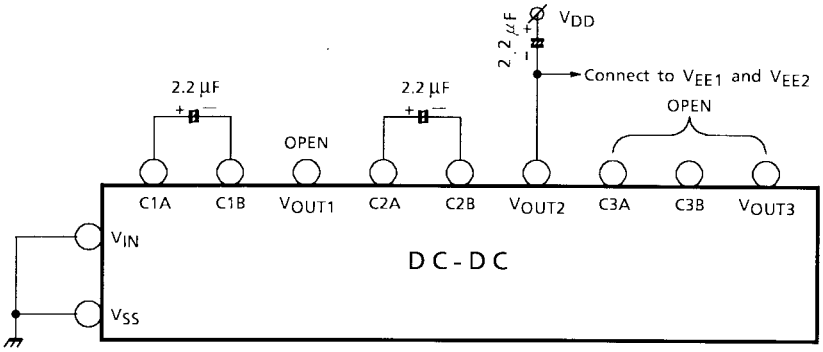


Fig. 6 (2)

Quadrupler (×4) mode

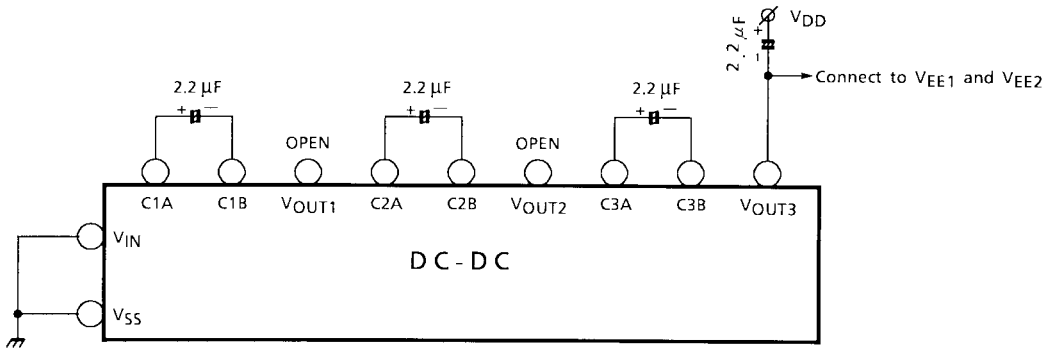


Fig. 6 (3)

When using an external power supply, input the voltage to V_{EE1} and V_{EE2} and do not connect the capacitors.

- **Voltage divider resistors, contrast control circuit**

The T6K04 has on-chip resistors which include op-amps, that divide the bias voltage, and a contrast control circuit.
The voltage bias is modified by the values of R_1 and R_2. One of four biases can be selected. These resisters and contrast control circuit are shown in Fig. 7 as follows.

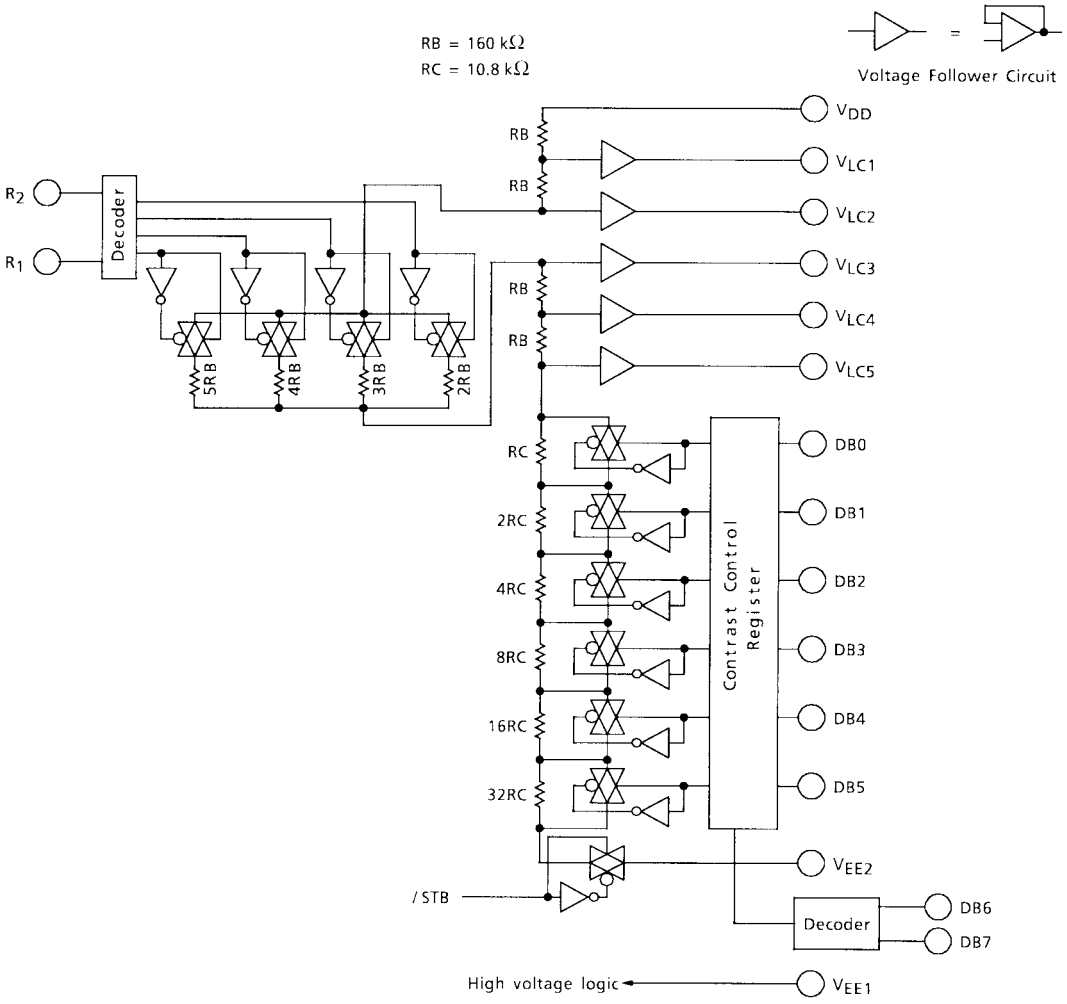


Fig. 7

- **Op-amp, Op-amp control register**

The T6K04 has 5 operational amplifiers that determine the LCD driving level. The power supplied by these op-amps is modified by the contents of op-amp control register to match the LCD panel. The op-amp can be also controlled in such a way that it supplies full current on the rising edge of C_L and a reduced current otherwise. To maintain good LCD contrast, connect a capacitor between the op-amp output and V_{DD}. The valve of the capacitor should normally be in the range 0.1 to 1.0 μF.

- **Display RAM**

The display RAM consists of 64 rows × 128 columns for a total 8192 cells. It is directly bit mapped to the LCD. The relation between the display RAM and LCD are shown in Fig. 8.
When the word length is set to 8 bits, the display RAM is arranged in 16 pages and each page contains 48 words. When the word length is set to 6 bits, the display RAM is arranged as 22 pages and each page contains 34 words. See Fig. 9.

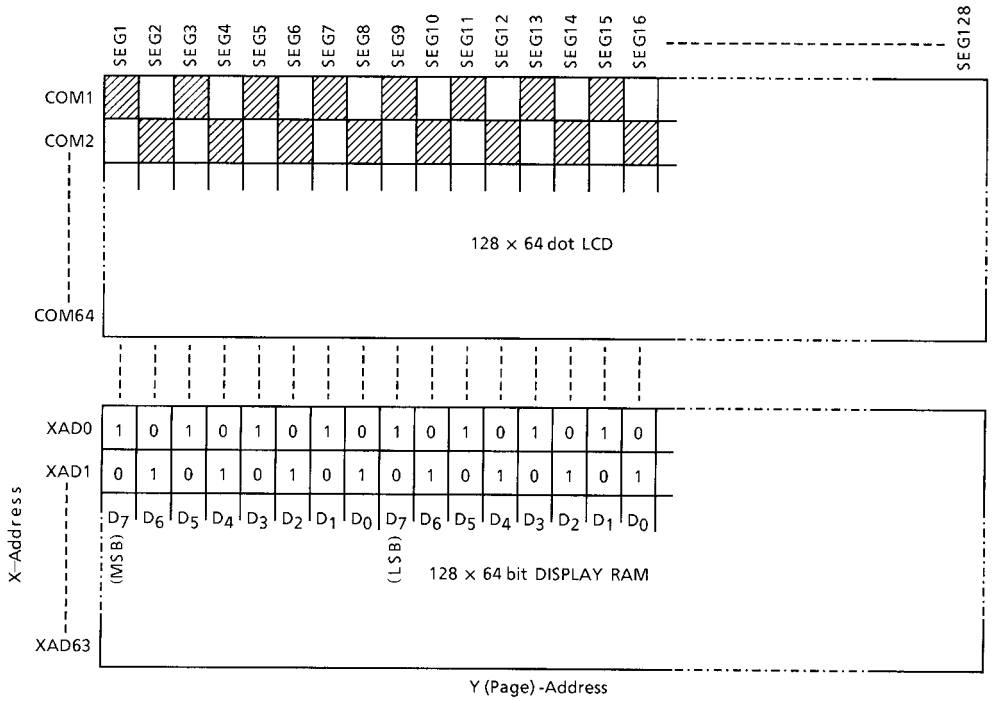
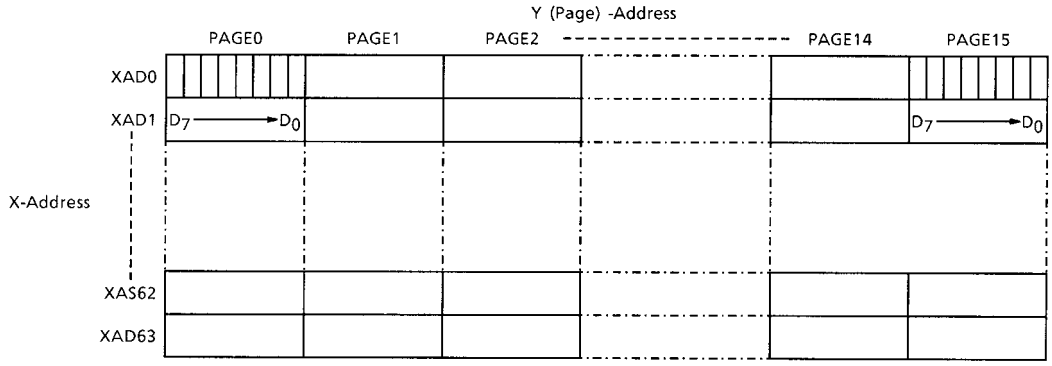


Fig. 8

8 bits per word mode



6 bits per word mode

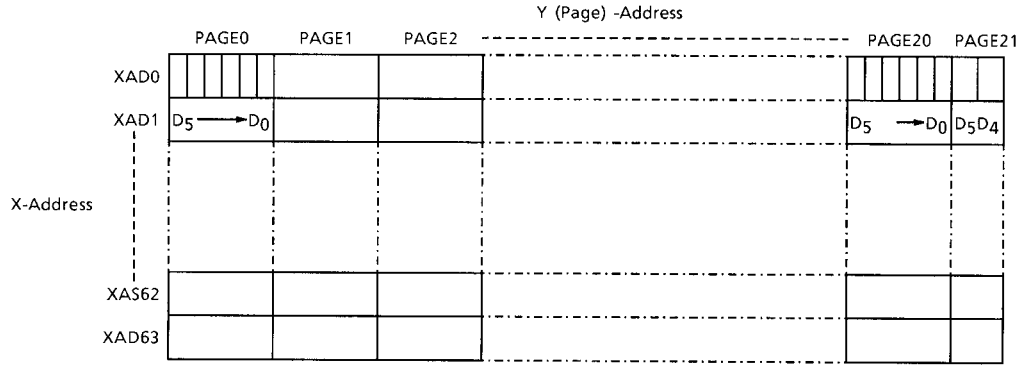


Fig. 9

Command Definitions

Command Name	D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
86E	0	0	0	0	0	0	0	0	0	1/0	Word Length: 8 bits (1)/6 bits (0)
DPE	0	0	0	0	0	0	0	0	1	1/0	Display ON (1)/OFF (0)
UDE	0	0	0	0	0	0	0	1	1/0	1/0	Counter Select: DB1 Y (1)/X (0) Mode Select : DB0 UP (1)/DOWN (0)
CHE	0	0	0	0	0	1	1	*	*	*	Test Mode Select
OPA1	0	0	0	0	0	1	0	1/0	1/0	1/0	Op-amp Control 1
OPA2	0	0	0	0	0	0	1	0	1/0	1/0	Op-amp Control 2
SYE	0	0	0	0	1	Y-Address (0 to 21)					Y-(Page) address Set
SZE	0	0	0	1	Z-Address (0 to 63)						Z-Address Set
SXE	0	0	1	0	X-Address (0 to 63)						X-Address Set
SCE	0	0	1	1	CONTRAST CONTROL (0 to 63)						Contrast Set
STRD	0	1	B	8/6	D	R	OP	0	Y/X	U/D	Status Read
DAWR	1	0	Write Data								Display Data Write
DARD	1	1	Read Data								Display Data Read

*: INVALID

- **Display ON/OFF select (DPE)**

D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	0	1	1	Display ON (03H)
0	0	0	0	0	0	0	0	1	0	Display OFF (02H)

This command turns display ON/OFF. It does not affect the data in the display RAM.
When input the display OFF command, V_{LC1} to V_{LC5} is all V_{DD} level.

Note: An L input on /RST turns display OFF.

- **Word length 8 bits/6 bits select (86E)**

D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	0	0	1	Word Length 8 bits/Word mode (01H)
0	0	0	0	0	0	0	0	0	0	Word Length 6 bits/Word mode (00H)

This command sets the word length for the display RAM data to either 6 bits or 8 bits.

Note: An L input on /RST sets the word length to 8 bits per word.

- **X/Y (Page) counter, Up/Down mode select (UDE)**

D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	1	0	0	X-Counter/Down mode (04H)
0	0	0	0	0	0	0	1	0	1	X-Counter/Up mode (05H)
0	0	0	0	0	0	0	1	1	0	Y-Counter/Down mode (06H)
0	0	0	0	0	0	0	1	1	1	Y-Counter/Up mode (07H)

This command selects the counter and up/down mode. For instance, when X-counter /up mode is selected, the X-address is incremented in response to every data read and write. However, when X-Counter /up mode is selected, the address in the Y- (Page) counter will not change. Hence, the Y-address must be set (with the SYE command) before it can be changed.

Note: An L input on /RST sets the Y-counter to up mode.

- **Test mode select (CHE)**

D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	*	*	*

This command selects the test mode. Don't use this command.

- **Set Y- (Page) address (SYE)**

D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	A	A	A	A	A

Range: 8-bit/word: 20H to 2FH (Page 0 to Page 15)
6-bit/word: 20H to 35H (Page 0 to Page 21)
When operating in 8 bits per word mode, this command selects one of the 16 pages from the display RAM. (Don't try to select a page outside this range) When operating in 6 bits per word mode, this command selects one of the 22 pages from the display RAM.

Note: An L input on /RST sets the Y-address to page 0.

- **Set Z-address (SZE)**

D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	A	A	A	A	A	A

Range: 40H to 7FH (ZAD0 to ZAD63)
This command sets the top row of LCD screen, irrespective of the current X-address.
For instance, when the Z-address is 16, the top row of LCD screen is address 16 of the display RAM, and the bottom row of the LCD screen is address 15 of the display RAM.

Note: An L input on /RST sets the Y-address to page 0.

- **Set X-address (SXE)**

D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	A	A	A	A	A	A

Range: 80H to BFH (XAD0 to XAD63)

This command sets the X-address (in the range 0 to 63).

Note: An L input on /RST sets the X-address to page 0.

- **Set contrast (SCE)**

D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	A	A	A	A	A	A

Range: C0H to FFH

This command sets the contrast for the LCD. The LCD contrast can be set in 64 steps. The command C0H selects the brightest level; the command FFH selects the darkest level.

- **Op-amp control 1 (OPA1)**

D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	A	A	A

Range: 14H to 17H

This command sets the power supply strength of the operational amplifier. This command selects one of four levels. The command 14H selects the lowest power supply strength and the command 17H selects the maximum strength. This command can turn off op-amp by inputting 0 to DB2.

Note: An L input on /RST sets the op-amp power supply strength to the lowest level.

- **Op-amp control 2 (OPA2)**

D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	0	A	A

Range: 08H to 0BH

This command enhances the power supply strength of the operational amplifier over a shot period from the rising edge of CL. This command selects one of four levels of strength.

Note: An L input on /RST sets to 0 for op-amp. See Fig. 10.

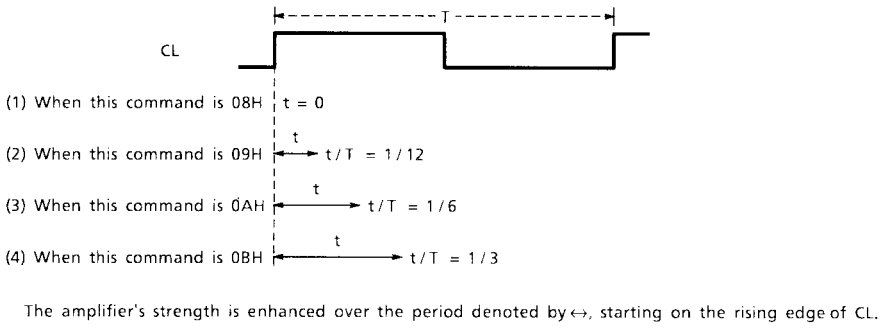


Fig. 10

- **Status read (STRD)**

D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	B	8/6	D	R	OP	0	Y/X	U/D

B (Busy) : When B = 1, the T6K04 is executing an internal operation and no instruction can be accepted except STRD.
When B = 0, the T6K04 can accept an instruction.

8/6 (Word Length) : When 8/6 = 1, the word length of the display data is 8 bits per word.
When 8/6 = 0, the word length of the display data is 6 bits per word.

D (Display) : When D = 1, display is ON.
When D = 0, display is OFF.

R (Reset) : When R = 1, the T6K04 is in reset state.
When R = 0, the T6K04 is operating state.

OP (Op-amp) : When OP = 1, op-amp is ON.
When OP = 0, op-amp is OFF.

Y/X (Counter) : When Y/X = 1, the Y counter is selected.
When Y/X = 0, the X counter is selected.

U/D (UP/DOWN) : When U/D = 1, the X and Y counters are in up mode.
When U/D = 0, the X and Y counters are in down mode.

- **Write/read display data (DAWR/DARD)**

D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	D	D	D	D	D	D	D	D	DAWR: Display Data Write
1	1	D	D	D	D	D	D	D	D	DARD: Display Data Read

The command DAWR writes the display data to the display RAM. The command DARD outputs the display data from the display RAM. However, when a data read is executed, the correct data does not appear on the first data reading. Therefore, ensure that the T6K04 performs a dummy data read before reading the actual data.

Detail of Performance

- **X-address counter and Y- (page) address counter**

Fig. 11 shows a sample operation involving the X-address counter.
After Reset is executed, X-address (XAD) becomes 0, then X-counter/up mode is selected. Next, the X-address is set to 62 using the SXE command.
After data has been written or read, the X-address is automatically incremented by one.
After X-counter/Down mode has been selected and data has been written to or read, the X-address is automatically decremented by one.
When the X-counter is selected, Y-counter is not incremented or decremented.

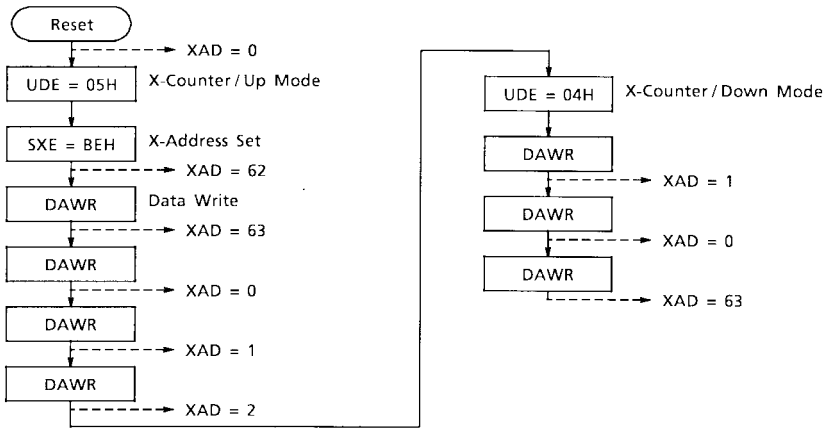


Fig. 11

Fig. 12 shows a sample operation involving the Y-address counter in 8-bit word length mode.
After Reset is executed, Y- (page) address becomes 0, then select Y- (page) counter/up mode and 8-bit word length mode are selected. After data has been written or read, the Y- (page) address counter is automatically incremented by one.
After Y- (page) counter/down mode has been selected and data has been written or read, the Y- (page) address is automatically decremented by one.
When the Y- (page) counter is selected, X-counter is not incremented or decremented.

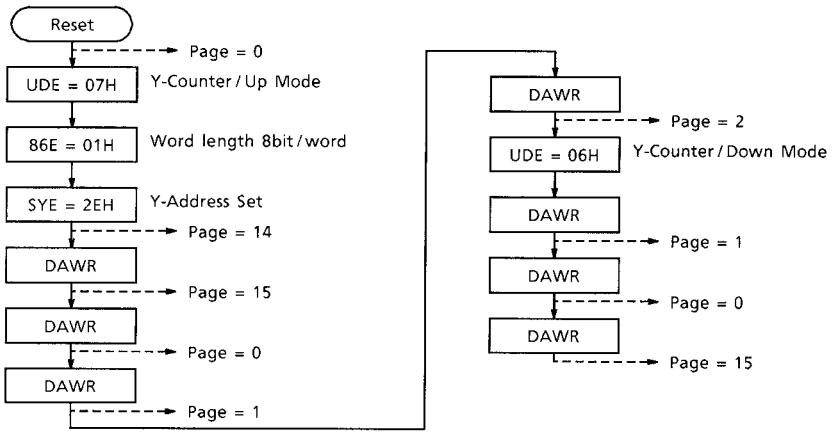


Fig. 12

When operating in 6-bit word length mode, the Y- (page) address counter can count up to 22.
If page = 21 in up mode, after data has been written or read, Y- (page) address becomes 0.
If page = 0 in down mode, after data has been written or read, Y- (page) address becomes 21.

- **Data read**

When reading data, there are some cases when dummy data must be read. This is because when the data read command is invoked, the data pointed to by the address counter is transferred to the output resister; the contents of the output resister are then transferred by the next data read command.
Therefore when reading data straight after power-on or straight after address-setting command, such as SYE or SXE, a dummy data read must be performed. See Fig. 13.

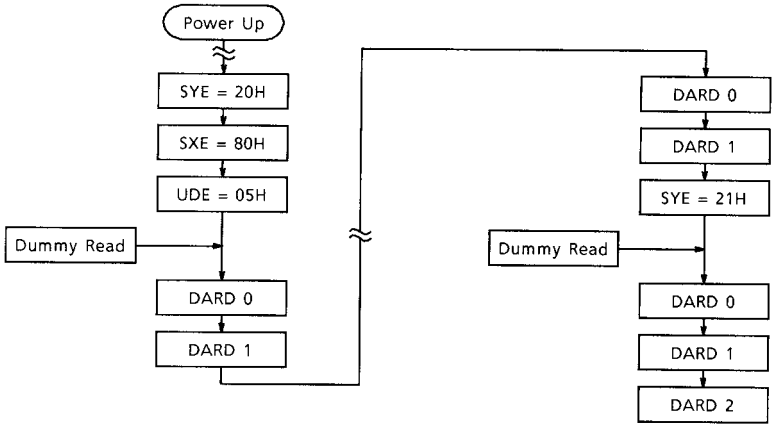


Fig. 13

● Reset function

When /RST = L, the reset function is executed and the following setting are mode.

- Display ..... OFF
- Word length ..... 8 bits/word
- Counter mode ..... Y counter/up mode
- Y- (page) address ..... Page = 0
- X-address ..... XAD = 0
- Z-address ..... ZAD = 0
- Op-amp ..... ON
- OPA1 ..... Min.
- OPA2 ..... Min.
- CONTRAST ..... Min. ($V_{LC5} = V_{EE1, 2}$)

● Stand-by function

When /STB = L, the T6K04 is in stand-by state. The internal oscillator is stopped, power consumption is reduced, and the power supply level for the LCD (V_{LC1} to V_{LC5}) becomes V_{DD}.

● Busy flag

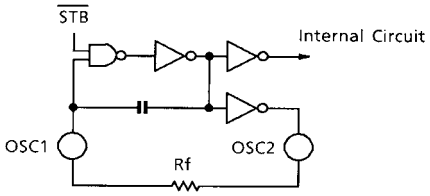
When the T6K04 is executing an internal operation (other than the STRD command), the busy flag is set at logical H. The state of the busy flag is output in response to the STRD command. While the busy flag is H, no instruction can be accepted (except the STRD command). The busy state period (T) is shown as follows.

$2/f_{OSC} \leq T \leq 4/f_{OSC}$ [sec] f_{OSC}: Frequency of OSC1

● Oscillation frequency

The frequency select pins (FS1 and FS2), are used to set the relation between oscillation frequency (f_{OSC}) and frame frequency (f_M).

Next table shows the choice of the frequency select pins (FS1 and FS2) and oscillation frequency to set f_{COM} = 35 (Hz). The resistance values are typical values. The oscillation frequency depends on the mounting condition. So it is necessary to adjust the oscillation frequency to a target value.



Rf (kΩ)	f_{OSC} (kHz)	f_{COM} (Hz)	FS1	FS2
1100	28.56	35	0	0
530	57.12	35	1	0
140	228.48	35	0	1
70	456.96	35	1	1

● Expansion function

The T6K04's expansion function, allows two, the T6K04s to drive an LCD panel of up to 256 by 64 dots. The table below shows the functions that can be selected with the M/S, EXP pins.

		M/S	
		H	L
EXP	H	● Two-chip mode (Enable expansion mode) ● Master chip COM1 to COM32 are available.	● Two-chip mode (Enable expansion mode) ● Slave chip ● COM33 to COM64 are available. ● Timing signals and power voltage are supplied from master chip.
	L	● Single-chip mode (Disable expansion mode) ● COM1 to COM64 are available.	● Do not select

Fig. 13-1 and -2 illustrate the application examples of disable expansion mode and enable expansion mode.
In Enable Expansion Mode (Two-chip mode)
As shown in Fig. 13-2, Fig.14 the master chip supplies the LCD drive signals and power voltage to the slave chip (the oscillator, the timing circuits, op-amp and contrast control circuit are disabled).
COM1 to COM32 of the master chip and COM33 to COM64 of the slave chip are available (COM33 to COM64 of the master chip and COM1 to COM32 of the slave chip are disabled).

(1) Disable expansion mode

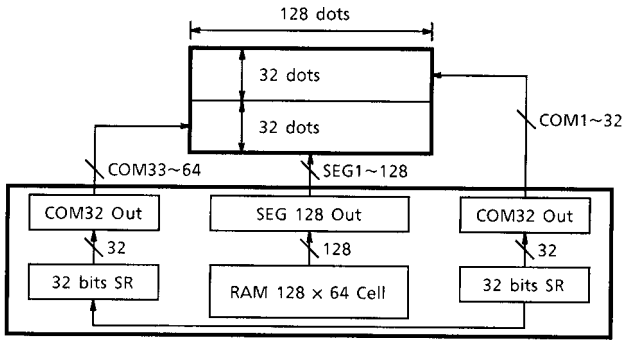


Fig. 13-1

(2) Expansion mode

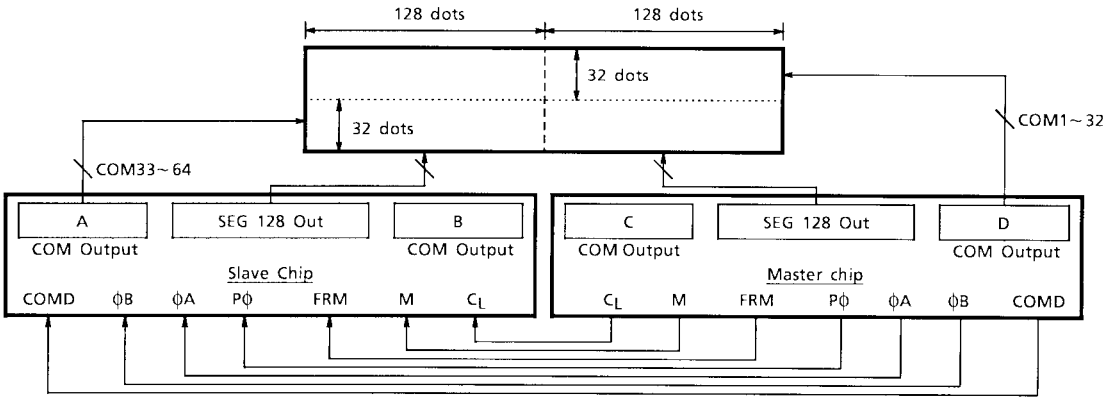


Fig. 13-2

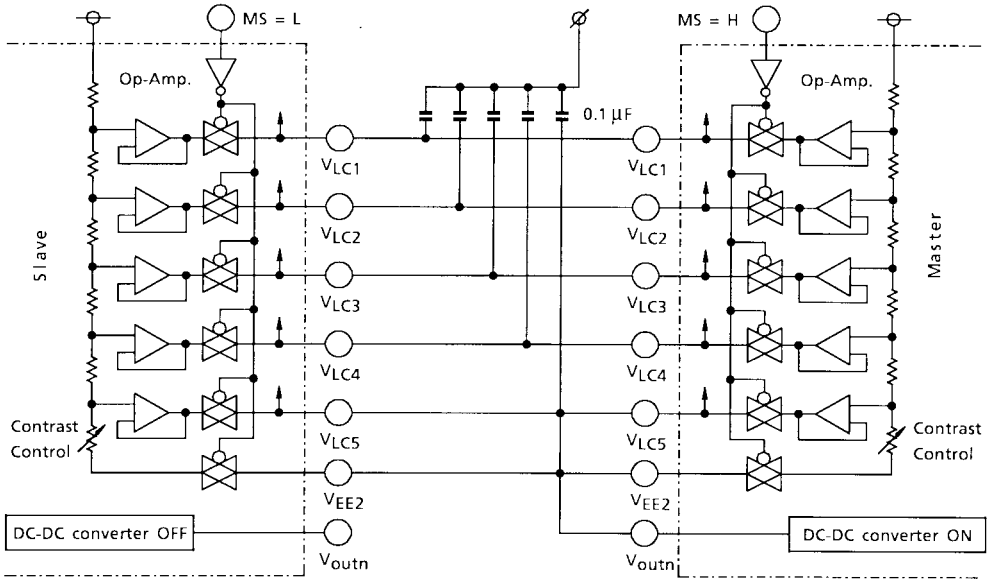
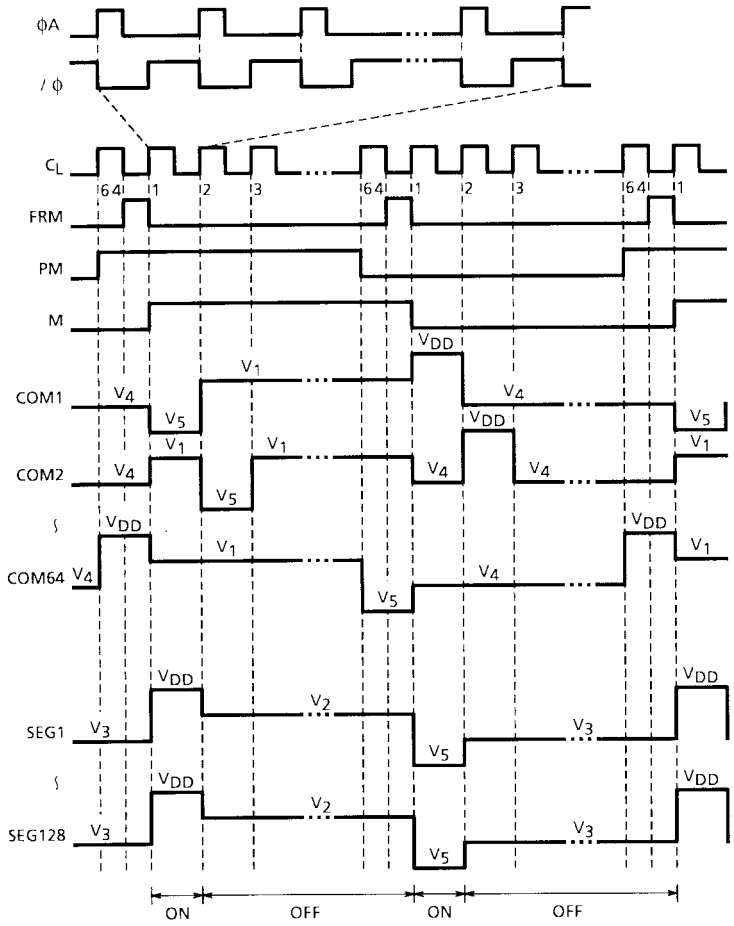


Fig. 14

- **LCD Driver Waveform**



LCD driver timing chart (1/64 duty)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage (1)	V_{DD} (Note 1)	−0.3 to 7.0	V
Supply Voltage (2)	$V_{LC1, 2, 3, 4, 5}$ V_{EE1}, V_{EE2}	V_{DD} − 18.0 to V_{DD} + 0.3	V
Input Voltage	V_{INP} (Note 1, 2)	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	−20 to 75	°C
Storage Temperature	T_{stg}	−55 to 125	°C

Note 1: Referred to V_{SS} = 0 V

Note 2: Applied data bus terminals and Input terminals expect V_{EE1}, V_{EE2}, V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4} and V_{LC5}.

Electrical Characteristics
DC Characteristics (1)
(Test conditions: Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, V_{LC5} = 0 V, Ta = 25°C)

Item		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Operating Supply (1)		V_{DD}	—	—	2.7	—	3.3	V	V_{DD}, V_{IN}
Operating Supply (2)		V_{LC5} $V_{EE1, 2}$	—	—	V_{DD} − 16.5	—	V_{DD} − 4.0	V	V_{LC5}, V_{EE1}, V_{EE2}
Input Level	H Level	V_{IH}	—	—	0.8 V_{DD}	—	V_{DD}	V	DB0 to 7, D/I, /WR,/CE, /RST,/STB, M/S, EXP, CL, M, FRM, φA, φB, COMD, FS1, FS2, DS1, DS2, Pφ
	L Level	V_{IL}	—	—	0	—	0.2 V_{DD}	V	
Output Level	H Level	V_{OH}	—	I_{OH} = −400 μA	V_{DD} − 0.2	—	V_{DD}	V	DB0 to DB7
	L Level	V_{OL}	—	I_{OL} = 400 μA	0	—	0.2	V	
Column Driver On Resistance		Rcol	—	V_{DD} − V_{LC5} = 11.0 V Load current = ± 100 μA	—	—	7.5	kΩ	SEG1 to SEG128
Row Driver On Resistance		Rrow	—	V_{DD} − V_{LC5} = 11.0 V Load current = ± 100 μA	—	—	1.5	kΩ	COM1 to COM64
Input Leakage		I_{IL}	—	V_{IN} = V_{DD} to GND	−1	—	1	μA	DB0 to 7, D/I, /WR,/CE, /RST,/STB, M/S, EXP, CL, M, FRM, φA, φB, COMD, FS1, FS2, DS1, DS2, Pφ
Operating Freq		f_{OSC}	—	—	20	—	500	kHz	OSC1
External Clock Freq		f_{ex}	—	—	20	—	500	kHz	OSC1
External Clock Duty		f_{duty}	—	—	45	50	55	%	OSC1
External Clock Rise/Fall Time		t_r/t_f	—	—	—	—	50	ns	OSC1
Current Consumption (1)		I_{DD1}	—	(Note 1)	—	300	420	μA	V_{DD}
Current Consumption (2)		I_{DD2}	—	(Note 2)	—	400	530	μA	V_{DD}
Current Consumption (3)		I_{DDSTB}	—	(Note 3)	−1	—	1	μA	VDD
Output Voltage (Tripler Mode)		VO2	(2)	(Note 4)	−4.50	−4.90	—	V	V_{OUT2}
Output Voltage (Quadruplexer Mode)		VO3	(3)	(Note 5)	−6.75	−7.50	—	V	V_{OUT3}

Note 1: V_{DD} = 3.0 ± 10%, $V_{EE1, 2}$ = V_{OUT2} (Tripler mode), Master mode, No data access, R_f = 62 kΩ, LCD out pin No Load, 1/9 bias, FS1, 2 = H, OPA1 = 14H, OPA2 = 08 H

Note 2: V_{DD} = 3.0 ± 10%, $V_{EE1, 2}$ = V_{OUT2} (Tripler mode), Master mode, Data access cycle f/CE= 1 MHz, R_f = 62 kΩ, LCD out pin No Load, 1/9 bias, FS1, 2 = H, OPA1 = 14H, OPA2 = 08 H

Note 3: V_{DD} = 3.0 ± 10%, V_{DD} − $V_{EE1, 2}$ = 16.0 V,/STB = L

Note 4: V_{DD} = 3.0 V, I_{Load} = 500 μA, $V_{EE1, 2}$ = −6.0 V (external power supply) CnA − CnB = 2.2 μF, V_{DD} − V_{OUT2} = 2.2 μF, R_f = 62 kΩ, Ta = 25°C

Note 5: V_{DD} = 3.0 V, I_{Load} = 500 μA, $V_{EE1, 2}$ = −9.0 V (external power supply) CnA − CnB = 2.2 μF, V_{DD} − V_{OUT3} = 2.2 μF, R_f = 62 kΩ, Ta = 25°C

DC Characteristics (2)

(Test conditions: Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, V_{LC5} = 0 V, Ta = 25°C)

Item		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Operating Supply (1)		V_{DD}	—	—	4.7	—	5.5	V	V_{DD}
Operating Supply (2)		V_{LC5} $V_{EE1, 2}$	—	—	V_{DD} − 16.5	—	V_{DD} − 4.0	V	V_{LC5}, V_{EE1}, V_{EE2}
Input Level	H Level	V_{IH}	—	—	0.7 V_{DD}	—	V_{DD}	V	DB0 to 7, D/I, /WR,/CE, /RST,/STB, M/S, EXP, CL, M, FRM, φA, φB, COMD, FS1, FS2, DS1, DS2, Pφ
	L Level	V_{IL}	—	—	0	—	0.3 V_{DD}	V	
Output Level	H Level	V_{OH}	—	I_{OH} = −400 μA	V_{DD} − 0.2	—	V_{DD}	V	DB0 to DB7
	L Level	V_{OL}	—	I_{OL} = 400 μA	0	—	0.2	V	
Column Driver On Resistance		Rcol	—	V_{DD} − V_{LC5} = 11.0 V Load current = ± 100 μA	—	—	7.5	kΩ	SEG1 to SEG128
Row Driver On Resistance		Rrow	—	V_{DD} − V_{LC5} = 11.0 V Load current = ± 100 μA	—	—	1.5	kΩ	COM1 to COM64
Input Leakage		I_{IL}	—	V_{IN} = V_{DD} to GND	−1	—	1	μA	DB0 to 7, D/I, /WR,/CE, /RST,/STB, M/S, EXP, CL, M, FRM, φA, φB, COMD, FS1, FS2, DS1, DS2, Pφ
Operating Freq		f_{OSC}	—	—	20	—	500	kHz	OSC1
External Clock Freq		f_{ex}	—	—	20	—	500	kHz	OSC1
External Clock Duty		f_{duty}	—	—	45	50	55	%	OSC1
External Clock Rise/Fall Time		t_r/t_f	—	—	—	—	50	ns	OSC1
Current Consumption (1)		I_{DD1}	—	(Note 1)	—	510	640	μA	V_{DD}
Current Consumption (2)		I_{DD2}	—	(Note 2)	—	620	830	μA	V_{DD}
Current Consumption (3)		I_{DDSTB}	—	(Note 3)	−1	—	1	μA	VDD
Output Voltage (Tripler Mode)		VO1	(1)	(Note 4)	−4.25	−4.50	—	V	V_{OUT1}
Output Voltage (Quadruplexer Mode)		VO2	(2)	(Note 5)	−8.50	−9.00	—	V	V_{OUT2}

Note 1: V_{DD} = 5.0 ± 10%, $V_{EE1, 2}$ = V_{OUT1} (Doubler mode), Master mode, No data access, R_f = 62 kΩ, LCD out pin No Load, 1/9 bias, FS1, 2 = H, OPA1 = 14H, OPA2 = 08 H

Note 2: V_{DD} = 5.0 ±10%, $V_{EE1, 2}$ = V_{OUT1} (Doubler mode), Master mode, Data access cycle f/CE = 1 MHz, R_f = 62 kΩ, LCD out pin No Load, 1/9 bias, FS1, 2 = H, OPA1 = 14H, OPA2 = 08 H

Note 3: V_{DD} = 5.0 ± 10%, V_{DD} − $V_{EE1, 2}$ = 16.0 V,/STB = L

Note 4: V_{DD} = 5.0 V, I_{Load} = 500 μA, $V_{EE1, 2}$ = −5.0V (external power supply) CnA − CnB = 2.2 μF, V_{DD} − V_{OUT1} = 2.2 μF, R_f = 62 kΩ, Ta = 25°C

Note 5: V_{DD} = 5.0 V, I_{Load} = 500 μA, $V_{EE1, 2}$ = −10.0 V (external power supply) CnA − CnB = 2.2 μF, V_{DD} − V_{OUT2} = 2.2 μF, R_f = 62 kΩ, Ta = 25°C

DC Characteristics (3)

(Test conditions: Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.7 to 3.3 V)

Item	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Op-Amp Output Voltage Offset (1)	V_{opoff}	—	(Note 1)	−150	—	150	mV	V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4}, V_{LC5}
Op-Amp Output Voltage Offset (2)	V_{opoffs}	—	(Note 2)	−100	—	100	mV	V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4}, V_{LC5}

Note 1: V_{DD} = 3.0 V, V_{SS} = 0 V, 1/9 bias, 1/64 duty, $V_{EE1, 2}$ = −9.5 V, Contrast control = Max, Op-amp ON, DC-DC OFF, LCD out pin No Load

V_{LC1} pin: $V_{DD} - |V_{DD} - V_{EE}| \times 1/9 = V_{opoff}$

V_{LC2} pin: $V_{DD} - |V_{DD} - V_{EE}| \times 2/9 = V_{opoff}$

V_{LC3} pin: $V_{DD} - |V_{DD} - V_{EE}| \times 7/9 = V_{opoff}$

V_{LC4} pin: $V_{DD} - |V_{DD} - V_{EE}| \times 8/9 = V_{opoff}$

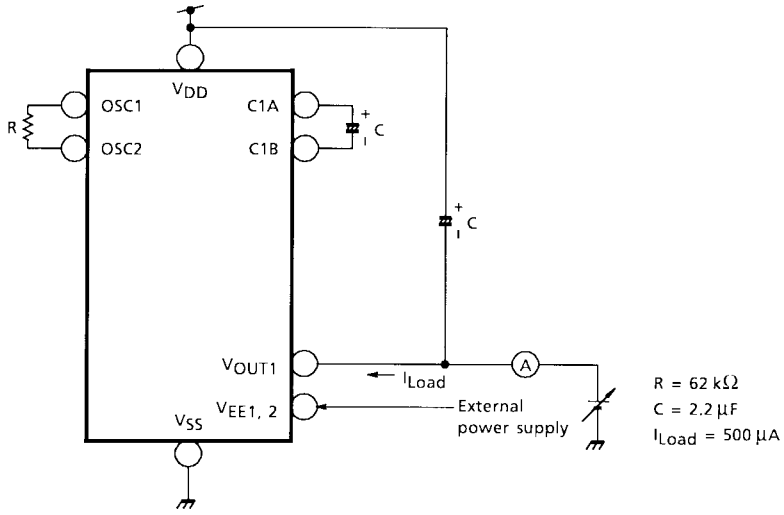
V_{LC5} pin: $V_{DD} - |V_{DD} - V_{EE}| = V_{opoff}$

Note 2: V_{DD} = 3.0 V, V_{SS} = 0 V, 1/9 bias, 1/64 duty, $V_{EE1, 2}$ = −9.5 V, Contrast control = Max, Op-amp ON, DC-DC OFF, LCD out pin No Load

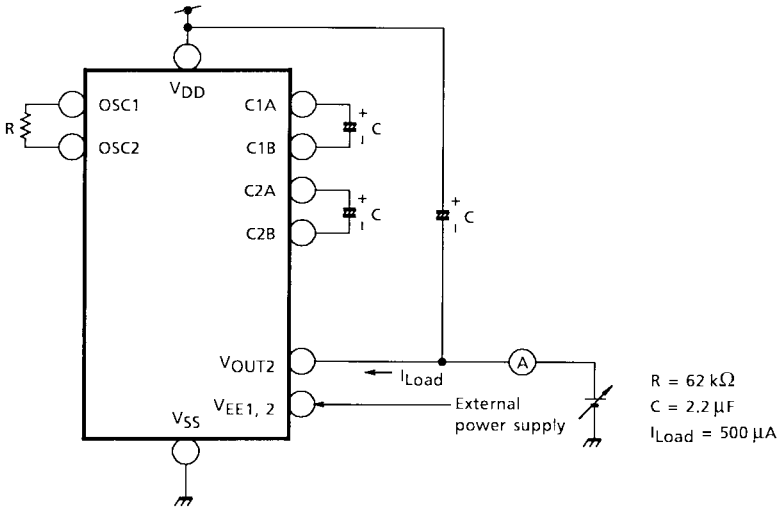
$V_{opoffs} = ((V_{LC1} - V_{LC2}) - (V_{DD} - V_{LC1})) + ((V_{LC3} - V_{LC4}) - (V_{LC4} - V_{LC5}))$

Test Circuit

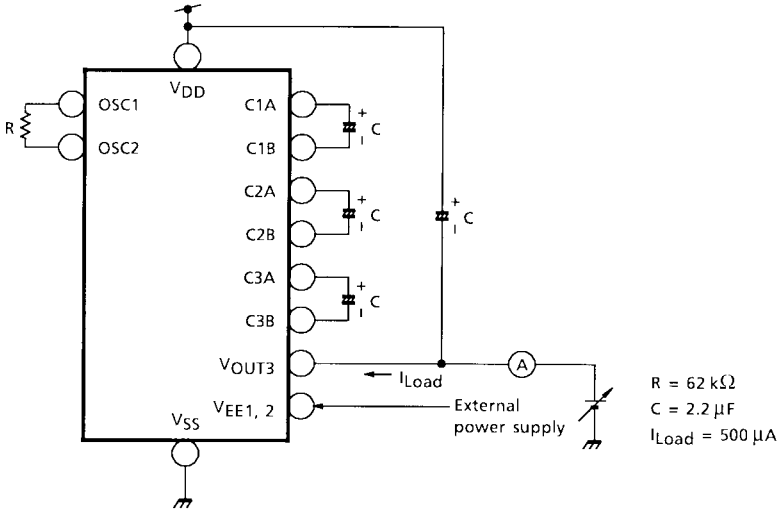
(1) Doubler mode



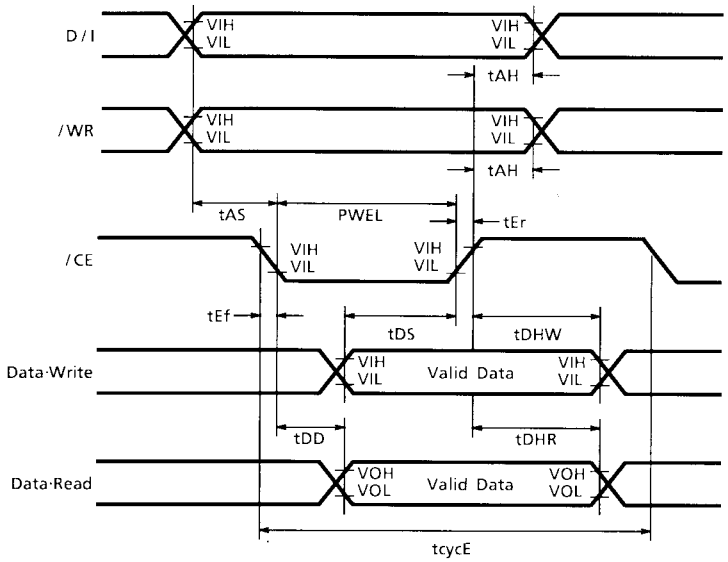
(2) Tripler mode



(3) Quadrupler mode



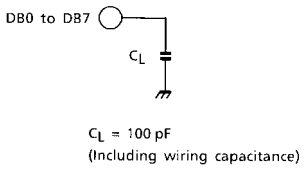
Switching Characteristics



Test Conditions (V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, V_{LC5} = 0 V, Ta = 25°C)

Item	Symbol	Min	Max	Unit
Enable Cycle Time	tcycE	1000	—	ns
Enable Pulse Width	PWEL	450	—	ns
Enable Rise/Fall Time	tEr, tEf	—	25	ns
Address Set-up Time	tAS	100	—	ns
Address Hold Time	tAH	0	—	ns
Data Set-up Time	tDS	280	—	ns
Data Hold Time	tDHW	20	—	ns
Data Delay Time	tDD (Note)	—	350	ns
Data Hold Time	tDHR (Note)	20	—	ns

Load Circuit



Test Conditions (V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, V_{LC5} = 0 V, Ta = 25°C)

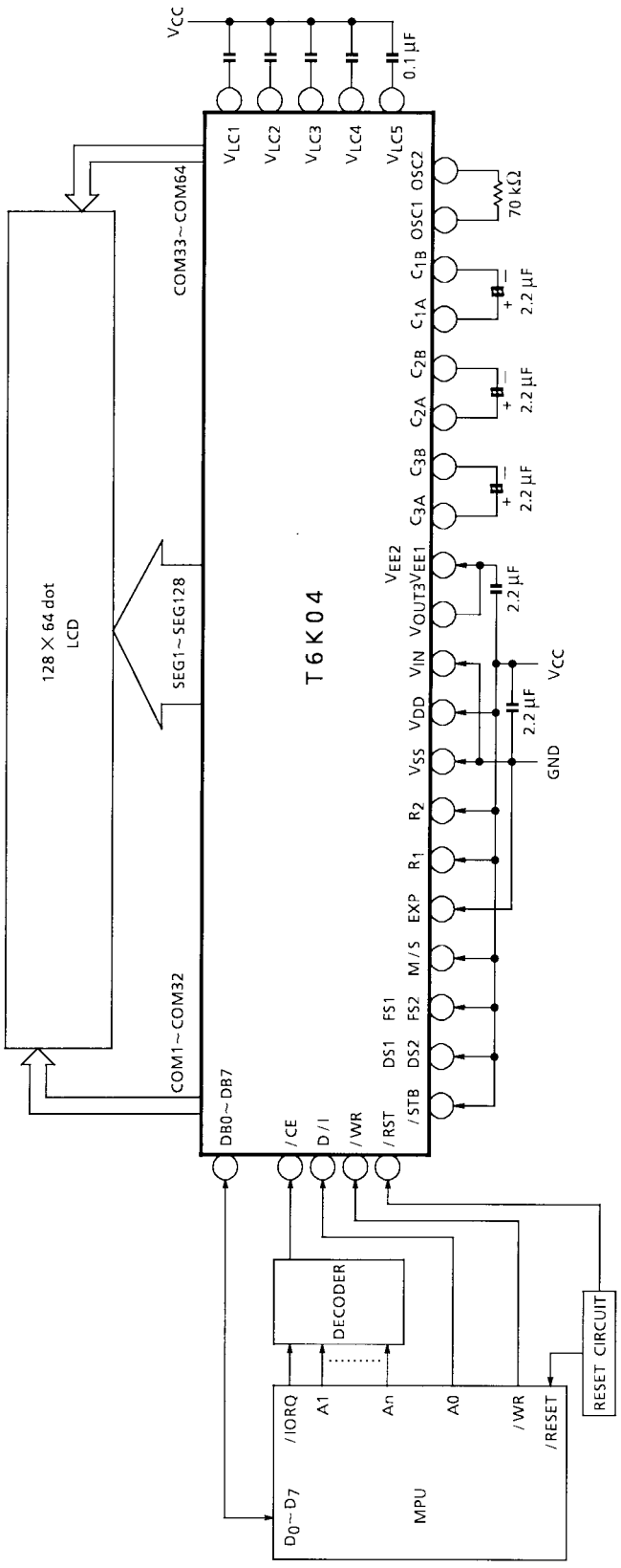
Item	Symbol	Min	Max	Unit
Enable Cycle Time	tcycE	500	—	ns
Enable Pulse Width	PWEL	220	—	ns
Enable Rise/Fall Time	tEr, tEf	—	20	ns
Address Set-up Time	tAS	60	—	ns
Address Hold Time	tAH	0	—	ns
Data Set-up Time	tDS	60	—	ns
Data Hold Time	tDHW	10	—	ns
Data Delay Time	tDD (Note)	—	160	ns
Data Hold Time	tDHR (Note)	20	—	ns

Note: Connect to Load circuit.

Application

(1) T6K04 Circuit single-chip mode

- Oscillation frequency is at a maximum.
- LCD drive bias is 1/9.
- DC–DC Converter is used.



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000707EBE

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- Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.
  This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.
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