TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T6F19,JT6F19-AS

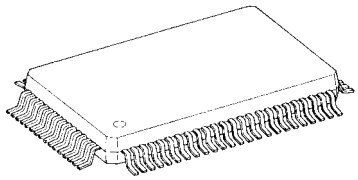
T6F19, JT6F19-AS CMOS Single-Chip LSI for LCD Calculator

The T6F19, JT6F19-AS is a CMOS single-chip microcomputer for 12-digit capacity 1-memory calculation.

T6F19, JT6F19-AS is the complete single chip CMOS LSI for calculator with single power supply operation.

Wide operating voltage range and low power consumption make it suitable for 1.5 V solar battery operated.

Besides T6F19, JT6F19-AS can selectable with a pin-programmable to function of Power timer and Memory hold. With the following features.



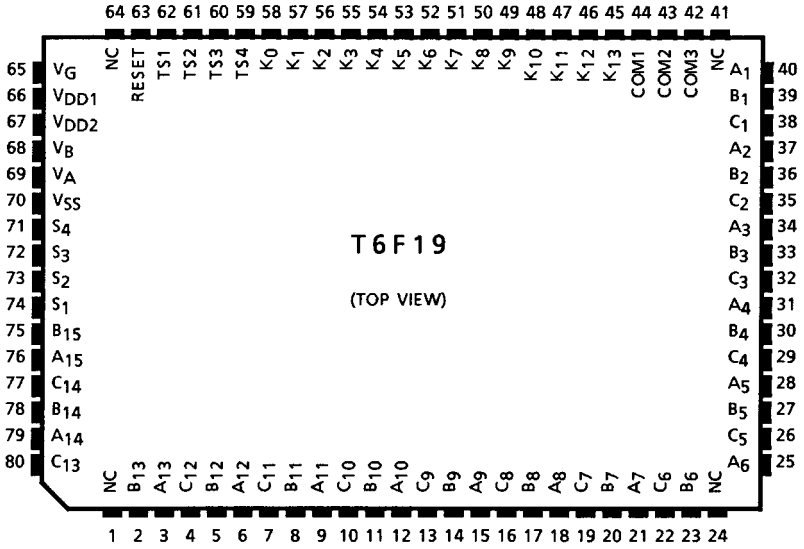
QFP80-P-1420-0.80A

Weight: 1.52 g (typ.)

Features

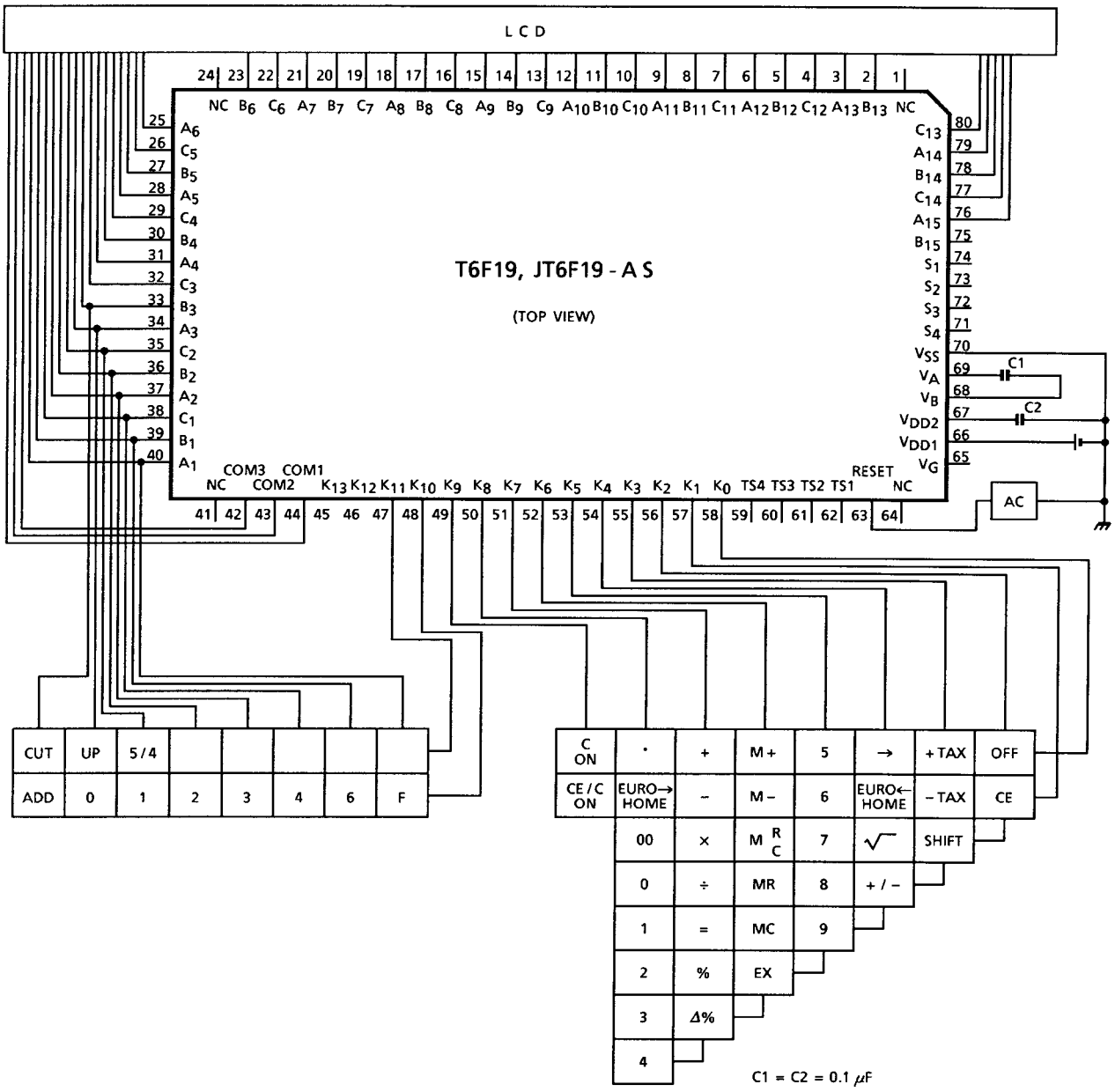
- Display: 12 digits (selectable with a pin-programmable) of data, 2 digits of sign, error symbol, memory load symbol.
- Algebraic mode.
- Standard 4 functions (+, −, ×, ÷)
- Rate conversion calculation
- Automatic percentage operation with add-on, discount.
- Automatic delta percentage, mark-up and markdown operations.
- Square root.
- Constant calculation.
- Chain calculation.
- Change sign.
- Floating point or momentary mode (selectable with a switch).
- Fixed point (“0”, “1”, “2”, “3”, “4” or “6” places) or floating point (selectable with a switch).
- Adding point mode (selectable with a switch).
- Rounding switches (rounding up, down and off).
- Leading zero suppression.
- Trailing zero suppression.
- Punctuation on display, commas for thousands.
- Memory contents indicator, turned on with non-zero in the memory.
- Registration overflow, indicating that too many digits are entered (the most significant digit are protected).
- Result overflow, indicating during calculation (most function key are locked as it happened).
- Memory overflow indicating to flashing of memory load mark.
- Key roll over function.
- Floating minus.

Pin Assignment (top view)

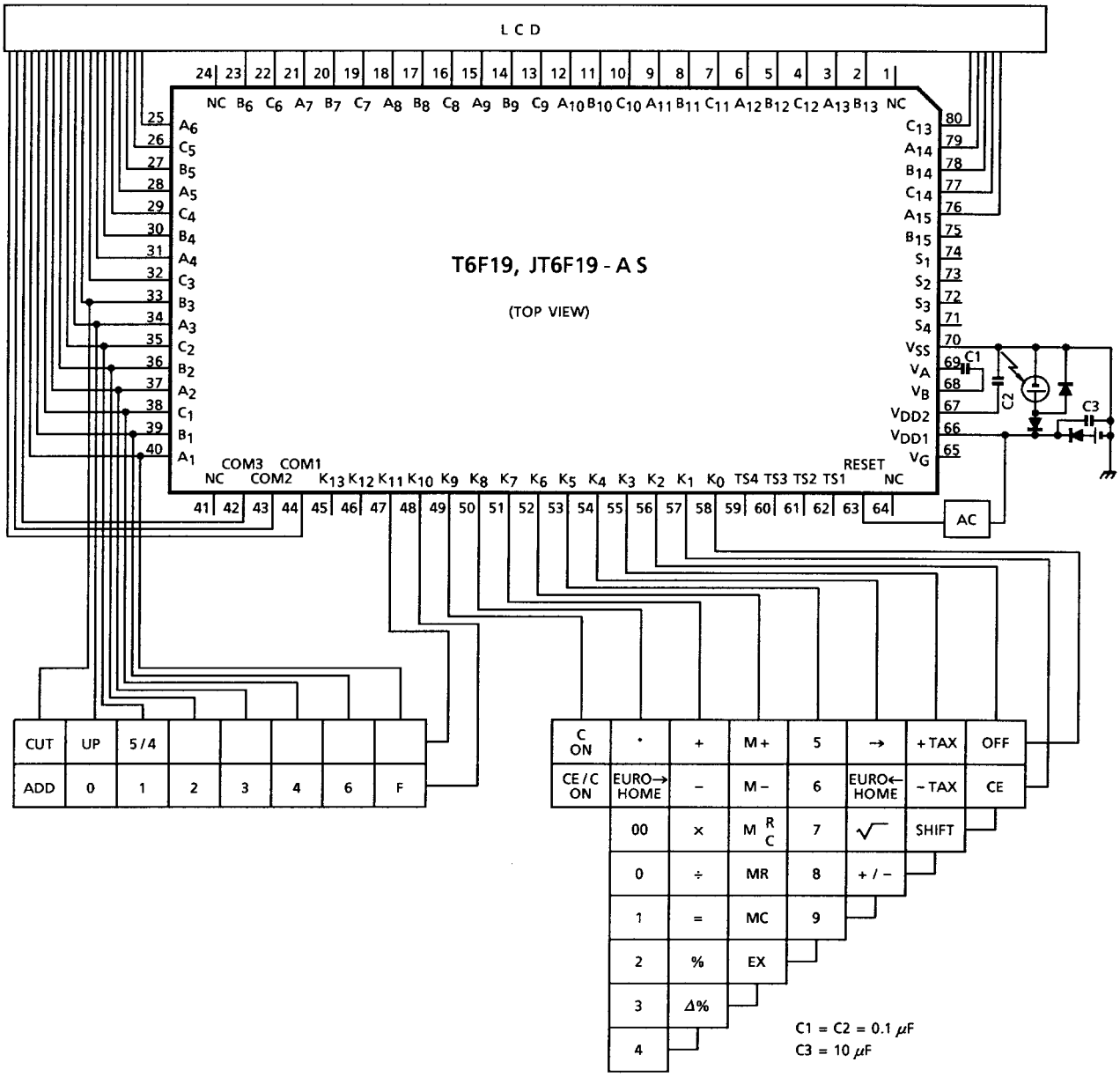


System Block Diagram

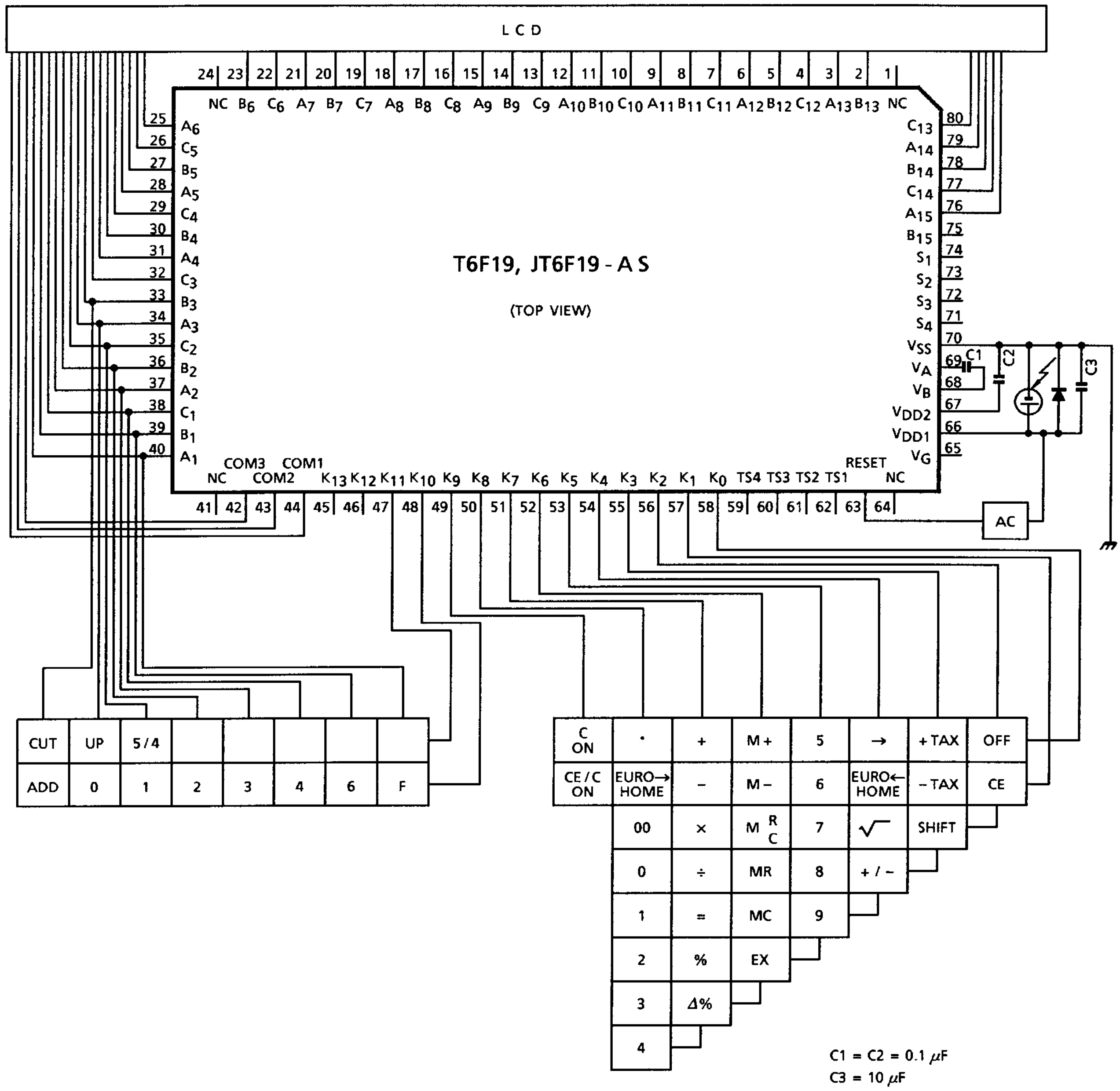
Battery Type



Dual Type

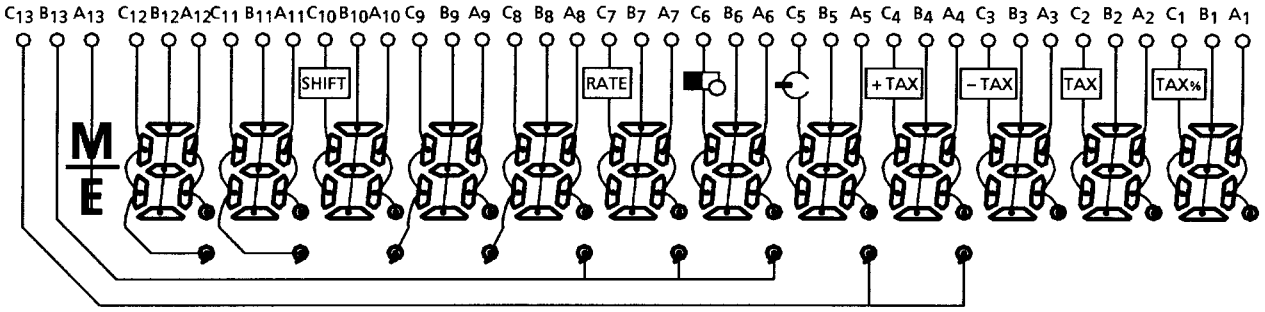

LCD
T6F19, JT6F19 - A S
(TOP VIEW)
C1 = C2 = 0.1 μF
C3 = 10 μF
AC
CUT UP 5/4 ADD 0 1 2 3 4 6 F
C ON CE/C ON EURO→ HOME 00 0 1 2 3 4 · + − × ÷ = % Δ% M+ M− MRC MR MC EX 5 6 7 8 9 → EURO← HOME √ +/− +TAX −TAX SHIFT OFF CE

Solar Type

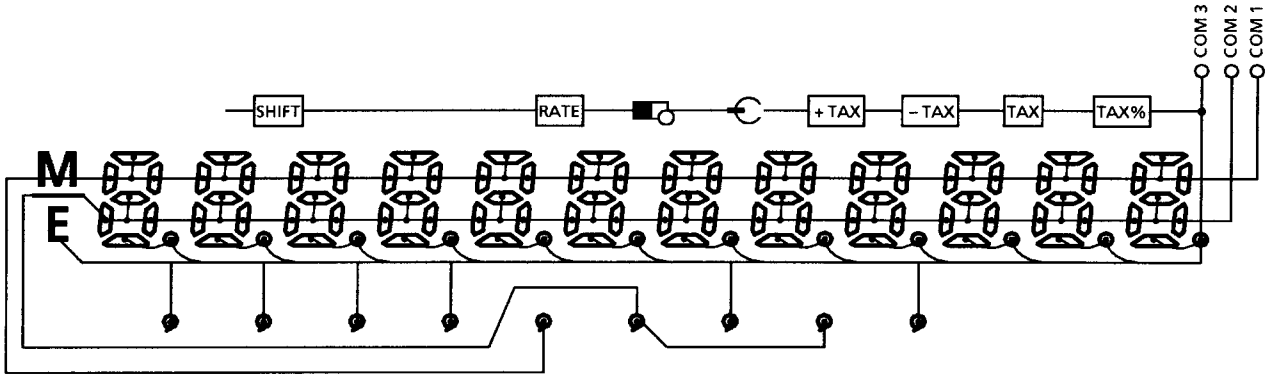

LCD
T6F19, JT6F19-AS
(TOP VIEW)
NC B6 C6 A7 B7 C7 A8 B8 C8 A9 B9 C9 A10 B10 C10 A11 B11 C11 A12 B12 C12 A13 B13 NC
A6 C5 B5 A5 C4 B4 A4 C3 B3 A3 C2 B2 A2 C1 B1 A1
C13 A14 B14 C14 A15 B15 S1 S2 S3 S4 VSS VA VB VDD2 VDD1 VG
NC COM3 COM2 COM1 K13 K12 K11 K10 K9 K8 K7 K6 K5 K4 K3 K2 K1 K0 TS4 TS3 TS2 TS1 RESET NC
C1 C2 C3
AC
CUT UP 5/4
ADD 0 1 2 3 4 6 F
C ON · + M+ 5 → +TAX OFF
CE/C ON EURO→HOME − M− 6 EURO←HOME −TAX CE
00 × M R C 7 √ SHIFT
0 ÷ MR 8 +/−
1 = MC 9
2 % EX
3 Δ%
4
C1 = C2 = 0.1 μF
C3 = 10 μF

Connection of LCD

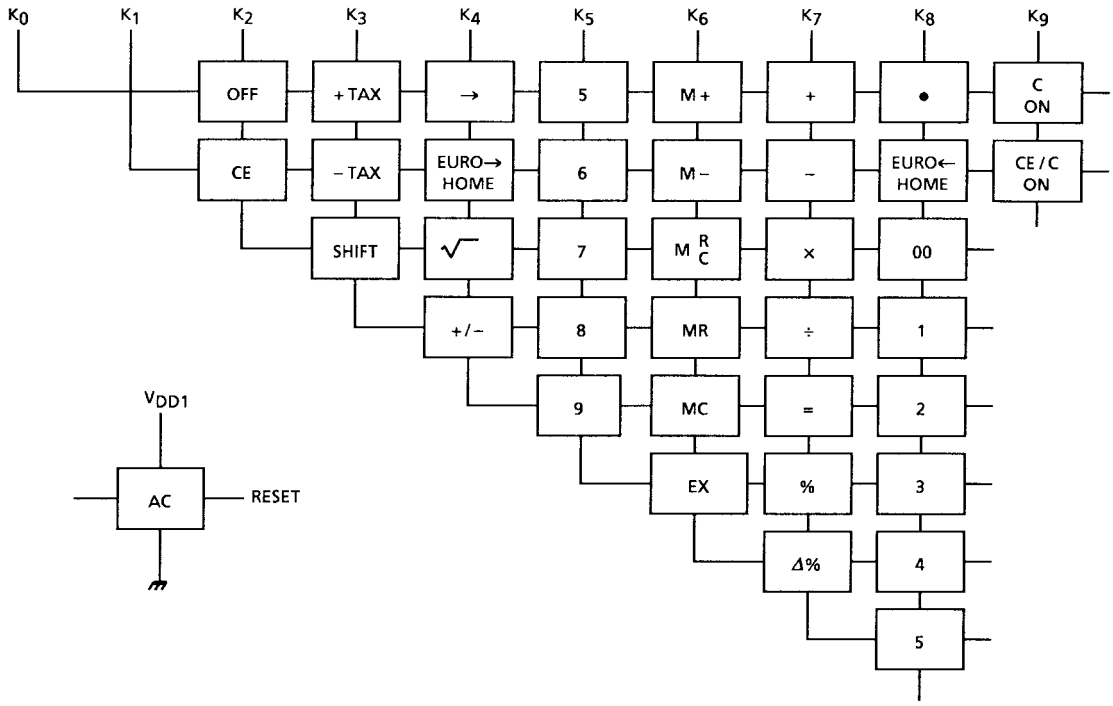
Segment



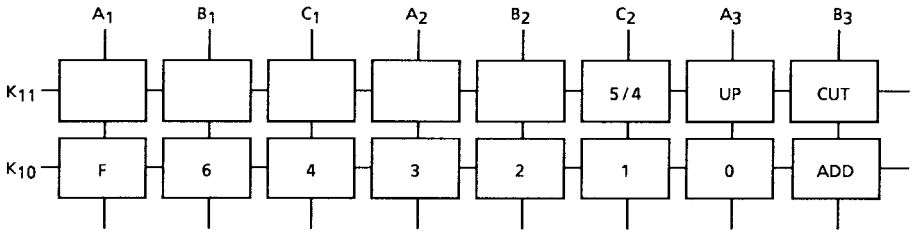
Common



Key Connection



Touch Key



Lock Key

K_{11}: Rounding switches.

K_{10}: Selectable with fixed point or floating mode.

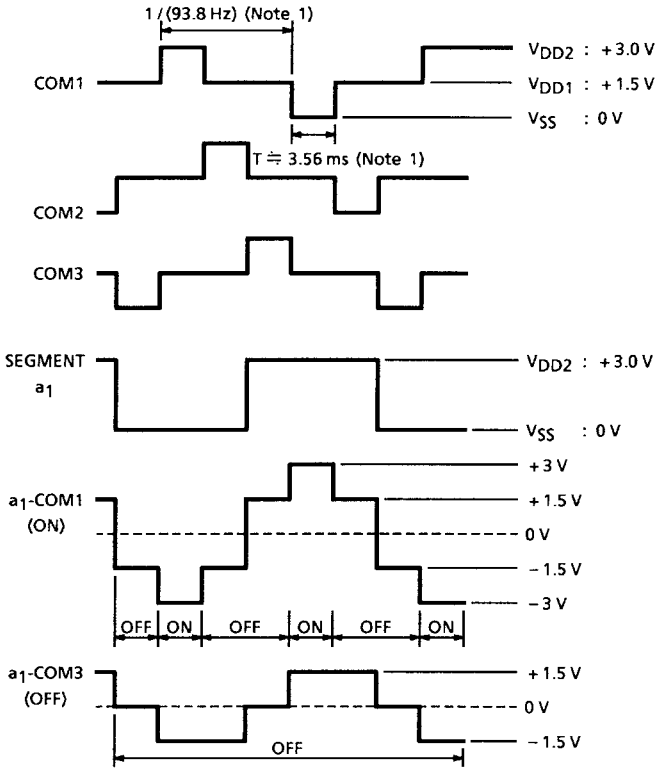
Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD1}	−0.3~2.0	V
Input voltage	V_{IN}	−0.3~V_{DD1} + 0.3	V
Operating temperature	T_{opr}	0~40	°C
Storage temperature	T_{stg}	−55~125	°C

Electrical Characteristics (V_{DD1} = 1.5 ± 0.2 V, V_{DD2} = 3.0 ± 0.4 V, V_{SS} = 0 V, Ta = 25°C)

Characteristics		Symbol	Test Circuit	Pin Name	Test Condition	Min	Typ.	Max	Unit
Operating voltage		V_{DD1}	—	—	—	1.2	1.5	2.0	V
“1” input voltage		$V_{IH\ (1)}$	—	K_2~K_9 RESET	—	V_{DD1} − 0.4	—	V_{DD1}	V
“1” input voltage		$V_{IH\ (2)}$	—	K_{10}~K_{13}	—	V_{DD2} − 0.4	—	V_{DD2}	V
“0” input voltage		V_{IL}	—	K_2~K_{13} RESET	—	0	—	0.4	V
“1” output voltage		$V_{OH\ (1)}$	—	SEGMENT COM1~3	—	V_{DD2} − 0.2	—	V_{DD2}	V
“0” output voltage		$V_{OL\ (1)}$	—	SEGMENT COM1~3	—	0	—	0.2	V
“M” output voltage		V_{OM}	—	COM1~3	—	V_{DD1} − 0.2	—	V_{DD1} + 0.2	V
“1” output voltage		$V_{OH\ (2)}$	—	K_1~K_9	—	V_{DD1} − 0.2	—	V_{DD1}	V
“0” output voltage		$V_{OL\ (2)}$	—	K_1~K_{13}	—	0	—	0.2	V
“1” output resistance		R_{OH}	—	SEGMENT COM1~3	V_{OUT} = V_{DD2} − 0.5 V	—	—	70	kΩ
“0” output resistance		R_{OL}	—	SEGMENT COM1~3	V_{OUT} = 0.5 V	—	—	70	kΩ
Key pull up resistance		$R_{KEYH\ (1)}$	—	RESET	V_{OUT} = V_{DD1} − 0.5 V	—	—	25	kΩ
		$R_{KEYH\ (2)}$	—	K_0~K_9	V_{OUT} = V_{DD1} − 0.5 V	—	—	14	
		$R_{KEYH\ (3)}$	—	K_{10}~K_{13}	V_{OUT} = 0 V	120	—	800	
Key pull down resistance		$R_{KEYL\ (1)}$	—	RESET (1)	V_{OUT} = V_{DD1}	100	—	300	kΩ
		$R_{KEYL\ (2)}$	—	RESET (2)	V_{OUT} = V_{DD1}	18	—	300	
		$R_{KEYL\ (3)}$	—	K_0~K_9 (1)	V_{OUT} = 0.5 V	—	—	50	
		$R_{KEYL\ (4)}$	—	K_0~K_9 (2)	V_{OUT} = V_{DD1}	72	—	170	
Oscillating (WAIT)		fϕWAIT	—	—	V_{DD1} = 1.5 V	5.4	9.0	15.5	kHz
Frequency (OPERATE)		fϕOP	—	—	V_{DD1} = 1.5 V	20.0	34	61.3	kHz
Frame frequency		f_F	—	SEGMENT COM1~3	V_{DD1} = 1.5 V	56.3	93.8	161.5	Hz
Supply current	1 (WAIT)	I_{DDWAIT}	—	—	V_{DD1} = 1.5 V	—	—	3.3	μA
	2 (OPERATE)	I_{DDOP}	—	—	V_{DD1} = 1.2 V	—	—	8.9	
	3 (OFF)	I_{DDOFF}	—	—	V_{DD1} = 1.5 V	—	—	2.0	
Power off timer times		T	—	—	V_{DD1} = 1.5 V	429	600	1001	s

Waveforms for Display



Note 1: at f_ϕ = 9 kHz

Pad Location Table

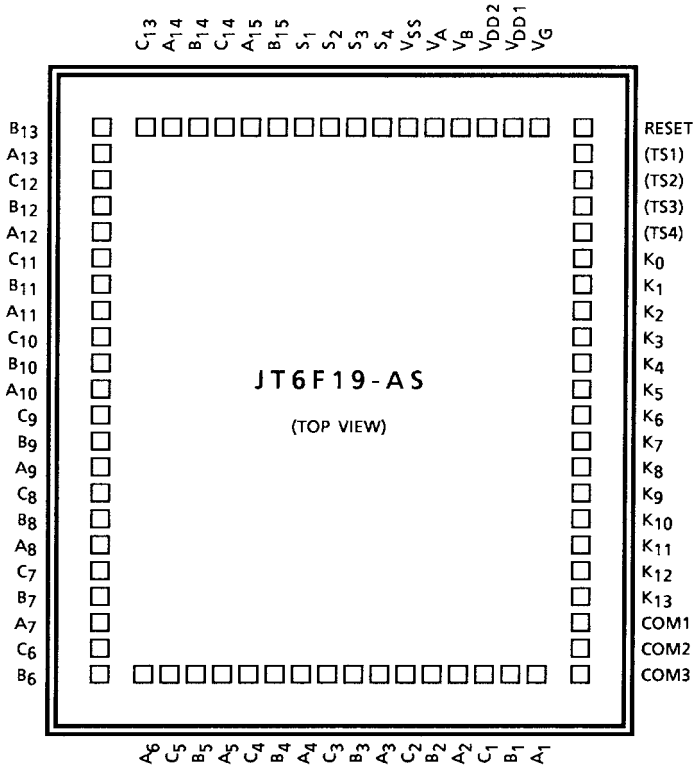
(μm)

Name	X Point	Y Point
B_6	−1757	−1680
C_6	−1757	−1520
A_7	−1757	−1360
B_7	−1757	−1200
C_7	−1757	−1040
A_8	−1757	−880
B_8	−1757	−720
C_8	−1757	−560
A_9	−1757	−400
B_9	−1757	−240
C_9	−1757	−80
A_{10}	−1757	80
B_{10}	−1757	240
C_{10}	−1757	400
A_{11}	−1757	560
B_{11}	−1757	720
C_{11}	−1757	880
A_{12}	−1757	1040
B_{12}	−1757	1200
C_{12}	−1757	1360
A_{13}	−1757	1520
B_{13}	−1757	1680
C_{13}	−1089	1753
A_{14}	−929	1753
B_{14}	−769	1753
C_{14}	−609	1753
A_{15}	−449	1753
B_{15}	−289	1753
S_1	−129	1753
S_2	31	1753
S_3	191	1753
S_4	351	1753
V_{SS}	511	1753
V_A	671	1753
V_B	831	1753
V_{DD2}	991	1753
V_{DD1}	1151	1753
V_G	1388	1753

Name	X Point	Y Point
RESET	1757	1680
(TS1)	1757	1520
(TS2)	1757	1360
(TS3)	1757	1200
(TS4)	1757	1040
K_0	1757	880
K_1	1757	720
K_2	1757	560
K_3	1757	400
K_4	1757	240
K_5	1757	80
K_6	1757	−80
K_7	1757	−240
K_8	1757	−400
K_9	1757	−560
K_{10}	1757	−720
K_{11}	1757	−880
K_{12}	1757	−1040
K_{13}	1757	−1200
COM1	1757	−1360
COM2	1757	−1520
COM3	1757	−1680
A_1	1122	−1752
B_1	962	−1752
C_1	802	−1752
A_2	642	−1752
B_2	482	−1752
C_2	322	−1752
A_3	162	−1752
B_3	2	−1752
C_3	−158	−1752
A_4	−318	−1752
B_4	−478	−1752
C_4	−638	−1752
A_5	−798	−1752
B_5	−958	−1752
C_5	−1118	−1752
A_6	−1278	−1752

Note 2: ( ) Do not connect.

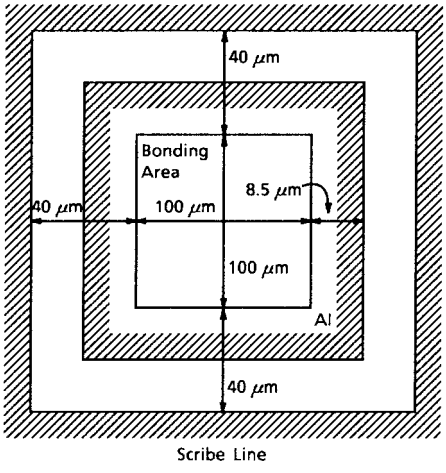
Chip Layout



Chip size : 3.79 x 3.84 (mm)
Chip thickness : 440 ± 30 (μm)
Substrate : V_{SS}

Pad Layout

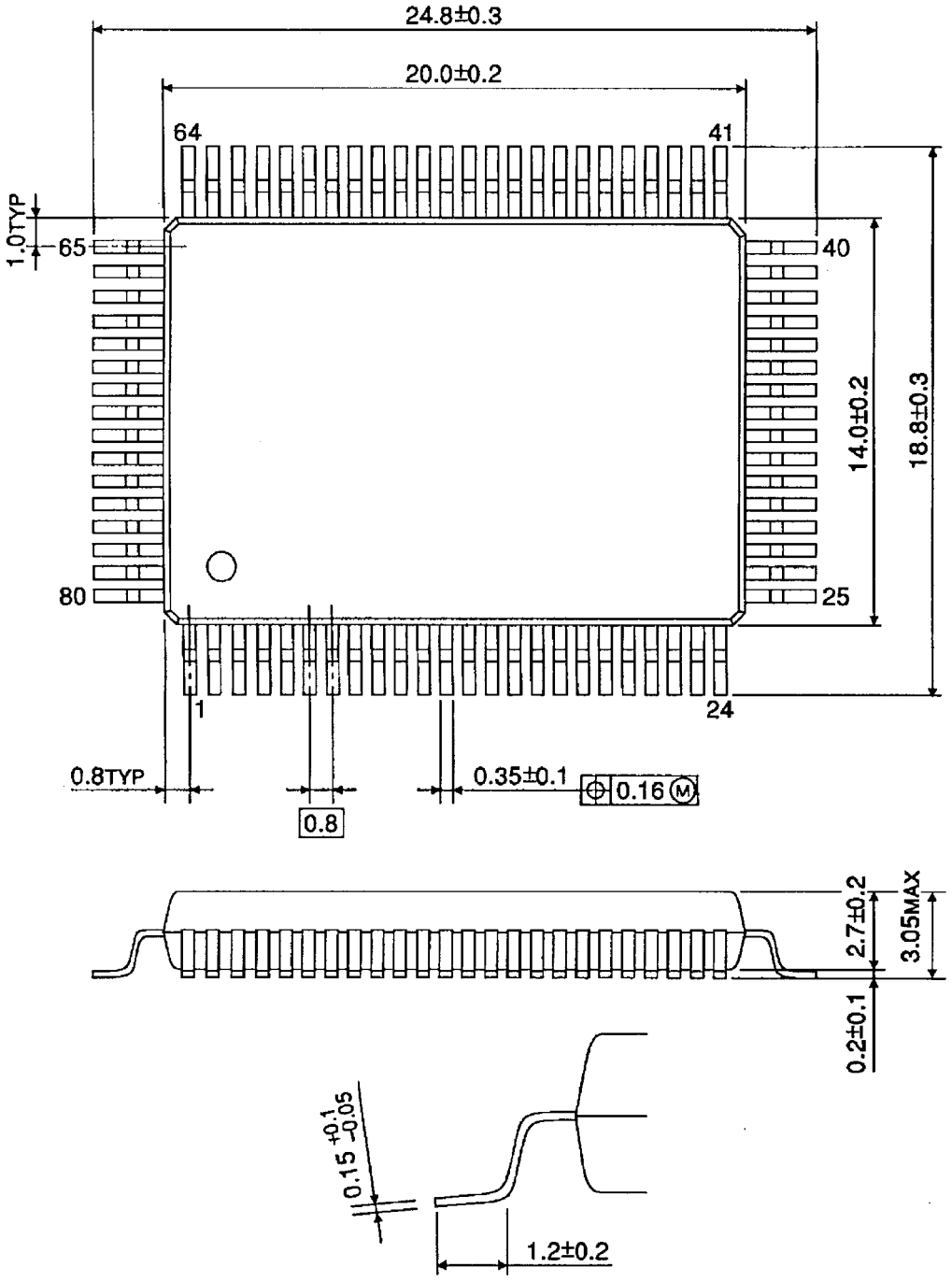
Active Element



PAD Pitch 160 μm

Package Dimensions

QFP80-P-1420-0.80A Unit : mm



Weight: 1.52 g (typ.)

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