TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

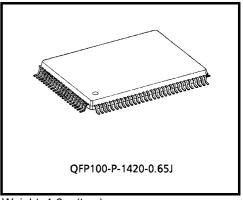
T6A92

COLUMN DRIVER LSI FOR A DOT MATRIX LCD

The T6A92 is a column driver with 80 output channels for a dot matrix LCD. The T6A92 realizes low power LCD systems using the CMOS Si-Gate process. The T6A92 has two types of data flow. (1) $O_1 \rightarrow O_{80}$, (2) $O_{80} \rightarrow O_1$

Features

- 80-output column driver
- Data input format : 1-bit (ENABLE mode) : 2-bit (SHIFT mode)
- Two types of data flow:
 - (1) $O_1 \rightarrow O_{80}$
 - (2) $O_{80} \rightarrow O_1$
- Low power consumption
- Power supply $: 5 V \pm 10\%$
- 100-pin plastic flat package



Weight: 1.6 g (typ.)

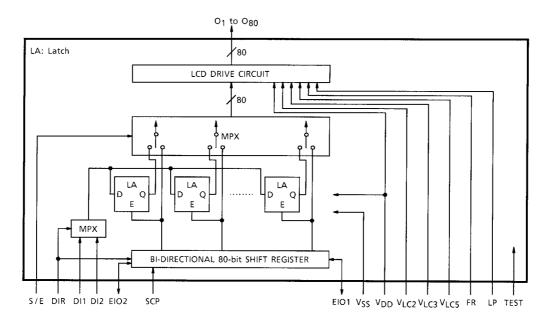
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Pin Assignment

		Ŋ	NC	E I 01	۷ _{LC5}	v _{LC3}	V _{LC2}	D11	NC	NC	D12	۲ _{DD}	DIR	NC	V _{SS}	TEST	S/E	۲P	FR	SCP	E 102		
	1	10) 99	98	97	96	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81		1
o1	1		\sim																			80	080
o2	2	(\bigcirc																			79	079
o3	3																					78	078
04	4																					77	077
05	5																					76	076
06	6																					75	075
07	7																					74	074
08	8																					73	073
	9																					72	072
	10																					71	071
011	11																					70	070
012	12																						069
013	13									T	6 A		2										068
014 015	14									1	θA	19	Z										067
015	15									(T	OP	VIEV	V)										066
018	I																						065
018	1																						064
019	1																						063
020	I																						
021	21																						061 060
022	22																					I	o59
o23	23																					- 1	059
o24	24																						057
o25	25																					1	056
026	26																						055
o27	27																					. L	054
o28	28																					. L	053
029	29																					L L	o52
o30	30																				!		051
		31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	ノ	
		031	032	033	034	035	036	037	038	039	040	041	042	043	044	045	046	047	048	049	050		

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Block Diagram



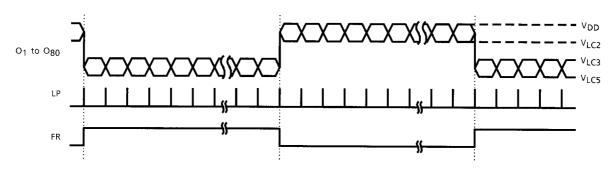
Pin Functions

Pin Name	1/0	Functions	Level
O1 to O80	Output	LCD drive signal output	V _{DD} to V _{LC5}
DI1, DI2	Input	Data signal input	
EIO1, EIO2	1/0	ENABLE signal input / output When S / E = H, this pin is for input.	
SCP	Input	(Shift Clock Pulse) Shift clock pulse input	
FR	Input	(Frame) Frame signal input	V_{DD} to V_{SS}
LP	Input	(Latch Pulse) Latch pulse signal input	
S / E	Input	Input for mode selection	
DIR	Input	Input data flow direction select	
TEST	Input	Test pin: usually connected to V _{SS} (0 V)	
V _{LC2, 3, 5}	—	Power supply for LCD drive	
V _{DD}	_	Power supply (5 V)	—
V _{SS}	_	Power supply (0 V)	

Function of Data and Enable Pins

-	/ E IR	DI1	DI2	EIO1	EIO2	Data Flow	First Data	Last Data	Mode
L	L	Open	DATA INPUT	ENABLE signal input	ENABLE signal output	$O_{80} \rightarrow O_1$	0 ₁	O ₈₀	ENABLE
L	н	DATA INPUT	Open	ENABLE signal output	ENABLE signal input	$O_1 \rightarrow O_{80}$	O ₈₀	0 ₁	LNADLL
н	L	Open	Open	DATA INPUT	DATA OUTPUT	$O_1 \rightarrow O_{80}$	O ₈₀	0 ₁	SHIFT
н	н	Open	Open	DATA OUTPUT	DATA INPUT	$O_{80} \rightarrow O_1$	0 ₁	0 ₈₀	

Timing Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage (1)	V _{DD} (Note 1)	-0.3 to 7.0	V
Supply Voltage (2)	V _{LC2} , V _{LC3} , V _{LC5} (Note 1, 2)	-0.3 to 7.0	V
Input Voltage	V _{IN} (Note 1)	-0.3 to V _{DD} + 0.3	V
Operating Temperature	T _{opr}	-20 to 75	°C
Storage Temperature	T _{stg}	−55 to 125	°C

Note 1: Referenced to V_{SS} = 0 V

Note 2: Ensure that the following condition is always maintained. $V_{DD} \ge V_{LC2} \ge V_{LC3} \ge V_{LC5}$

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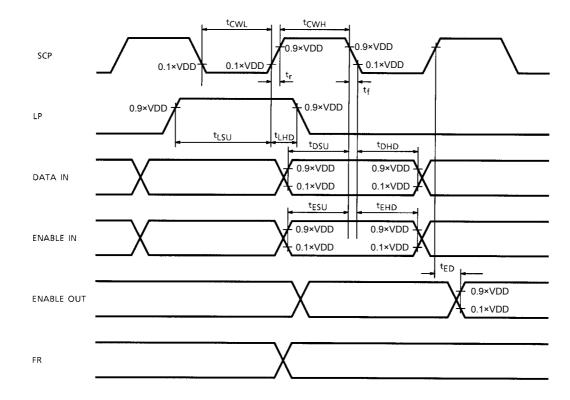
Electrical Characteristics DC Characteristics Test Conditions (Unless Otherwise Noted, $V_{SS} = 0 V$, $V_{DD} = 5.0 V \pm 10\%$, $V_{LC5} = 0 V$, Ta = -20 to 75°C)

lte	m	Symbol	Test Circuit	Test C	Min	Тур.	Max	Unit	Pin Name	
Operating	Voltage (1)	V _{DD}	—	-	4.5	5.0	5.5	V	V _{DD}	
Operating	/oltage (2)	V_{LC5}	_	-		0	_	V _{DD} -3.0	V	V _{LC5}
Input	H Level	V _{IH}	_	_		V _{DD} -1.0	_	V _{DD}	V	(Note)
voltage	L Level	VIL	_	—		0	_	1.0	V	(Note)
Output	H Level	V _{OH}	_	I _{OH} = −0.4 mA		V _{DD} -0.4	_	V _{DD}	V	EIO1, EIO2
voltage	L Level	V _{OL}	_	I _{OH} = 0.4 mA		0	_	0.4	V	EIO1, EIO2
Output Res	sistance	R _{COL}	_	I _d = ± 50 μA		_		30	kΩ	O ₁ to O ₈₀
Operating I	requency	f _{scp}	_	$T_a = -20$ to $75^{\circ}C$		-		400	kHz	SCP
Current Consumption		nsumption I _{SS}		$V_{DD} = 5.0 V$ $V_{LC2} = 3.0 V$ $V_{LC3} = 2.0 V$ $V_{LC5} = 0.0 V$	Binary Data Input	_	_	1.0	mA	
				f _{FR} = 39 Hz f _{scp} = 250 kHz O ₁ to O ₈₀ : No Load	Input Data : LOW Constant	_	_	0.4	mA	V _{SS}

Note: SCP, LP, FR, EIO1, EIO2, DI1, DI2, DIR, S / E, TEST

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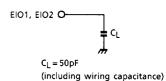
AC Characteristics



Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 5 V ± 10%, V_{LC5} = 0 V, Ta = -20 to 75°C)

Item	Symbol	Min	Max	Unit
Operating Frequency	f _{scp}	_	400	kHz
SCP Pulse Width	t _{CWH} , t _{CWL}	800	_	ns
SCP Rise / Fall Time	t _r , t _f		200	ns
LP Set-up Time	tLSU	500	—	ns
LP Hold Time	tLHD		10	ns
Data Set-up Time	t _{DSU} (Note 1)	300	—	ns
Data Hold Time	t _{DHD} (Note 1)	300	—	ns
Enable Set-up Time	t _{ESU} (Note 2)	300	—	ns
Enable Hold Time	t _{EHD} (Note 2)	300	_	ns
Enable Delay Time	t _{ED} (Note 3)		500	ns

Load Circuit



Note 1: Applies to DI1 and DI2

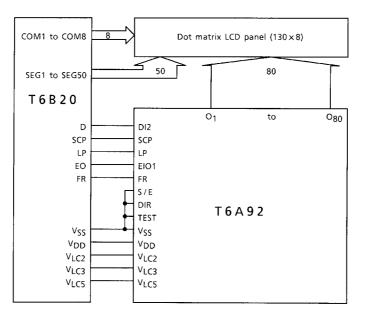
Note 2: Applies to EIO1 and EIO2

Note 3: With load circuit connected

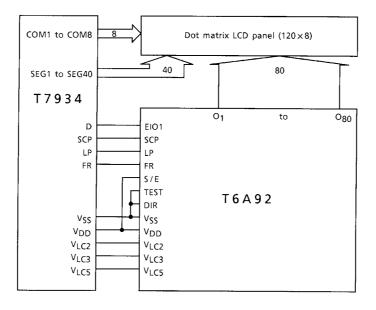
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Application Circuit

• S / E = L (ENABLE mode)

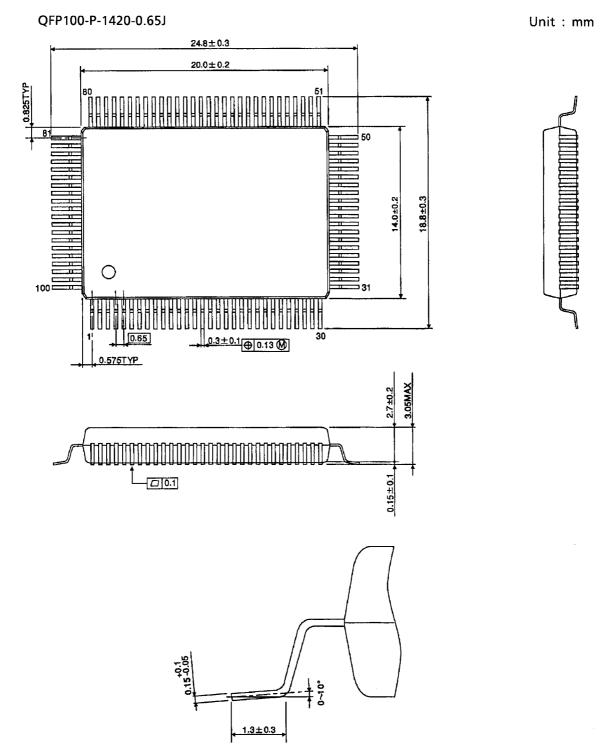


• S / E = H (SHIFT mode)



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Package Dimensions





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