Features

- **Low-power, Low-voltage Operation**
- **Contactless Power Supply**
- **Contactless Read/Write Data Transmission**
- **Radio Frequency (RF): 100 kHz to 150 kHz**
- **264-bit EEPROM Memory in 8 Blocks of 33 Bits**
- **224 Bits in Seven Blocks of 32 Bits are Free for User Data**
- **Block Write Protection**
- **Extensive Protection Against Contactless Malprogramming of the EEPROM**
- **On-chip Resonance Capacitor (70 or 200 pF Mask Option)**
- **Anticollision Using Answer-On-Request (AOR)**
- **Typical < 50 ms to Write and Verify a Block**
- **Other Options Set by EEPROM:**
  - **Bitrate [bit/s]: RF/8, RF/16, RF/32, RF/40, RF/50, RF/64, RF/100, RF/128**
  - **Modulation: BIN, FSK, PSK, Manchester, Biphase**
  - **Other: Terminator Mode, Password Mode, AOR Mode**

Description

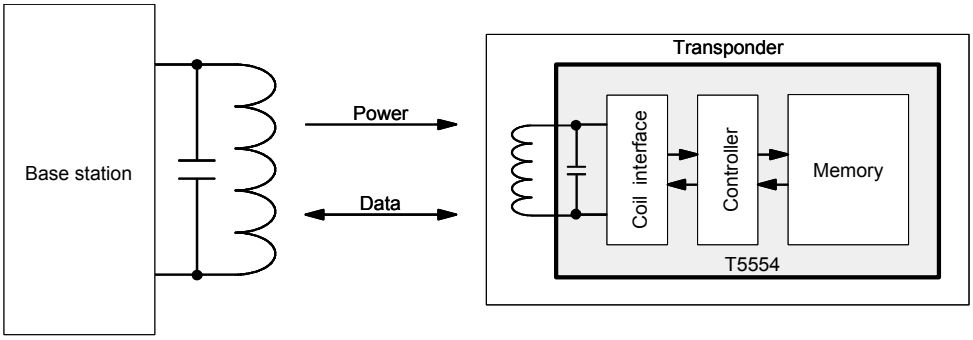
The T5554 is a contactless R/W-**ID**entification **IC** (IDIC®) for general-purpose applications in the 125 kHz range. A single coil, connected to the chip, serves as the IC's power supply and bidirectional communication interface. The coil and chip together form a transponder.

The on-chip 264-bit EEPROM (8 blocks 33 bits each) can be read and written blockwise from a base station. The blocks can be protected against overwriting. One block is reserved for setting the operation modes of the IC. Another block can contain a password to prevent unauthorized writing.

Reading occurs by damping the coil by an internal load. There are different bitrates and encoding schemes possible. Writing occurs by interrupting the RF field in a special way.

System Block Diagram

Figure 1. RFID System Using T5554 Tag



Standard R/W IDIC (264 Bit) with Integrated Capacitance

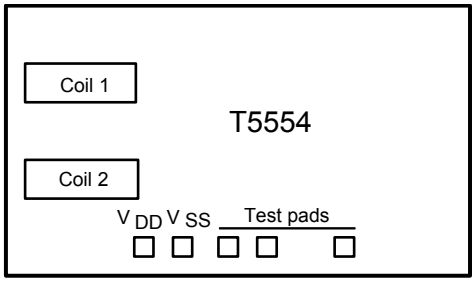
T5554

Preliminary

Rev. 4576A–RFID–12/02

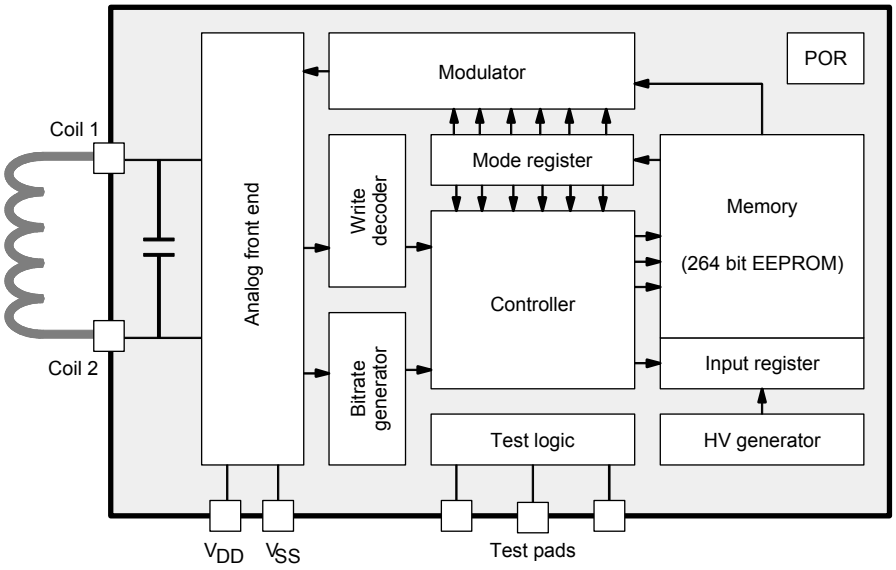
Pad Layout

Figure 2. Pad Layout of T5554



T5554 Building Blocks

Figure 3. Block Diagram



Analog Front End (AFE)

The AFE includes all circuits which are directly connected to the coil. It generates the IC's power supply and handles the bidirectional data communication with the reader unit. It consists of the following blocks:

- Rectifier to generate a DC supply voltage from the AC coil voltage
- Clock extractor
- Switchable load between Coil1/Coil2 for data transmission from the IC to the reader unit (read)
- Field gap detector for data transmission from the reader unit into the IC (write)

Resonance Capacitor

The resonance capacitor is integrated on chip. By mask option the value can be 70 pF or 200 pF typically.

Controller

The main controller has the following functions:

- Load mode register with configuration data from EEPROM block 0 after power-on and also during reading
- Control memory access (read, write)
- Handle write data transmission and the write error modes
- The first two bits of the write data stream are the OP-code. There are two valid OP-codes (standard and stop) which are decoded by the controller.
- In password mode, the 32 bits received after the OP-code are compared with the stored password in block 7.

Bitrate Generator

The bitrate generator can deliver the following bitrates:
RF/8 – RF/16 – RF/32 – RF/40 – RF/50 – RF/64 – RF/100 – RF/128

Write Decoder

Decode the detected gaps during writing. Check if write data stream is valid.

Test Logic

Test circuitry allows rapid programming and verification of the IC during test.

HV Generator

Voltage pump which generates ~18 V for programming of the EEPROM.

Power-On Reset (POR)

The power-on reset is a delay reset which is triggered when supply voltage is applied.

Mode Register

The mode register stores the mode data from EEPROM block 0. It is continually refreshed at the start of every block. This increases the reliability of the device (if the originally loaded mode information is false, it will be corrected by subsequent refresh cycles).

Modulator

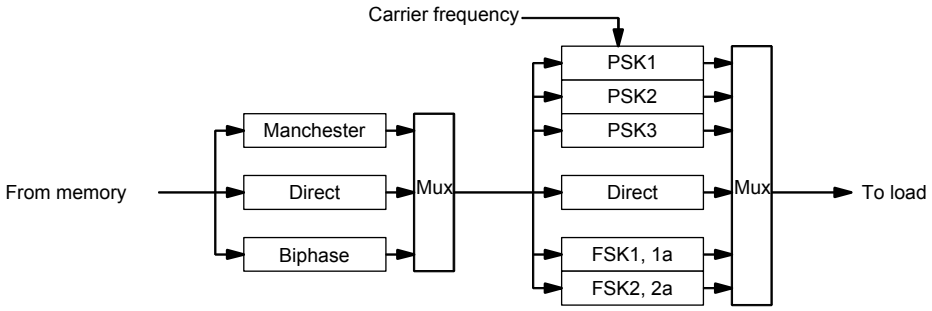
The modulator consists of several data encoders in two stages, which may be freely combined to obtain the desired modulation. The basic types of modulation are:

- PSK: phase shift: 1) every change; 2) every “1”; 3) every rising edge (carrier: fc/2, fc/4 or fc/8)
- FSK: 1) f1 = rf/8 f2 = rf/5; 2) f1 = rf/8, f2 = rf/10
- Manchester: rising edge = H; falling edge = L
- Biphase: every bit creates a change, a data “H” creates an additional mid-bit change

Note: The following modulation type combinations will not work:

- Stage1 Manchester or Biphase and stage2 PSK, at any PSK carrier frequency (because the first stage output frequency is higher than the second stage strobe frequency);
- Stage1 Manchester or Biphase and stage2 PSK with bitrate = rf/8 and PSK carrier frequency = rf/8 (for the same reason as above);
- Any stage1 option with any PSK for bitrates rf/50 or rf/100 if the PSK carrier frequency is not an integer multiple of the bitrate (e.g., br = rf/50, PSKcf = rf/4, because 50/4 = 12.5). This is because the PSK carrier frequency must maintain constant phase with respect to the bit clock.

Figure 4. Modulator Block Diagram



Memory

The memory of the T5554 is a 264-bit EEPROM, which is arranged in 8 blocks of 33 bits each. All 33 bits of a block, including the lock bit, are programmed simultaneously. The programming voltage is generated on-chip.

Block 0 contains the mode data, which are not normally transmitted (see figure 6).

Blocks 1 to 6 are freely programmable. Block 7 may be used as a password. If password protection is not required, it may be used for user data.

Bit 0 of every block is the lock bit for that block. Once locked, the block (including the lockbit itself) cannot be field-reprogrammed.

Data from the memory is transmitted serially, starting with block 1, bit 1, up to block “MAXBLK”, bit 32. “MAXBLK” is a mode parameter set by the user to a value between 0 and 7 (if maxblk = 0, only block 0 will be transmitted).

Figure 5. Memory Map

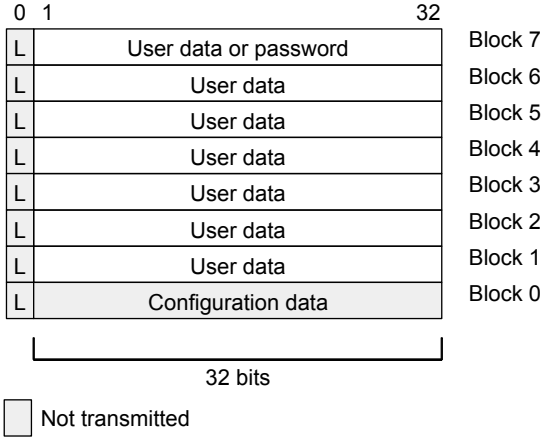
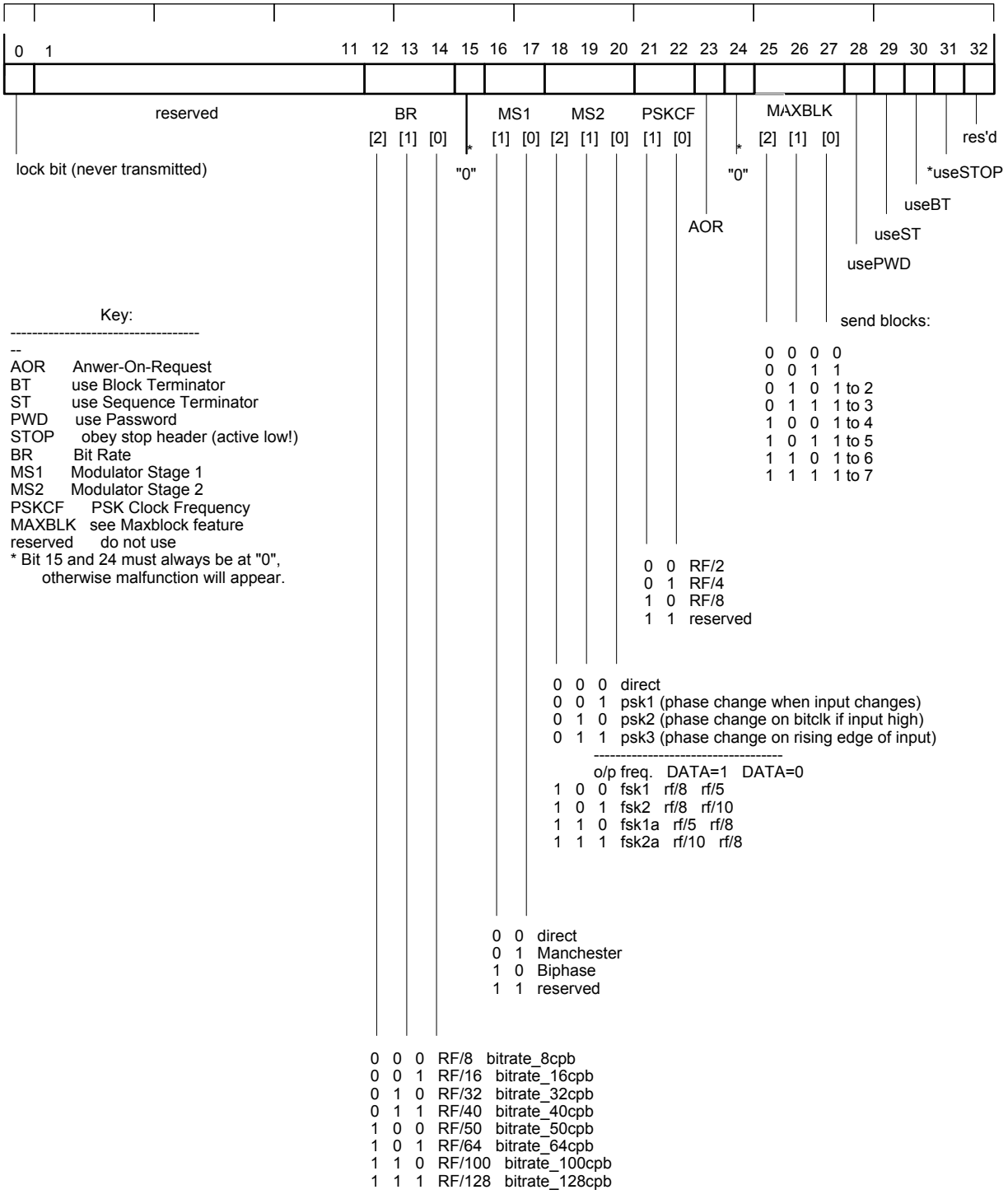


Figure 6. Memory Map of Block 0



Operating the T5554

General

The basic functions of the T5554 are: supply IC from the coil, read data from the EEPROM to the reader, write data into the IC and program these data into the EEPROM. Several errors can be detected to protect the memory from being written with the wrong data (see figure 21).

Supply

The T5554 is supplied via a tuned inductance (L ~ 8 mH) which is connected to the Coil 1 and Coil 2 pads. The incoming RF (actually a magnetic field) induces a current into the coil. The on-chip rectifier generates the dc supply voltage (V_{DD}, V_{SS} pads). Overvoltage protection prevents the IC from damage due to high-field strengths. Depending on the coil, the open-circuit voltage across the LC circuit can reach more than 100 V. The first occurrence of RF triggers a power-on reset pulse, ensuring a defined start-up state.

Read

Reading is the default mode after power-on reset. It is done by switching a load between the coil pads on and off. This changes the current through the IC coil, which can be detected from the reader unit.

Start-up

The many different modes of the T5554 are activated after the first readout of block 0. The modulation is off while block 0 is read. After this set-up time of 256 field clock periods, modulation with the selected mode starts.

Any field gap during this initialization will restart the complete sequence.

Read Data Stream

The first block transmitted is block 1. When the last block is reached, reading restarts with block 1. Block 0, which contains mode data, is normally never transmitted. However, the mode register is continuously refreshed with the contents of EEPROM block 0.

Figure 7. Application Circuit

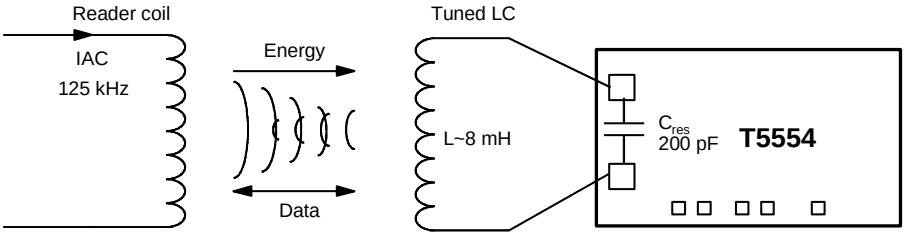


Figure 8. Voltage at Coil1/Coil2 After Power-on

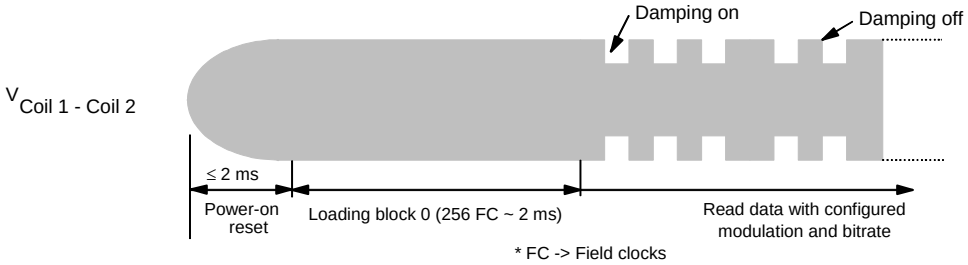


Figure 9. Terminators

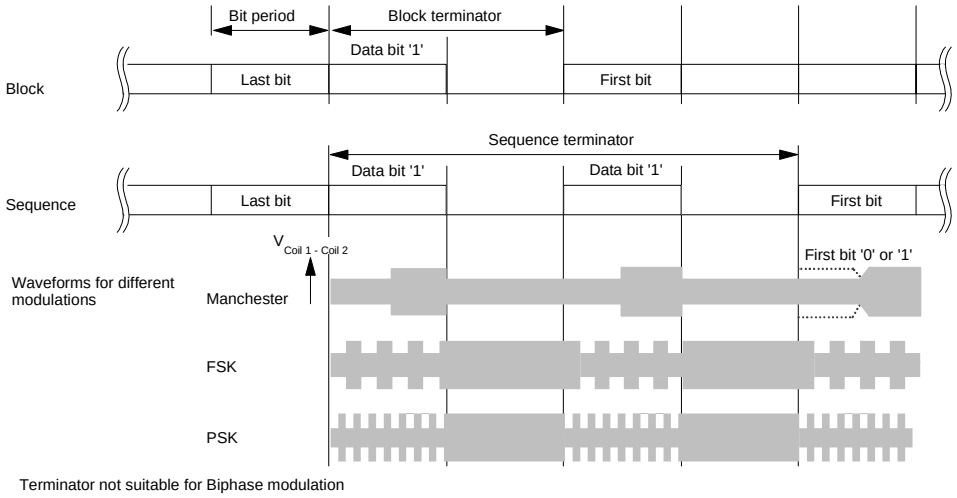


Figure 10. Read Data Streams and Terminators

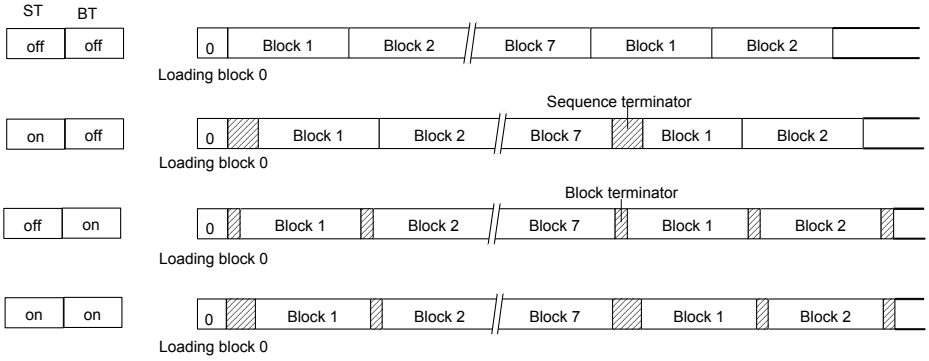
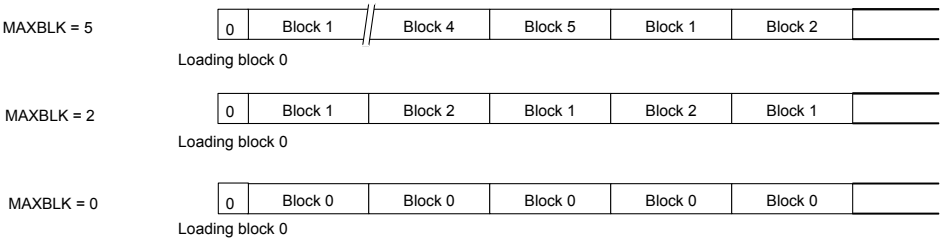


Figure 11. MAXBLK Examples



Maxblock Feature

If it is not necessary to read all user data blocks; the MAXBLK field in block 0 can be used to limit the number of blocks read. For example, if MAXBLK = 5, the T5554 repeatedly reads and transmits only blocks 1 to 5 (see figure 11). If MAXBLK is set to “0”, block 0 - which is normally not transmitted - can be read.

Terminators

The terminators are (optionally selectable) special damping patterns, which may be used to synchronize the reader. There are two types available; a block terminator which precedes every block, and a sequence terminator which always follows the last block.

The sequence terminator consists of two consecutive block terminators. The terminators may be individually enabled with the mode bits ST (Sequence Terminator enable) or BT (Block Terminator enable).

Note: It is not possible to include a sequence terminator in a transmission where MAXBLK = 0.

Direct Access

The direct access command allows the reading of an individual block by sending the OP-code (“10”), the lock-bit and the 3-bit address.

Note: PWD has to be 0.

Modulation and Bitrate

There are two modulator stages in the T5554 (see figure 4) whose mode can be selected using the appropriate bits in block 0 (MS1[1:0] and MS[2:0]). Also the bitrate can be selected using BR[2:0] in block 0. These options are described in detail in figures 21 through 26.

Answer-On-Request Mode (AOR)

When the AOR bit is set, the IDIC does not start modulation after loading configuration block 0. It waits for a valid AOR data stream (wake-up command) from the reader before modulation is enabled.

The wake-up command consists of the OP-code (“10”) following by a valid password. The IC will remain active until the RF field is turned off or a stop OP-code is received.

Table 1. T5554 - Modes of Operation

PWD	AOR	STOP	Behavior of Tag after Reset/POR	STOP Function
1	1	0	Anticollision mode: Modulation starts after wake-up with a matching PWD • Programming needs valid PWD • AOR allows programing with read protection (no read after write)	STOP OP-code (“11”) defeats modulation until RF field is turned off
1	0	0	Password mode: • Modulation starts after reset • Programming needs valid PWD	
0	1	0	• Modulation starts after wake-up command • Programming with modulation defeat without previous wake-up possible • AOR allows programing with read protection (no read after write)	
0	0	0	Plain/Normal mode: • Modulation starts after reset • Direct access command • Programming without password	
x	0	1	See corresponding modes above	STOP OP-code ignored, modulation continues until RF field is turned off

Figure 12. Answer-on-request (AOR) Mode

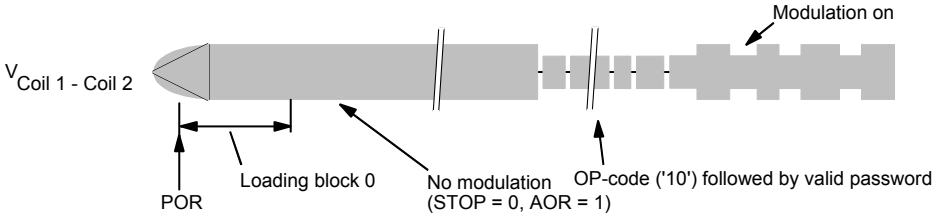


Figure 13. Anticollision Procedure Using AOR Mode

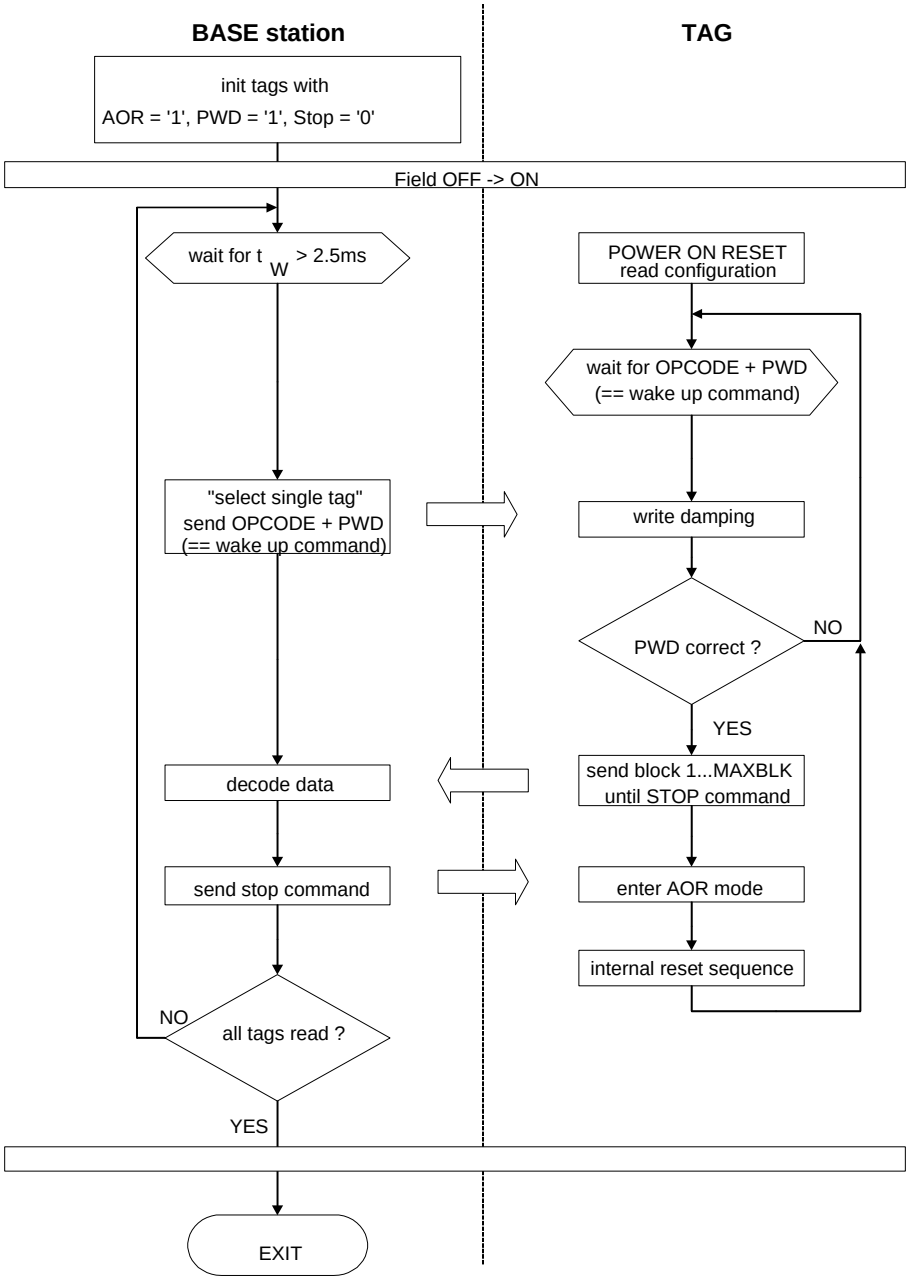


Figure 14. Signals During Writing

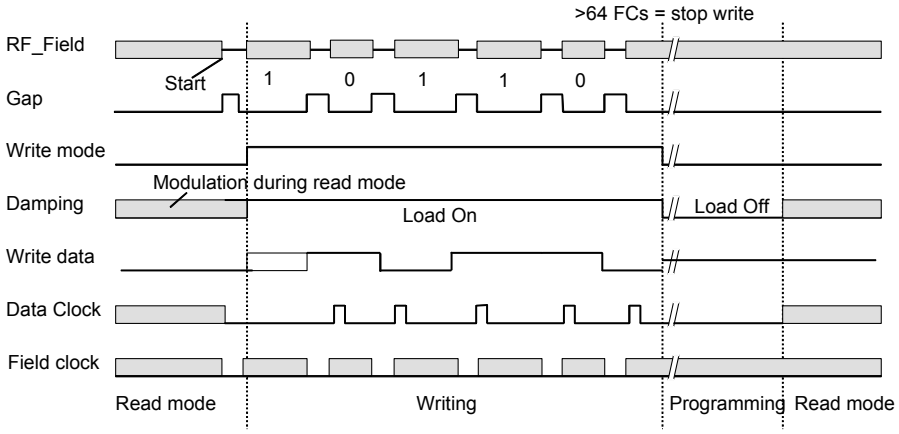


Figure 15. Write Data Decoding Schemes

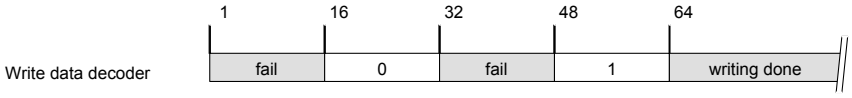
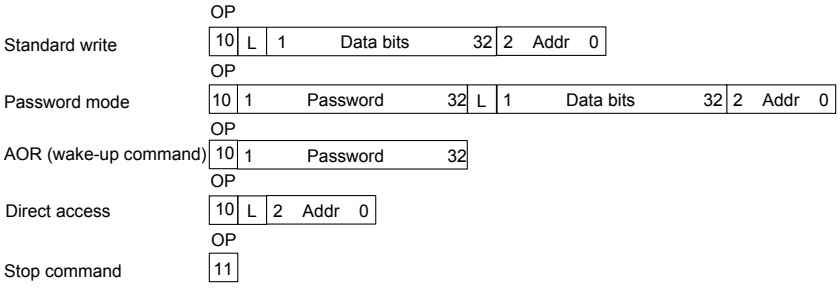


Figure 16. T5554 – OP-code Formats



Write

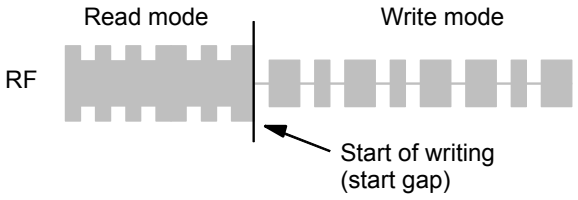
Writing data into the IC occurs via the Atmel write method. It is based on interrupting the RF field with short gaps. The time between two gaps encodes the “0/1” information to be transmitted.

Start Gap

The first gap is the start gap which triggers write mode. In write mode, the damping is permanently enabled which eases gap detection. The start gap may need to be longer than subsequent gaps in order to be detected reliably.

A start gap will be detected at any time after block 0 has been read (field-on plus approximately 2 ms).

Figure 17. Start of Writing



Decoder

The duration of the gaps is usually 50 to 150 µs. The time between two gaps is nominally 24 field clocks for a “0” and 56 field clocks for a “1”. When there is no gap for more than 64 field clocks after previous gap, the IDIC exits write mode; it starts with programming if the correct number of valid bits were received.

If there is a gap fail - i.e., one or more of the intervals did represent not a valid “0” or “1” - the IC does not program, but enters read mode beginning with block 1, bit 1.

Writing Data into the T5554

The T5554 expects a 2-bit OP-code first. There are two valid OP-codes (“10” and “11”). If the OP-code is invalid, the T5554 starts read mode beginning with block 1 after the last gap. The OP-code (“10”) is followed by different information (see figure 17):

- Standard writing needs the OP-code, the lock bit, the 32 data bits and the 3-bit block address.
- Writing with usePWD set requires a valid password between OP-code and address/data bits.
- In AOR mode with usePWD, OP-code and a valid password are necessary to enable modulation.
- The STOP OP-code is used to silence the T5554 (disable damping until power is cycled).

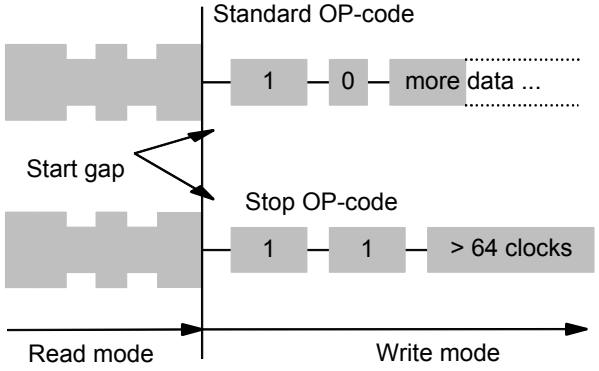
Note: The data bits are read in the same order as written.

STOP OP-code

The STOP OP-code (“11”) is used to disable the modulation until a power-on reset occurs. This feature can be used to have a steady RF field where single transponders are collected one by one. Each IC is read and than disabled, so that it does not interfere with the next IC.

Note: The STOP OP-code should contain only the two OP-code bits to disable the IC. Any additional data sent will not be ignored, and the IC will not stop modulation.

Figure 18. OP-code Transmission



Password

When password mode is on (usePWD = 1), the first 32 bits after the OP-code are regarded as the password. They are compared bit-by-bit with the contents of block 7, starting at bit 1. If the comparison fails, the IC will not program the memory, but restart in read mode at block 1 once writing has completed.

Notes:
1) If PWD is not set, but the IC receives a write datastream containing any 32 bits in place of a password, the IC will enter programming mode.
2) In password mode, MAXBLK should be set to a value below 7 to prevent the password from being transmitted by
3) Every transmission of 2 OP-code bits, 32 password bits, one lock bit, 32 data bits and 3 address bits (= 70 bits) needs about 35 ms. Testing all 232 possible combinations (about 4.3 billion) takes about 40,000 h, or over four years. This is a sufficient password protection for a general-purpose IDIC.

Programming

When all necessary information has been written to the T5554, programming may proceed. There is a 32-clock delay between the end of writing and the start of programming. During this time, Vpp - the EEPROM programming voltage - is measured and the lock bit for the block to be programmed is examined. Furthermore, Vpp is continually monitored throughout the programming cycle. If at any time Vpp is too low, the chip enters read mode immediately.

The programming time is 16 ms.

After programming is done, the T5554 enters read mode, starting with the block just programmed. If either block or sequence terminators are enabled, the block is preceded by a block terminator. If the mode register (block 0) has been reprogrammed, the new mode will be activated after the just-programmed block has been transmitted using the previous mode.

Figure 19. Programming

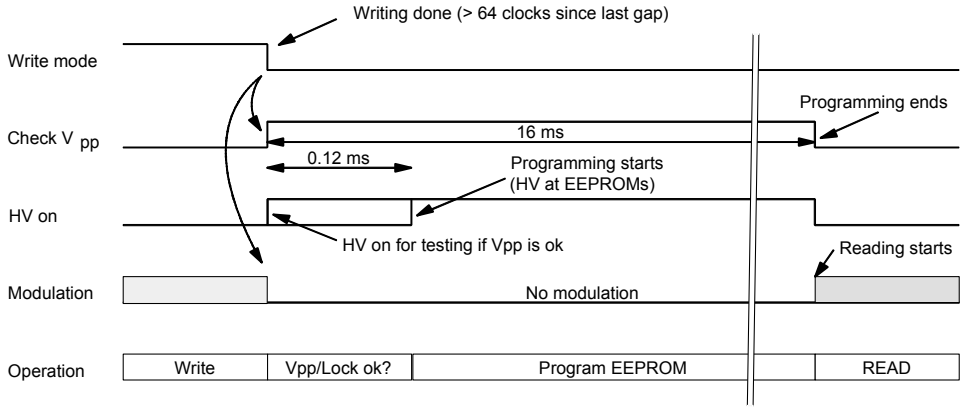
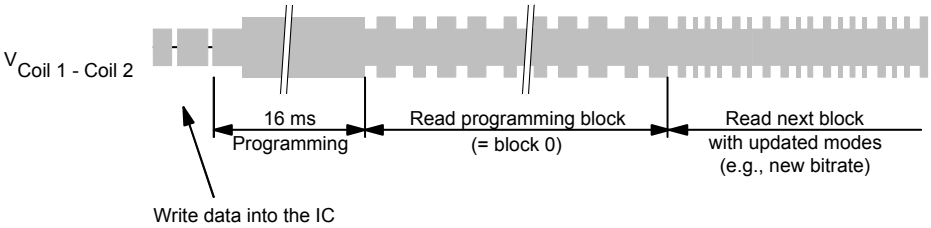


Figure 20. Coil Voltage after Programming of Block 0



Error Handling

Several error conditions can be detected to ensure that only valid bits are programmed into the EEPROM. There are two error types which lead to different actions.

Errors During Writing

There are four detectable errors which could occur during writing data into the T5554:

- Wrong number of field clocks between two gaps
- The OP-code is neither the standard OP-code (’10‘) nor the stop OP-code (’11‘)
- Password mode is active but the password does not match the contents of block 7
- The number of bits received is incorrect; valid bit counts are
  - Standard write 38 bits (PWD not set)
  - Password write 70 bits (PWD set)
  - AOR wake-up 34 bits
  - Stop command 2 bits

If any of these four conditions are detected, the IC starts read mode immediately after leaving write mode. Reading starts with block 1.

Errors During Programming

If writing was successful, the following errors could prevent programming:

- The lock bit of the addressed block is set
- V_{PP} is too low

In these cases, programming stops immediately. The IC reverts to read mode, starting with the currently addressed block.

Figure 21. Functional Diagram of the T5554

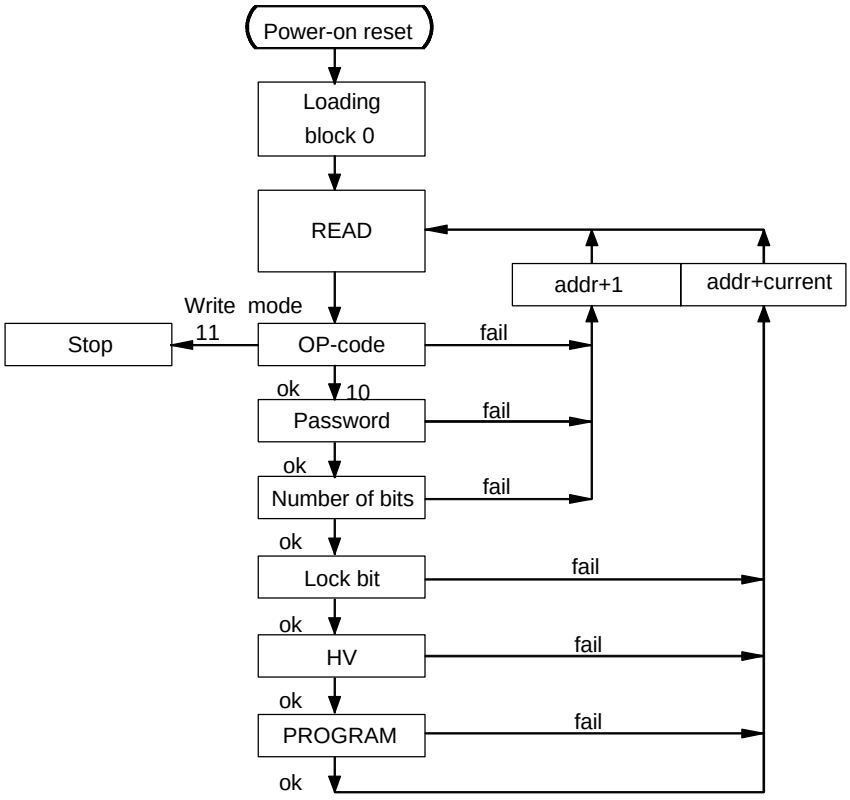


Figure 22. Example of Manchester Coding with Data Rate RF/16

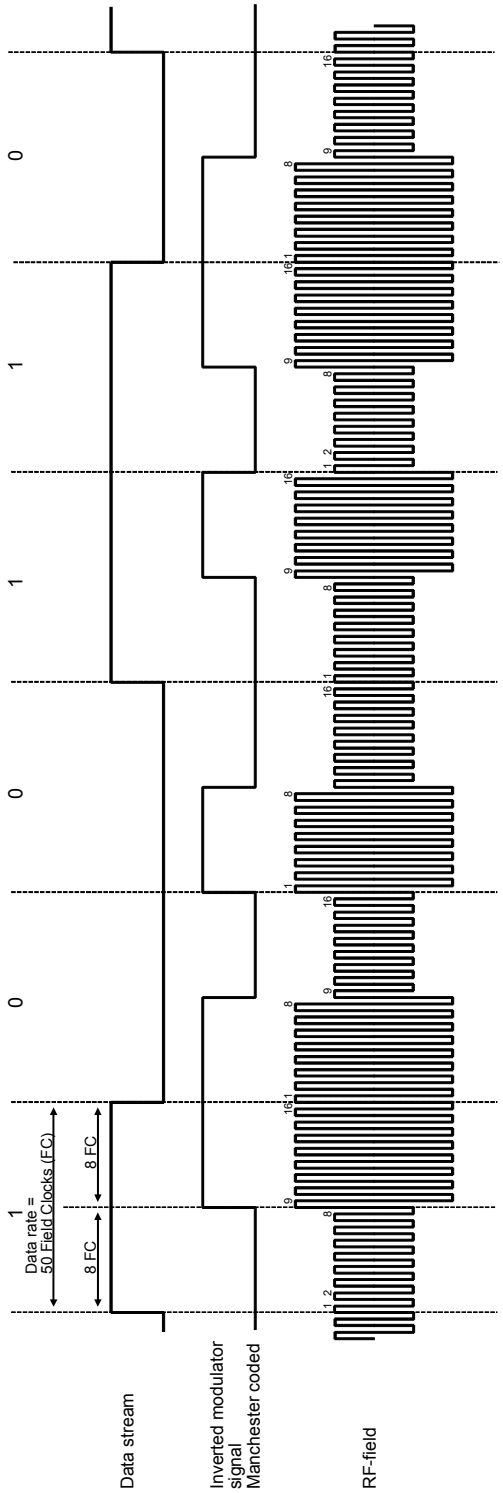


Figure 23. Example of Biphase Coding with Data Rate RF/16

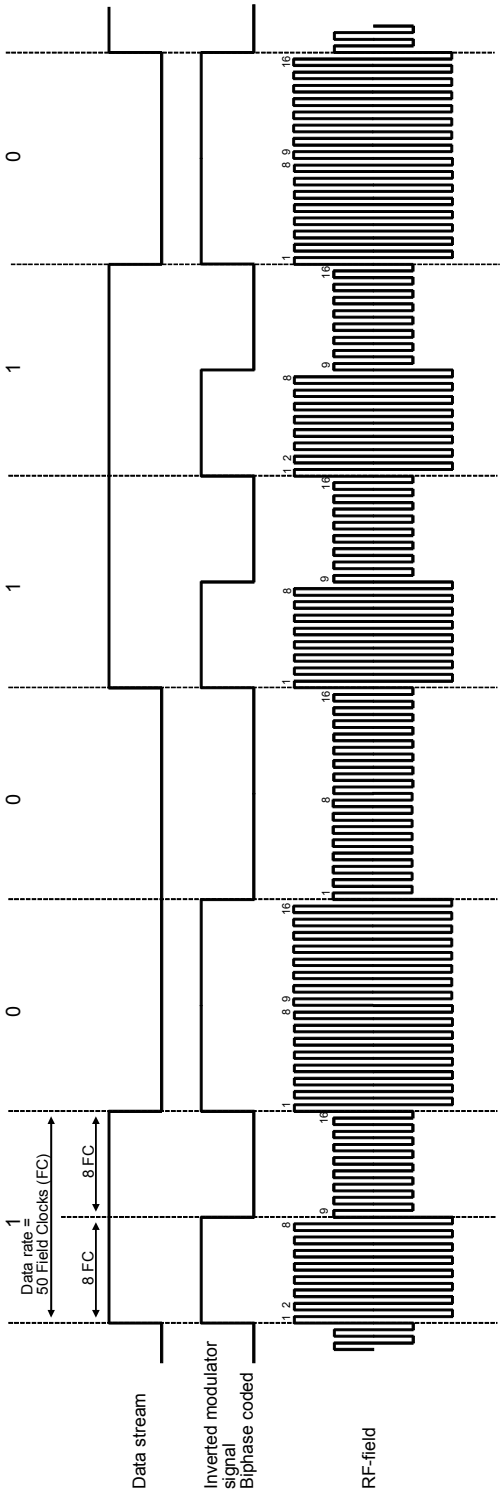


Figure 24. Example of FSK Coding with Data Rate RF/40 Subcarrier f_0 = RF/8, f_1 = RF/5,

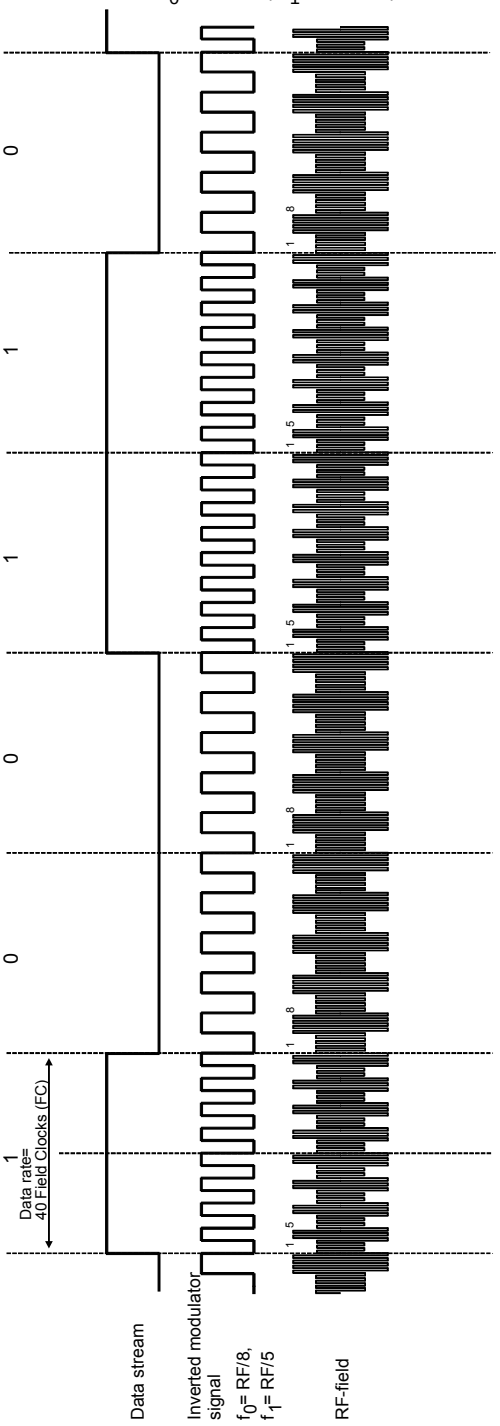


Figure 25. Example of PSK Coding with Data Rate RF/16

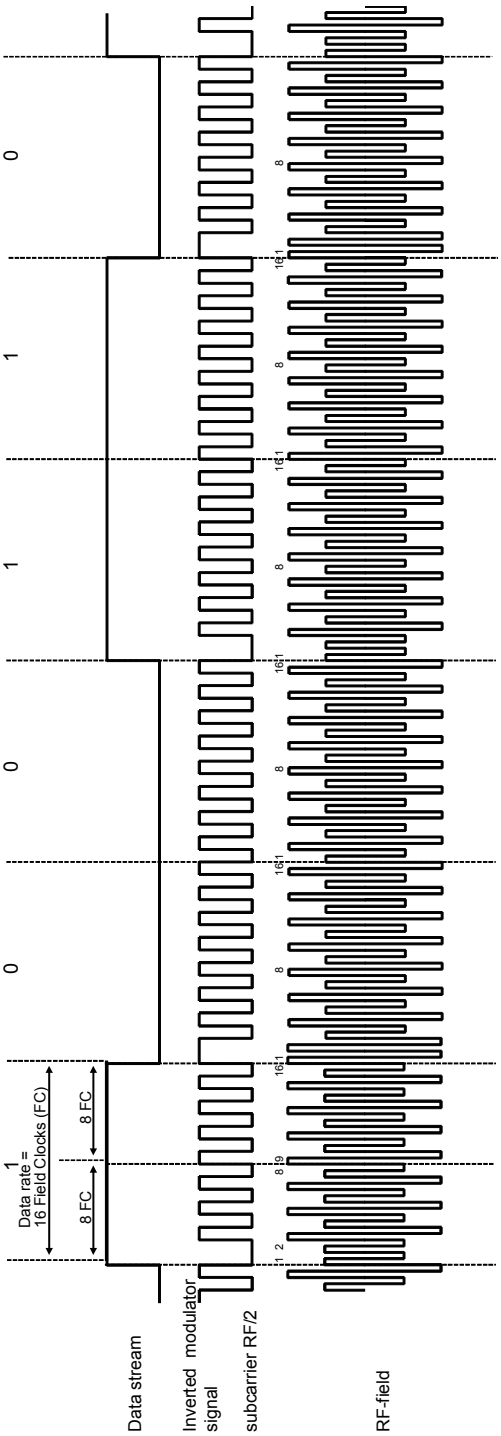


Figure 26. Example of PSK2 Coding with Data Rate RF/16

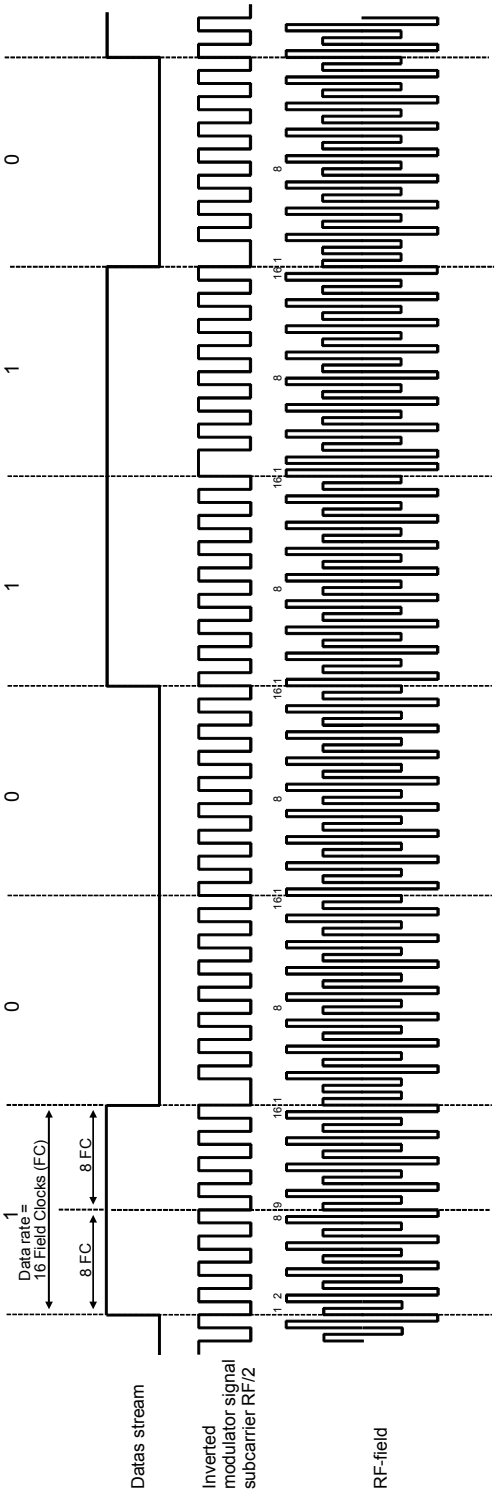


Figure 27. Example of PSK3 Coding with Data Rate RF/16

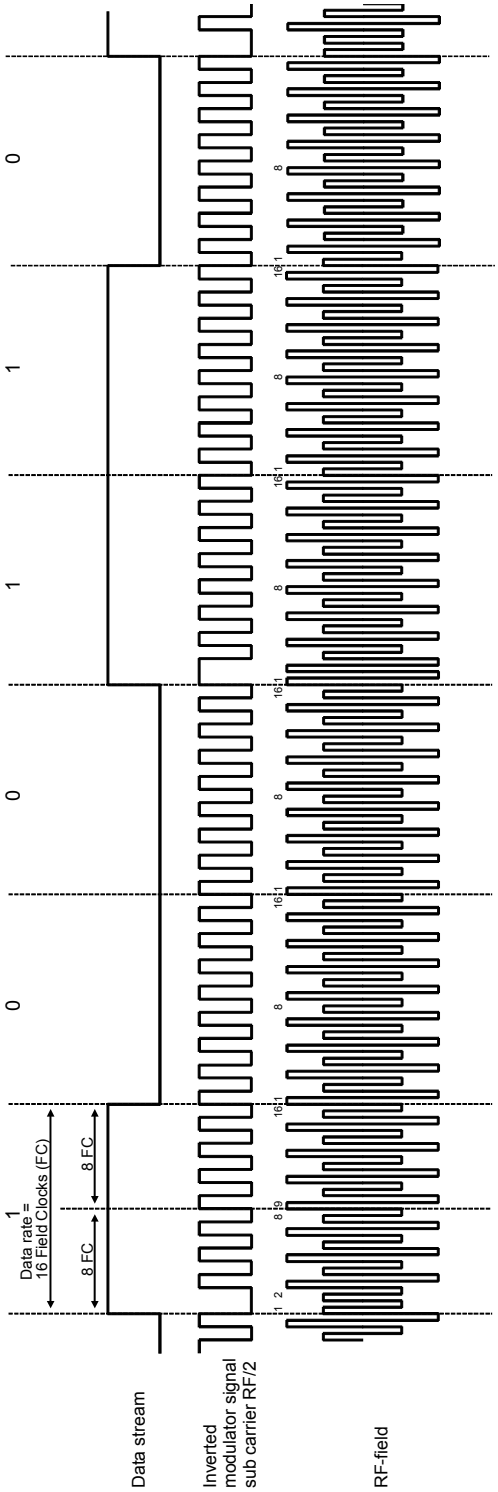


Figure 28. Measurement Setup for I_{DD}

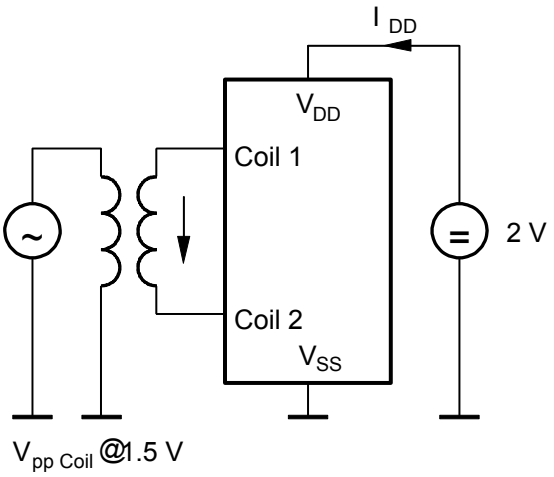
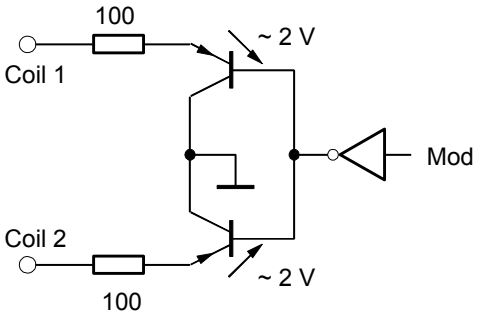
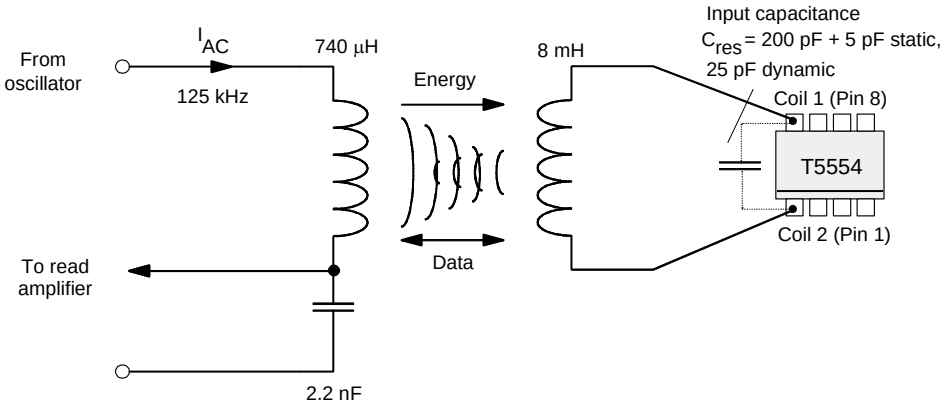


Figure 29. Simplified Damping Circuit



Application Example

Figure 30. Typical Application Circuit



Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Maximum DC current into Coil 1/Coil 2	I_{coil}	10	mA
Maximum AC current into Coil 1/Coil 2, f = 125 kHz	$I_{coil\ p}$	20	mA
Power dissipation (dice) (free-air condition, time of application: 1 s)	P_{tot}	100	mW
Electrostatic discharge maximum to MIL-Standard 883 C method 3015	V_{max}	2	kV
Operating ambient temperature range	T_{amb}	-40 to +85	°C
Storage temperature range (data retention reduced)	T_{stg}	-40 to +150	°C
Maximum assembly temperature for less than 5 min	T_{sld}	150	°C

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

Electrical Characteristics

T_{amb} = 25°C; f_{RF} = 125 kHz, reference terminal is V_{SS}

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
RF frequency range		f_{RF}	100	125	150	kHz
Supply current (see figure 28)	Read and write over the full temperature range	I_{DD}		5	7.5	µA
Supply current (see figure 28)	Programming over the full temperature range	I_{DD}		100	200	µA
Clamp voltage	10 mA current into Coil1/2	V_{cl}	9.5		11.5	V
Programming voltage	From on-chip HV-Generator	V_{pp}	16		20	V
Programming time		t_P		18		ms
Startup time		$t_{startup}$			4	ms
Data retention (1)		$t_{retention}$	10			Years
Programming cycles (1)		n_{cycle}	100,000			Cycles
Supply voltage	Read and write	V_{DD}			1.6	V
Supply voltage	Read-mode, T = -30°C	V_{DD}			2.0	V
Coil voltage	Read and write	$V_{coil\ pp}$			6.0	V
Coil voltage	Programming, RF field not damped	$V_{coil\ pp}$			10	V
Resonance capacitor		$C_{res(A)}$ (2)	63	70	77	pF
Resonance capacitor		$C_{res(B)}$ (2)	180	200	220	pF
Damping resistor		R_D		300		W

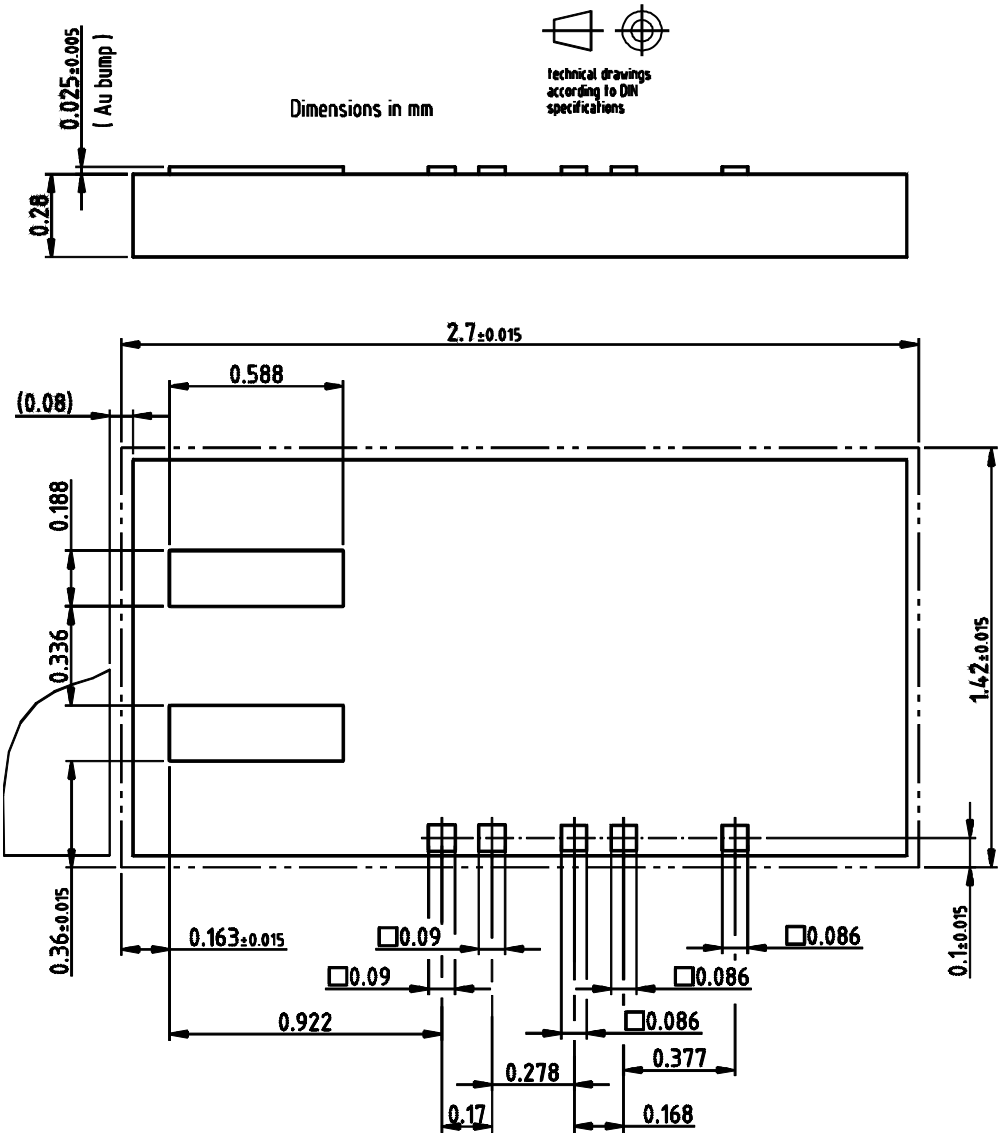
Notes: 1. Since EEPROM performance may be influenced by assembly and packaging, Atmel confirms the parameters for DOW (= die-on-wafer) and ICs assembled in standard package.
2. Tolerance/wafer ±4%; tolerance / lot ±5%; typical value selected by mask option

Ordering Information

Extended Type Number	Package	Remarks
T5554401-DBN	Au-bumped 25 µm chip on sticky	200 pF capacitor; default programming: all 0; EEPROM memory erased
T5554402-DBN		70 pF capacitor; default programming: all 0; EEPROM memory erased
T5554403-DBN	NiAu-bumped 15 µm chip on sticky	200 pF capacitor; default programming: all 0; EEPROM memory erased
T5554404-DBN		70 pF capacitor; default programming:all 0; EEPROM memory erased

Chip Dimensions

Figure 31. Chip Dimensions of T5554



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