Features

- **Excellent Power Added Efficiency**
- **1xRTT Compatible**
- **Industry Standard Digital Quiescent Current State Control**
- **Analog Continuous Bias Capability**
- **CMOS-compatible Logic Inputs**
- **High ACP and ALT**
- **Excellent RX Band Noise Performance**

Benefits

- **Extended Battery Operating Time**
- **Very Small 10 Pin 4 mm × 4 mm Package**
- **Few External Components**
- **Fully ESD Protected**

Applications

- **Cell Band CDMA IS-95/98 Based Mobile Phones**
- **Single-mode, Dual-mode and Tri-mode CDMA Phones**

Description

The T0372 is a 4 mm × 4 mm 3-V CDMA/AMPS cell-band power amplifier module designed for use in mobile phones. Its extremely small 4 mm × 4 mm package makes it ideal for today's very small data enable phones. The module supports the IS-95 and IS-98 standards and is also 1xRTT compliant. The T0372 provides excellent RF performance with low current consumption resulting in longer talk times in portable applications. The module has a small 4 mm × 4 mm footprint, which facilitates its use in the next generation of small, lightweight handsets and other wireless applications. The heart of the module is a two-stage power amplifier manufactured in Atmel's SiGe technology. The T0372 provides the capability to be operated digitally (one or two bias states), or in a continuous quiescent current mode. In two-state quiescent current mode operation, the T0372 is controlled by the baseband processor using a CMOS-compatible I_{CQ} control voltage. Overall current consumption of the device is minimized by selecting the lowest I_{CQ} state available for each power output level. The module is 50-Ω matched on the input and output, allowing the device to be used with minimal external circuitry.

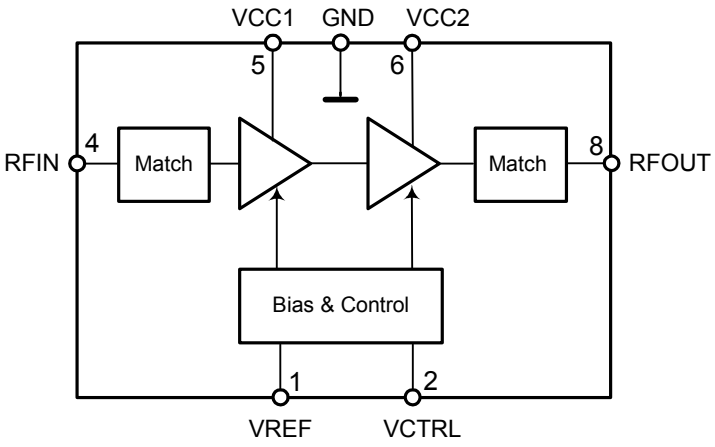
3-V CDMA/AMPS Power Amplifier Module 4 mm × 4 mm for Cell Band

T0372

Preliminary (Summary)

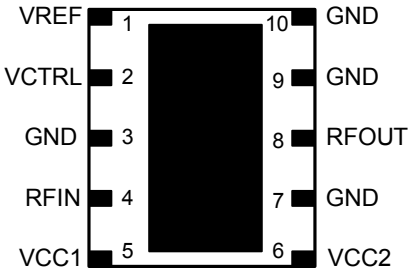
Rev. 4541AS–CDMA–08/02

Figure 1. Block Diagram



Pin Configuration

Figure 2. Pinning



Pin Description

Pin	Symbol	Function
1	VREF	Regulated supply for setting bias, reference voltage input
2	VCTRL	CMOS-compatible logic level used to set bias
3	GND	Ground recommended
4	RFIN	RF input, the RF circuit is DC-grounded internally, 50-Ω RF impedance
5	VCC1	Collector supply for input stage
6	VCC2	Collector supply for output stage
7	GND	Ground recommended
8	RFOUT	RF output, the RF circuit is DC-blocked internally, 50-Ω RF impedance
9	GND	Ground recommended
10	GND	Ground recommended
-	Paddle	Device ground and heat sink, requires good thermal path

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltages, no RF applied	V_{CC1}, V_{CC2}	-0.5 to +6.0	VDC
Supply voltages, RF applied	V_{CC1}, V_{CC2}	-0.5 to +5.0	VDC
Bias reference voltages and bias control voltages (Pins 3 and 4 respectively)	V_{REF}, V_{CTRL}	-0.5 to +5.0	VDC
Power dissipation	P_{DISS}	2.5	W
Case temperature, survival	T_C	-40 to +100	°C
Storage temperature	T_{stg}	-40 to +150	°C
DC-grounded RF input	RF_{IN}	0 to 0	VDC
DC-blocked RF output	RF_{OUT}	-20 to +20	VDC

Note: The part may not survive all maximum ratings applied simultaneously.

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	TBD	K/W

Electrical Characteristics

Test conditions: $V_{CC1, CC2}$ = 3.4 VDC, V_{REF} = 2.85 VDC, V_{CTRL} = 0.5 VDC, RF = 836 MHz, Tc = 25°C, P_{out} = 28 dBm, Minimum/maximum limits are at +25°C ambient temperature, unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
	Frequency		4, 8	f_o	824	836	849	MHz	A; D
	Output power		8	P_{out}		28		dBm	A
	Large signal gain	P_{out} = 28 dBm, V_{CTRL} = low	4, 8	G_{high}	26.0	29.0		dB	A
		P_{out} = 16 dBm, V_{CTRL} = high	4, 8	G_{low}	25.0	28.0		dB	A
	Gain variation versus temperature	-30°C to +85°C	4, 8			±1.4		dB	C
	Quiescent current (high-gain mode)	V_{CTRL} = low	1, 5, 6	$I_{CQ_}$hi		110		mA	A
	Quiescent current (low-gain mode)	V_{CTRL} = high	1, 5, 6	$I_{CQ_}$low		60		mA	A
	Current consumption	P_{out} = 28 dBm, V_{CTRL} = low	1, 5, 6	I_{cc}		503		mA	A
	Output power (low)	ACPR = -49 dBc, IS-95/98 standard, V_{CTRL} = high	8	P_{out}		16		dBm	B
	Power added efficiency	P_{out} = 28 dBm V_{CTRL} = low		PAE	33	36		%	A
	Adjacent channel power	P_{out} = 28 dBm, IS-95/98 standard, V_{CTRL} = low	8	ACP		-49	-44	dBc	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics (Continued)

Test conditions: $V_{CC1, CC2}$ = 3.4 VDC, V_{REF} = 2.85 VDC, V_{CTRL} = 0.5 VDC, RF = 836 MHz, Tc = 25°C, P_{out} = 28 dBm, Minimum/maximum limits are at +25°C ambient temperature, unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
	Alternate channel power	P_{out} = 28 dBm, IS-95/98 standard, V_{CTRL} = low	8	ALT		-57	-55	dBc	A
	Noise power in Rx band	P_{out} = 28 dBm, IS-95/98 standard, V_{CTRL} = low	8			-94		dBm/ 30 kHz	C
	RF input return loss	P_{out} = 28 dBm, V_{CTRL} = low	4	S_{11}		11.5		dB	A
	Second harmonic	P_{out} = 28 dBm, IS-95/98 standard, V_{CTRL} = low	8	2fo		-35		dBc	A
	Third harmonic	P_{out} = 28 dBm, IS-95/98 standard, V_{CTRL} = low	8	3fo		-45		dBc	A
	Supply voltage		5, 6	V_{CC}	3.1	3.4	4.2	VDC	D
	Reference voltage	For 1 or 2 bias state operation	1	V_{REF}	2.8	2.85	3.0	VDC	D
	Reference current	V_{CTRL} = low	1	I_{B_high}		10		mA	A
		V_{CTRL} = high	1	I_{B_low}		5		mA	A
	Leakage current	V_{CTRL} = high; V_{REF} = 0 VDC	5, 6			10		µA	A
	Logic current	At V_{CTRL}	2	I_{CTRL}		49	100	µA	A
	Control voltage	High Low	2	V_{CTRL}	1.7 0	2.0 0.25	4.5 0.5	VDC VDC	D
	Ruggedness	No damage, P_{OUT} = 28 dBm, IS-95/98 standard, $V_{CC1, CC2}$ = high	8				10:1		C
	Stability	No oscillations, P_{OUT} = 28 dBm, IS-95/98 standard, $V_{CC1, CC2}$ = high	8				10:1		C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics (AMPS Mode)

Test conditions: $V_{CC1, CC2}$ = 3.4 VDC, V_{REF} = 2.85 VDC, V_{CTRL} = 0.5 VDC, RF = 836 MHz, Tc = 25°C, P_{out} = 31.5 dBm, Minimum/maximum limits are at +25°C ambient temperature, unless otherwise specified

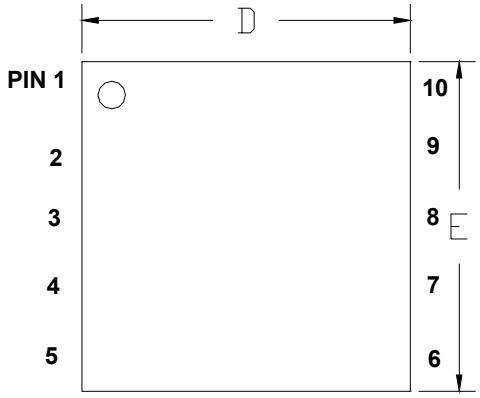
No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
	Frequency		4, 8	f_o	824	836	849	MHz	A, D
	Output power	Saturated, P_{IN} = 3.5 dBm	8	P_{out}		31.5		dBm	A
	Large signal gain	P_{out} = 31.5 dBm	4, 8	$I_{CQ_}$hi	24.5	27.0		dB	A
	Power added efficiency	P_{out} = 31.5 dBm		PAE	47	51		%	A
	Noise power in Rx band	P_{out} = 31.5 dBm	8			-93		dBm/ 30 kHz	C
	RF input return loss	All operating P_{out} and V_{CC}	4	S_{11}		11.5		dB	A
	Second harmonic	P_{out} = 31.5 dBm	8	2fo		-32.5		dBc	A
	Third harmonic	P_{out} = 31.5 dBm	8	3fo		-42.5		dBc	A
	Current consumption	P_{out} = 31.5 dBm	1, 5, 6	I_{CC}		783		mA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

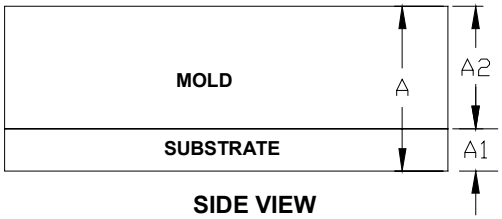
Ordering Information

Extended Type Number	Package	Remarks
T0372	4 mm × 4 mm module package	-

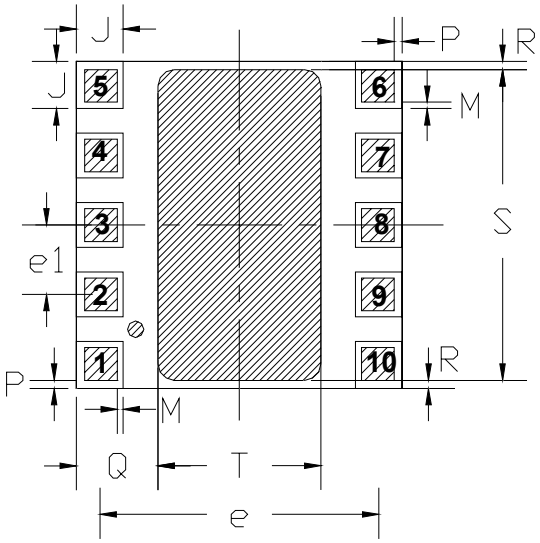
Package Information



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Designation	Description	Dimensions
A	Overall height	1.06 ± 0.09 mm
A1	Substrate thickness	0.38 ± 0.05 mm
A2	Mold thickness	0.68 ± 0.05 mm
D	Package length	4.0 ± 0.1 mm
E	Package width	4.0 ± 0.1 mm
J	Terminal solder mask opening length and width (for all terminals)	0.575 ± 0.075 mm
M	Distance between metal pad and solder mask	0.075 ± 0.05 mm
P	Distance between metal pad and package edge	0.10 ± 0.025 mm
T	GND solder mask opening width	2.00 ± 0.05 mm
S	GND solder mask opening length	3.80 ± 0.05 mm
R	Distance between GND solder mask opening and package edge	0.10 ± 0.01 mm
Q	Distance between GND solder mask opening and package edge	1.00 ± 0.01 mm
e	Terminal pitch for terminals 1-10, 2-9, 3-8, 4-7 and 5-6	3.400 mm
e1	Terminal pitch for terminals 1-2-3-4-5 and 6-7-8-9-10	0.850 mm

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