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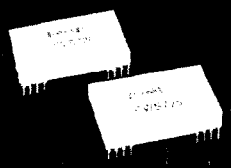

PWS725A
PWS726A

Isolated, Unregulated DC/DC CONVERTERS

FEATURES

- ISOLATED ±7 TO ±18VDC OUTPUT FROM SINGLE 7 TO 18VDC SUPPLY
- ±15mA OUTPUT AT RATED VOLTAGE ACCURACY
- HIGH ISOLATION VOLTAGE
  PWS725A, 1500Vrms
  PWS726A, 3500Vrms
- LOW LEAKAGE CAPACITANCE: 9pF
- LOW LEAKAGE CURRENT: 2μA max, at 240VAC 50/60Hz
- HIGH RELIABILITY DESIGN
- AVAILABLE WITH OUTPUT SYNCHRONIZATION SIGNAL FOR USE WITH ISO120 AND ISO121
- PROTECTED AGAINST OUTPUT FAULTS
- COMPACT
- LOW COST
- EASY TO APPLY—FEW EXTERNAL PARTS

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS EQUIPMENT
- TEST EQUIPMENT
- DATA ACQUISITION

DESCRIPTION

The PWS725A and PWS726A convert a single 7 to 18VDC input to bipolar voltages of the same value as the input voltage. The converters are capable of providing ±15mA at rated voltage accuracy and up to ±40mA without damage. (See Output Current Rating.)

The PWS725A and PWS726A converters provide reliable, engineered solutions where isolated power is required in critical applications. The high isolation voltage rating is achieved through use of a specially-designed transformer and physical spacing. An additional high dielectric-strength, low leakage transformer coating increases the isolation rating of the PWS726A.

Reliability and performance are designed in. The bifilar wound, wirebonded transformer simultaneously provides lower output ripple than competing designs, and a higher performance/cost ratio. The soft-start oscillator/driver design assures full operation of the oscillator before either MOSFET driver turns on, protects the switches, and eliminates high inrush currents during turn-on. Input current sensing protects both the converter and the load from possible thermal damage during a fault condition.

Special design features make these converters especially easy to apply. The compact size allows dense circuit layout while maintaining critical isolation requirements. The Input Sync connection allows frequency synchronization of multiple converters. The Output Sync is available to synchronize ISO120 and ISO121 isolation amplifiers. The Enable input allows control over output power in instances where shutdown is desired to conserve power, such as in battery-powered equipment, or where sequencing of power turn-on/turn-off is desired.

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SPECIFICATIONS

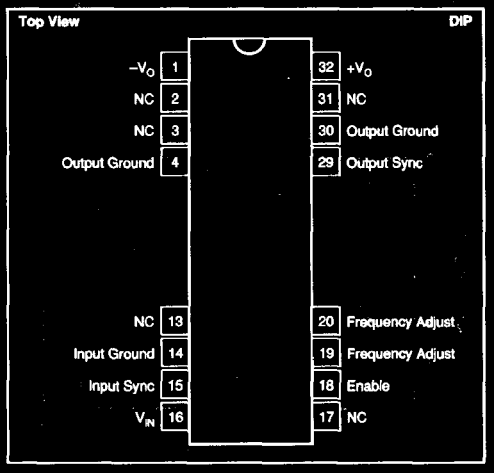
ELECTRICAL

T_A = +25°C, C_L = 1µF ceramic, V_{IN} = 15VDC, operating frequency = 800kHz, V_{OUT} = ±15VDC, C_{IN} = 1µF ceramic, I_{OUT} = ±15mA, unless otherwise specified.

PARAMETER	CONDITIONS	PWS725A MIN	PWS725A TYP	PWS725A MAX	PSW726A MIN	PSW726A TYP	PSW726A MAX	UNITS
INPUT								
Rated Voltage			15			*		VDC
Input Voltage Range		7		18	*		*	VDC
Input Current	I_O = ±15mA		77			*		mA
Input Current Ripple	No External Filtering		150			*		mAp-p
	L-C Input Filter, L_{IN} = 100µH, C_{IN} = 1µF(1)		5			*		mAp-p
	C Only, C_{IN} = 1µF		60					mAp-p
ISOLATION								
Test Voltages	Input to Output, 10 seconds	4000			8000			VDC
	Input to Output, 60 seconds, min	1500			3500			Vrms
Rated Voltage	Input to Output, Continuous, AC 60Hz			1500			3500	Vrms
	Input to Output, Continuous DC			2121			4950	VDC
Isolation Impedance	Input to Output		10^{12} || 9			*		Ω || pF
Leakage Current	Input to Output, 240Vrms, 60Hz		1.2	2.0		*	*	µA
OUTPUT								
Rated Output Voltage		14.25	15	15.75	*	*	*	VDC
Output Current	Balanced Loads		15	40		*	*	mA
	Single-Ended			80			*	mA
Load Regulation	Balanced Loads, ±10mA < I_{OUT} < ±40mA			0.4			*	%/mA
Ripple Voltage (400kHz)	No External Capacitor		60			*		mVp-p
	L_O = 10µH, C_O = 1µF (Figure 1)		10			*		mVp-p
	L_O = 0µH, C_O Filter Only			See Performance Curves				
Output Switching Noise	L_O = 10µH, C_O = 1µF		1			*		mVp-p
Output Capacitive Load	L_O = 100µH, C Filter			10			*	µF
	C Filter Only			1			*	µF
Voltage Balance, V+, V–			0.04					%
Sensitivity to ΔV_{IN}			1.15					V/V
Output Voltage Temp. Coefficient			10					mV/°C
Output Sync Signal	Square Wave, 50% Duty Cycle		30			*		Vp-p
TEMPERATURE								
Specification		–25		+85	*		*	°C
Operating		–25		+85	*		*	°C
Storage		–25		+125	*		*	°C

* Specification same as PWS725A.

PIN CONFIGURATION



PACKAGE INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PWS725A	32-Pin Ceramic DIP	210
PWS726A	32-Pin Ceramic DIP	210

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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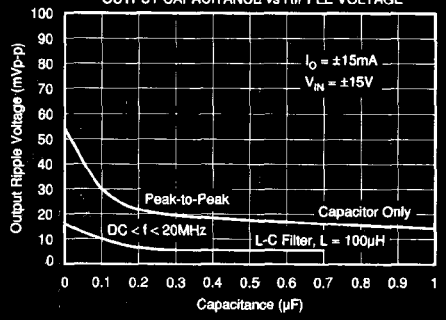
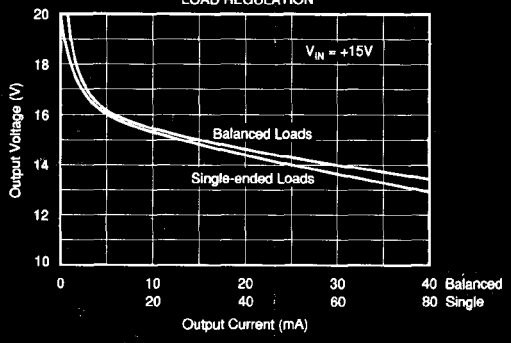
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

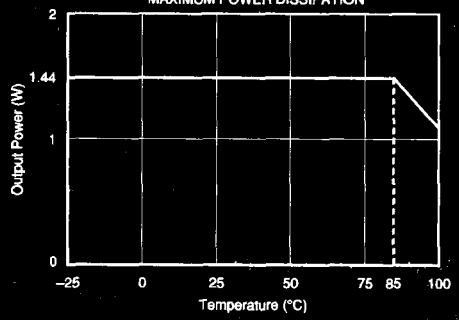
OUTPUT CAPACITANCE vs RIPPLE VOLTAGE



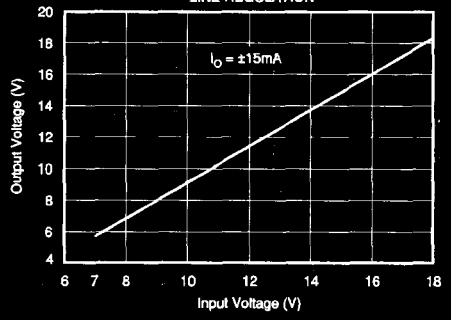
LOAD REGULATION



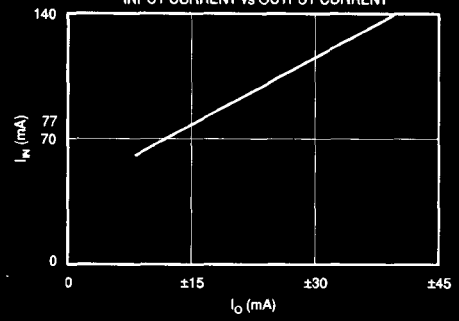
MAXIMUM POWER DISSIPATION



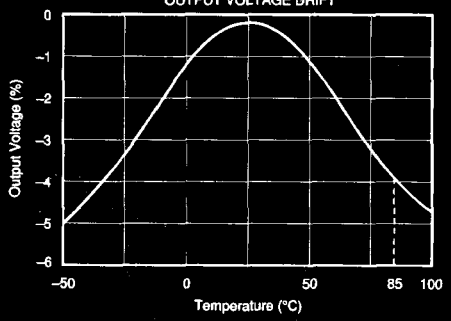
LINE REGULATION



INPUT CURRENT vs OUTPUT CURRENT

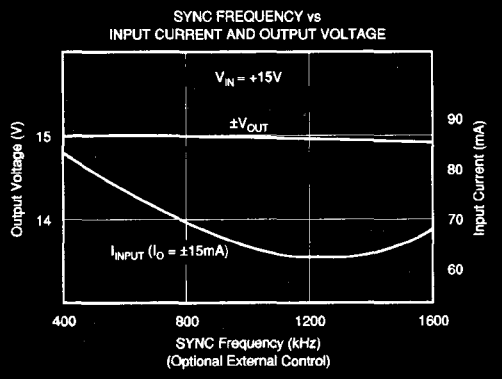


OUTPUT VOLTAGE DRIFT



TYPICAL PERFORMANCE CURVES (CONT)

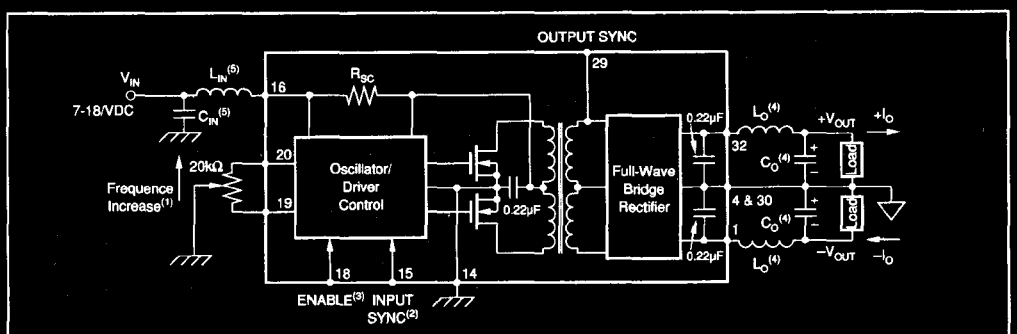
T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.



THEORY OF OPERATION

The PWS725A and the PWS726A DC/DC converters consist of a free-running oscillator, control and switch driver circuitry, MOSFET switches, a transformer, a bridge rectifier, and filter capacitors together in a 32-pin DIP (0.900 inches nominal) package. The control circuitry consists of current limiting, soft start, frequency adjust, enable, and synchronization features. See Figure 1. In instances where several converters are used in a system, beat frequencies developed between the converters are a potential source of low frequency noise in the supply and ground paths. This noise may couple into signal paths. See Figures 2 and 3 for connection of INPUT SYNC pin. Converters can be synchronized and these beat frequencies avoided. The unit with the highest natural frequency will determine the synchronized running frequency. To avoid excess stray capacitance, the INPUT SYNC pin should not be loaded with more than 50pF. If unused, the INPUT SYNC must be left open.

Soft start circuitry protects the MOSFET switches during start up. This is accomplished by holding the gate-to-source voltage of both MOSFET switches low until the free-running oscillator is fully operational. In addition to that soft start circuitry, input current sensing also protects the MOSFET switches. This current limiting keeps the FET



NOTES: (1) Frequency Adjust is optional, with pins 19 and 20 left open. The normal switching frequency is 800kHz.
(2) Leave INPUT SYNC pin open if unused; limit stray capacitance on INPUT SYNC pin to less than 50pF.
(3) Leave ENABLE pin open or connect to V_{IN} if not used.
(4) Optional output filtering, with L_O = 0, limit C_O ≤ 1µF, with L_O = 100µH, limit C_O ≤ 10µF, see Performance Curves for L_O = 0.
(5) Optional input filtering, see Performance Curves for L_{IN} = 0.
(6) CAUTION: Do not connect pin 29 to low impedance loads. See Figure 5.

FIGURE 1. PWS725A/726A Functional Diagram.

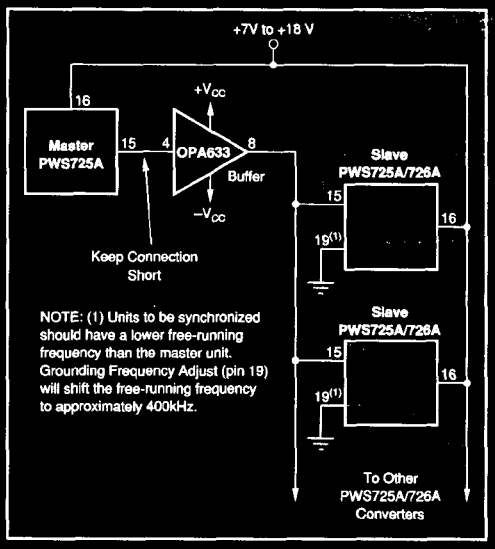


FIGURE 2. Synchronization of Multiple PWS725As or PWS726As from a Master Converter.

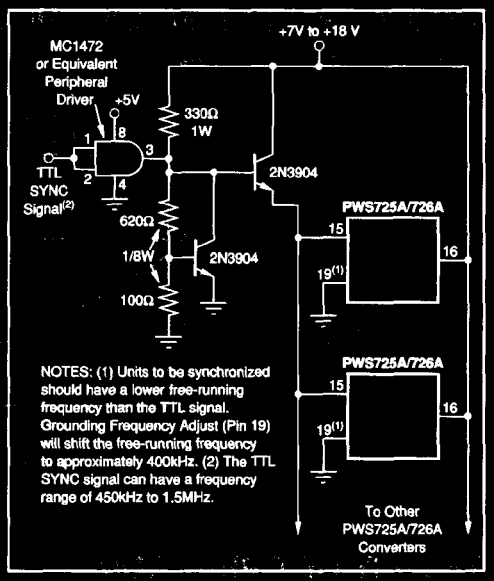


FIGURE 3. Synchronization of Multiple PWS725As or PWS726As from an External TTL Signal.

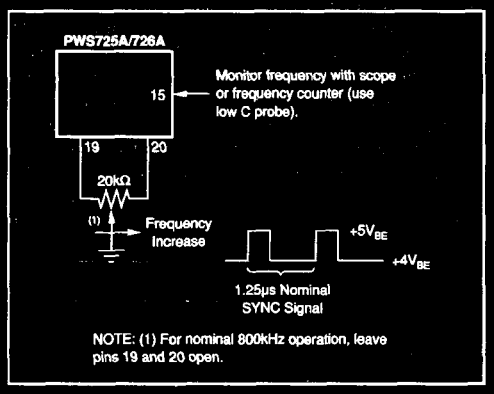


FIGURE 4. Frequency Adjustment Procedure.

switches operating in their safe operating area under fault conditions or excessive loads. When either of these conditions occur, the peak input current exceeds a safe limit. The result is an approximate 5% duty cycle, 300µs drive period to the MOSFET switches. This protects the internal MOSFET switches as well as the external load from any thermal damage. When the fault or excessive load is removed, the converter resumes normal operation. A delay period of approximately 50µs incorporated in the current sensing circuitry allows the output filter capacitors to fully charge after a fault is removed. This delay period corresponds to a filter capacitance of no more than 1µF at either of the output pins. This provides full protection of the MOSFET switches and also sufficiently filters the output ripple voltage (see specification table). The current sensing circuitry is designed to provide thermal protection for the MOSFET switches over the operating temperature range as well. The low thermal resistance for the package (θ_{JC} = 10°C/W) ensures safe operation under rated conditions. When these rated conditions are exceeded, the unit will go into its shutdown mode.

An optional potentiometer can be connected between the two FREQUENCY ADJUST pins to trim the oscillator operating frequency ±10% (see Figure 4). Care should be taken when trimming the frequency near the low frequency range. If the frequency is trimmed too low, the peak inductive currents in the primary will trip the input current sensing circuitry to protect the MOSFET switches from these peak inductive currents.

The ENABLE pin allows external control of output power. When this pin is pulled low, output power is disabled. Logic thresholds are TTL compatible. When not used, the Enable input may be left open or tied to V_{IN} (pin 16).

OUTPUT CURRENT RATING

The total current which can be drawn from the PWS725A or PWS726A is a function of total power being drawn from both outputs (see Functional Diagram). If one output is not used, then maximum current can be drawn from the other output. If both outputs are loaded, the total current must be limited such that:

$$|I_L+| + |I_L-| \leq 80mA$$

It should be noted that many analog circuit functions do not simultaneously draw full rated current from both the positive and negatives supplies. For example, an operational amplifier may draw 13mA from the positive supply under

full load while drawing only 3mA from the negative supply. Under these conditions, the PWS725A/726A could supply power for up to five devices (80mA + 16mA ≈ 5). Thus, the PWS725A/726A can power more circuits than is at first apparent.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter period of time. The relationship between actual test conditions and the continuous derated maximum specification is an important one. Burr-Brown has chosen a deliberately conservative one: VDC_{TEST} = (2 X $VACrms_{CONTINUOUS\ RATING}$) + 1000V for ten seconds. This choice is appropriate for conditions where system transient voltages are not well defined.(1) Where the real voltages are well-defined or where the isolation voltage is not continuous, the user may choose a less conservative derating to establish a specification from the test voltage.

NOTE: (1) Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS I-109 and ICS I-111.

OUTPUT SYNC SIGNAL

To allow synchronization of an ISO120 or ISO121 isolation amplifier, the PWS725A and PWS726A have an OUTPUT SYNC signal at pin 29. It should be connected as shown in Figure 5 to keep capacitive loading of pin 29 to a minimum. If output sync is not used, leave pin open.

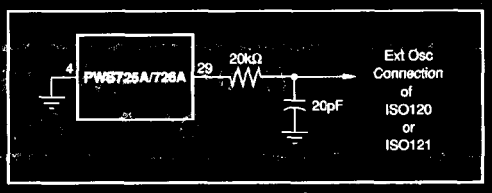


FIGURE 5. Synchronization with ISO120 or ISO121 Isolation Amplifier.