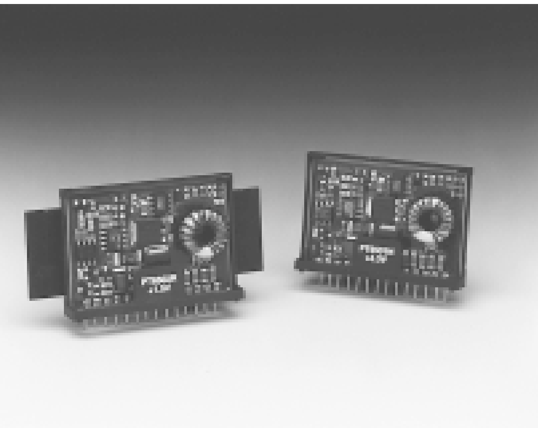
PT6500 Series

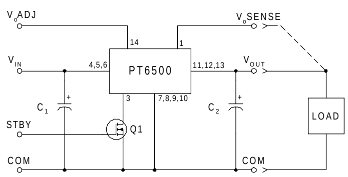
8 Amp 5V/3.3V Input Adjustable ISR with Short-Circuit Protection



- 8A Single Device Power
- Up to 90% efficiency (PT6501)
- Small SIP Footprint
- Standby Function
- Internal Short Circuit Protection
- Over-Temperature Protection
- Adjustable Output Voltage

The PT6500 series is a high performance +3.1 to 6V input, 8 Amp, 14-Pin SIP (Single In-line-Package) Integrated Switching Regulator (ISR). This ISR allows the integration of high-speed, low-voltage Pentium processors and their support logic into existing 3.3V or 5V systems without redesigning the central power supply. The PT6502 (1.5V) provides the low terminating voltages required by BTL/Futurebus+, CTT, HP, and GTL Buses from existing 3.3V or 5V power rails.

Standard Application



C_1 = Required 330µF electrolytic *
C_2 = Required 330µF electrolytic *
* See footnotes

Pin-Out Information

Pin	Function
1	Remote Sense
2	Do not connect
3	STBY*-Standby
4	V_{in}
5	V_{in}
6	V_{in}
7	GND
8	GND
9	GND
10	GND
11	V_{out}
12	V_{out}
13	V_{out}
14	V_{out} Adjust

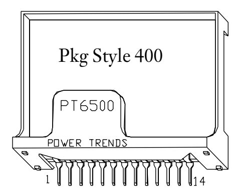
Ordering Information

PT6501□ = 3.3 Volts
† **PT6502□** = 1.5 Volts
PT6503□ = 2.5 Volts
PT6504□ = 3.6 Volts
† **PT6505□** = 1.2 Volts
† **PT6506□** = 1.8 Volts
† **PT6507□** = 1.3 Volts
† **PT6508□** = 1.7 Volts

†3.3V Input Bus Capable

PT Series Suffix (PT1234X)

Case/Pin Configuration	Heat Tab Configuration *None*	*Side*
Vertical Through-Hole	N	R
Horizontal Through-Hole	A	G
Horizontal Surface Mount	C	B



Specifications

Characteristics (T_a=25°C unless noted)	Symbols	Conditions		PT6500 SERIES Min	Typ	Max	Units
Output Current	I_o	Over V_{in} range		0.1 (1)	—	8.0	A
Current Limit	I_{cl}	V_{in}=+5V		—	13.0	20.0	A
Short Circuit Current	I_{sc}	V_{in}=+5V		—	15.0	—	Apk
Input Voltage Range	V_{in}	$0.1 \leq I_o \leq 8.0A$	V_o=2.5V and 3.3V $V_o \leq 1.8V$ V_o=3.6V	4.5 3.1 4.8	— — —	6 6 6	V
Output Voltage Tolerance	ΔV_o	V_{in} = +5V, I_o = 8.0A T_a = 0 to +70°C		V_o-0.1	—	V_o+0.1	V
Line Regulation	Reg_{line}	$4.5V \leq V_{in} \leq 6.0V$, I_o = 8.0A $3.1V \leq V_{in} \leq 6.0V$, I_o = 8.0A $4.5V \leq V_{in} \leq 6.0V$, I_o = 8.0A	$V_o \geq 3.3V$ $V_o \leq 1.8V$ V_o =2.5V	— —	±7 ±3 ±7	±17 ±8 ±13	mV
Load Regulation	Reg_{load}	$0.1 \leq I_o \leq 8.0A$, V_{in} = +5V	$V_o \geq 3.3V$ $V_o \leq 1.8V$ V_o =2.5V	— —	±17 ±12 ±13	±33 ±23 ±25	mV
V_o Ripple/Noise	V_n	V_{in} = +5V, I_o = 8.0 Amp		—	50	—	mVpp
Transient Response with C_o = 330µF	t_{tr} V_{os}	I_o step from 4A to 8.0A V_o over/undershoot		— —	100 150	— —	µsec mV
Efficiency	η	V_{in} = +5V, I_o = 3.0A	$V_o \geq 3.3V$ V_o =2.5V V_o =1.8V V_o =1.5V V_o =1.2V	— — — — —	90 85 78 76 67	— — — — —	%
		V_{in} = +5V, I_o = 8.0A	$V_o \geq 3.3V$ V_o =2.5V V_o =1.8V V_o =1.5V V_o =1.2V	— — — — —	83 76 74 68 65	— — — — —	%
Switching Frequency	f_o	Over V_{in} and I_o ranges		475	600	725	kHz
Absolute Maximum Operating Temperature Range	T_a			–40 (3)	—	+85 (4)	°C
Thermal Resistance	θ_{ja}	Free Air Convection (40-60LFM)		—	15	—	°C/W

Continued

Specifications *(continued)*

Characteristics (T_a=25°C unless noted)	Symbols	Conditions	PT6500 SERIES Min	Typ	Max	Units
Storage Temperature	T_s	—	-40	—	+125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3, 1msec, half sine, fixture mounted	—	500	—	G's
Mechanical Vibration		Per Mil-STD-883D, Methode 2007.2, 20-20,000 Hz, soldered ina PC board	—	7.5	—	G's
Weight			—	23	—	grams

Notes: (1) *ISR will operate down to no load with reduced specifications.*
(2) *The minimum input voltage required by the part is Vout +1.2V or 3.1V, whichever is greater.*
(3) *For operation below 0°C, use tantalum capacitors. For more information see the related applicatoin note, "PT6000/7000 Series Capacitor Recommendations."*
(4) *See Thermal Derating charts.*

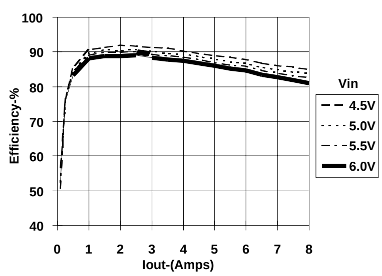
Input/Output Capacitors: *The PT6500 series requires a 330µF electrolytic or tantalum input and output capacitor for proper operation in all applications. C_1 (input) must be rated for 1.2Arms and 100mΩ max. ESR. C_2 (output) must must be rated for 400mArms ripple current and 0.2Ω max. ESR.*

TYPICAL CHARACTERISTICS

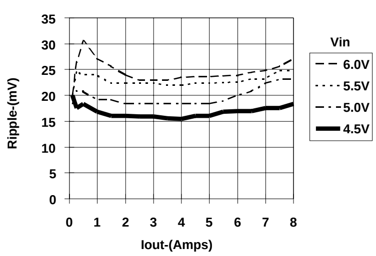
PT6501, 3.3 VDC, V_{in}=5.0V

(See Note A)

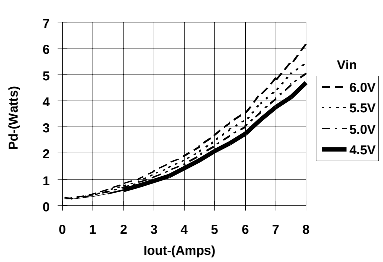
Efficiency vs Output Current



Ripple vs Output Current



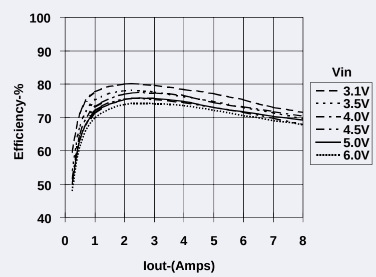
Power Dissipation vs Output Current



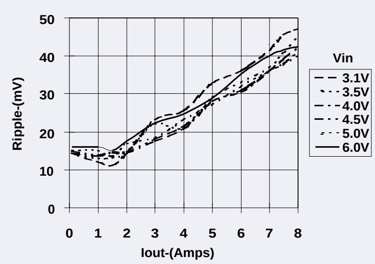
PT6502, 1.5 VDC, V_{in}=5.0V

(See Note A)

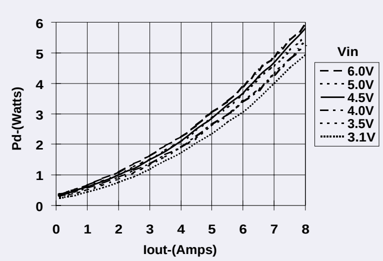
Efficiency vs Output Current



Ripple vs Output Current



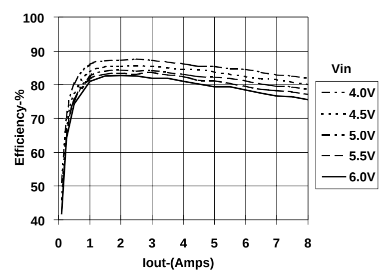
Power Dissipation vs Output Current



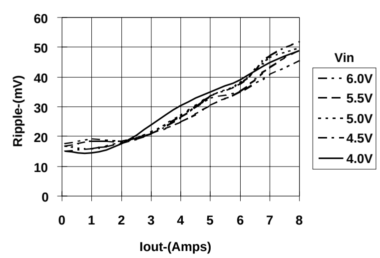
PT6503, 2.5 VDC, V_{in}=5.0V

(See Note A)

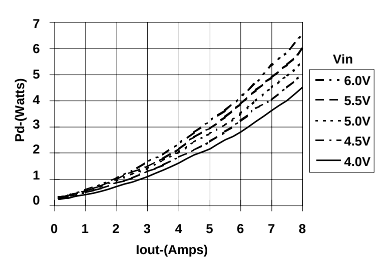
Efficiency vs Output Current



Ripple vs Output Current



Power Dissipation vs Output Current



Note A: *All data listed in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*

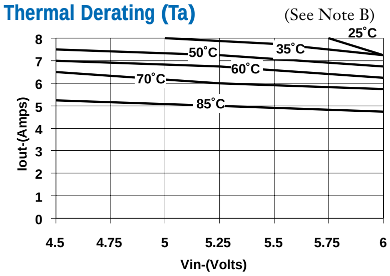
THERMAL DERATING CURVES

Air Flow (LFM)		
60	200	300

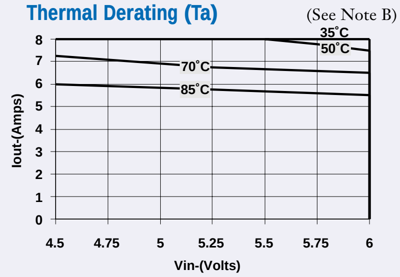
PT6501

No Heat Tab

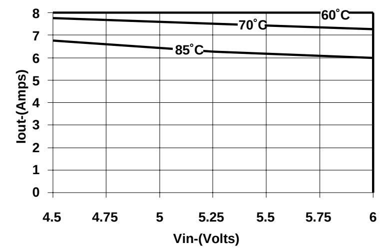
Thermal Derating (Ta) (See Note B)



Thermal Derating (Ta) (See Note B)

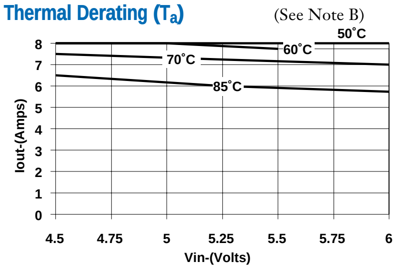


Thermal Derating (Ta) (See Note B)

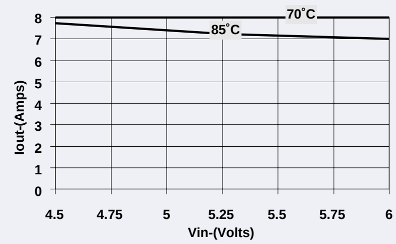


Heat Tab

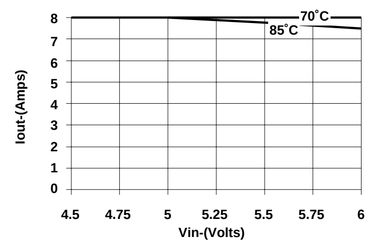
Thermal Derating (T_a) (See Note B)



Thermal Derating (T_a) (See Note B)



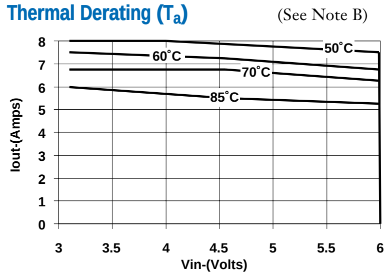
Thermal Derating (T_a) (See Note B)



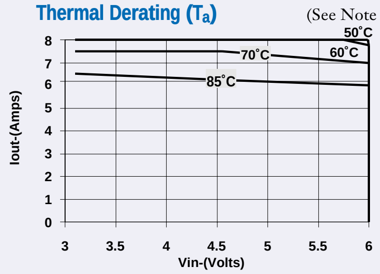
PT6502

No Heat Tab

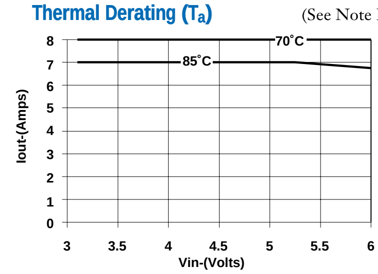
Thermal Derating (T_a) (See Note B)



Thermal Derating (T_a) (See Note B)

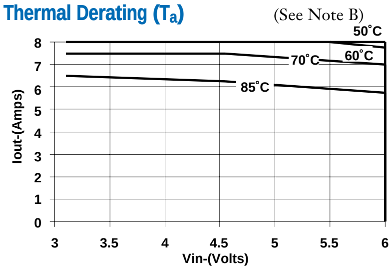


Thermal Derating (T_a) (See Note B)

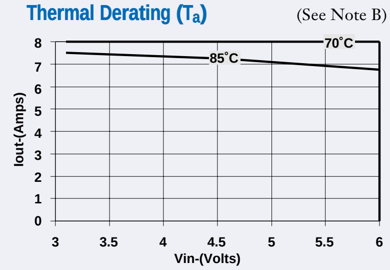


Heat Tab

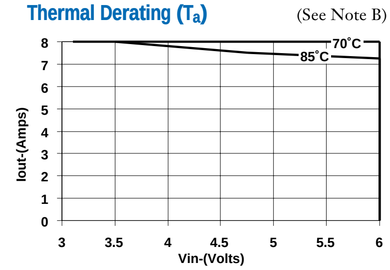
Thermal Derating (T_a) (See Note B)



Thermal Derating (T_a) (See Note B)



Thermal Derating (T_a) (See Note B)



Note B: *Thermal derating graphs are developed in different air flow rates as indicated on each graph, with or without the heat tab, soldered in a printed circuit board.*

THERMAL DERATING CURVES

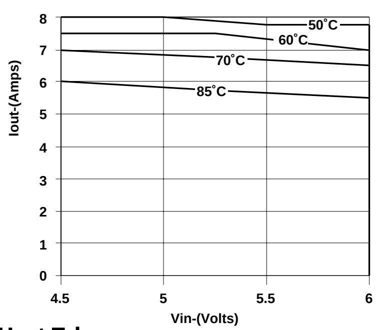
Air Flow (LFM)

60	200	300

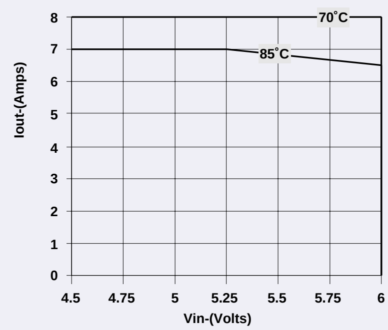
PT6503

No Heat Tab

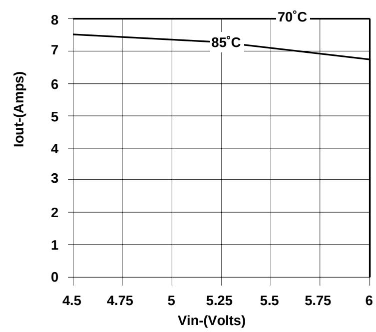
Thermal Derating (Ta) (See Note B)



Thermal Derating (Ta) (See Note B)

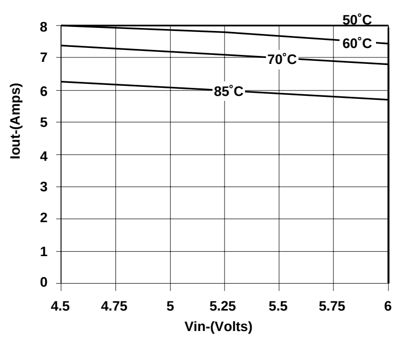


Thermal Derating (Ta) (See Note B)

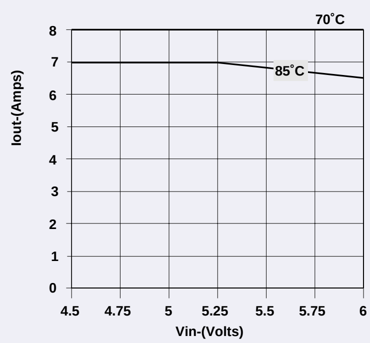


Heat Tab

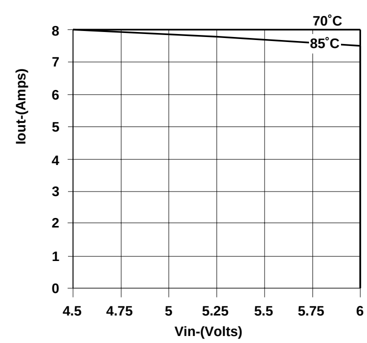
Thermal Derating (Ta) (See Note B)



Thermal Derating (Ta) (See Note B)



Thermal Derating (Ta) (See Note B)



Note B: *Thermal derating graphs are developed in different air flow rates as indicated on each graph, with or without the heat tab, soldered in a printed circuit board.*

Adjusting the Output Voltage of the PT6500 5V/3.3V Bus Converters

The output voltage of the Power Trends PT6500 Series ISRs may be adjusted higher or lower than the factory trimmed pre-set voltage with the addition of a single external resistor. Table 1 accordingly gives the allowable adjustment range for each model in the series as V_a (min) and V_a (max).

Adjust Up: An increase in the output voltage is obtained by adding a resistor R2, between pin 14 (V_o adjust) and pins 7-10 (GND).

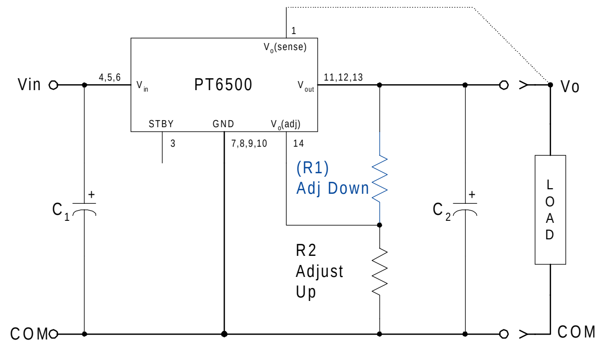
Adjust Down: Add a resistor (R1), between pin 14 (V_o adjust) and pins 11-13 (V_{out}).

Refer to Figure 1 and Table 2 for both the placement and value of the required resistor, either (R1) or R2 as appropriate.

Notes:

1. Use only a single 1% resistor in either the (R1) or R2 location. Place the resistor as close to the ISR as possible.
2. Never connect capacitors from V_o adjust to either GND, V_{out}, or the Remote Sense pin. Any capacitance added to the V_o adjust pin will affect the stability of the ISR.
3. If the Remote Sense feature is being used, connecting the resistor (R1) between pin 14 (V_o adjust) and pin 1 (Remote Sense) can benefit load regulation.
4. The minimum input voltage required by the part is V_{out} + 1.2 or V_{in}(min) from Table 1, whichever is higher.

Figure 1



The values of (R1) [adjust down], and R2 [adjust up], can also be calculated using the following formulae.

$$(R1) = \frac{R_o (V_a - 1.0)}{(V_o - V_a)} - R_s \quad k\Omega$$

$$R2 = \frac{R_o}{V_a - V_o} - R_s \quad k\Omega$$

Where: V_o = Original output voltage
V_a = Adjusted output voltage
R_o = The resistance value in Table 1
R_s = The series resistance from Table 1

Table 1

PT6500 ADJUSTMENT AND FORMULA PARAMETERS

Series Pt #	PT6505	PT6507	PT6502	PT6508	PT6506	PT6503	PT6501	PT6504
V_o (nom)	1.2	1.3	1.5	1.7	1.8	2.5	3.3	3.6
V_a (min)	1.14	1.19	1.27	1.36	1.4	1.8	2.25	2.5
V_a (max)	2.35	2.45	2.65	2.85	2.95	3.5	4.2	4.3
R_o (kΩ)	2.49	2.49	2.49	2.49	2.49	4.99	12.1	10.0
R_s (kΩ)	2.0	2.0	2.0	2.0	2.0	4.22	12.1	12.1
V_{in}(min)	3.1	3.1	3.1	3.1	3.1	4.5	4.5	4.5

Table 2

PT6500 ADJUSTMENT RESISTOR VALUES

Series Pt #	PT6505	PT6507	PT6502	PT6508	PT6506	PT6503	PT6501	PT6504
V_o (nom)	1.2	1.3	1.5	1.7	1.8	2.5	3.3	3.6
V_a (req'd)								
1.15	(5.5)kΩ							
1.2		(3.0)kΩ						
1.25	47.8kΩ	(10.5)kΩ						
1.3	22.9kΩ		(1.7)kΩ					
1.35	14.6kΩ	47.8kΩ	(3.8)kΩ					
1.4	10.5kΩ	22.9kΩ	(8.0)kΩ	(1.3)kΩ	(0.5)kΩ			
1.45	8.0kΩ	14.6kΩ	(20.4)kΩ	(2.5)kΩ	(1.2)kΩ			
1.5	6.3kΩ	10.5kΩ		(4.2)kΩ	(2.2)kΩ			
1.55	5.1kΩ	8.0kΩ	47.8kΩ	(7.1)kΩ	(3.5)kΩ			
1.6	4.2kΩ	6.3kΩ	22.9kΩ	(12.9)kΩ	(5.5)kΩ			
1.65	3.5kΩ	4.1kΩ	14.6kΩ	(30.4)kΩ	(8.8)kΩ			
1.7	3.0kΩ	4.2kΩ	10.5kΩ		(15.4)kΩ			
1.75	2.5kΩ	3.5kΩ	8.0kΩ	47.8kΩ	(35.4)kΩ			
1.8	2.2kΩ	3.0kΩ	6.3kΩ	22.9kΩ		(1.5)kΩ		
1.85	1.8kΩ	2.5kΩ	5.1kΩ	14.6kΩ	47.8kΩ	(2.3)kΩ		
1.9	1.6kΩ	2.2kΩ	4.2kΩ	10.5kΩ	22.9kΩ	(3.3)kΩ		
1.95	1.3kΩ	1.8kΩ	3.5kΩ	8.0kΩ	14.6kΩ	(4.4)kΩ		
2.0	1.1kΩ	1.6kΩ	3.0kΩ	6.3kΩ	10.5kΩ	(5.8)kΩ		
2.05	0.9kΩ	1.3kΩ	2.5kΩ	5.1kΩ	8.0kΩ	(7.4)kΩ		
2.1	0.8kΩ	1.1kΩ	2.2kΩ	4.2kΩ	6.3kΩ	(9.5)kΩ		
2.15	0.6kΩ	0.9kΩ	1.8kΩ	3.5kΩ	5.1kΩ	(12.2)kΩ		
2.2	0.5kΩ	0.8kΩ	1.6kΩ	3.0kΩ	4.2kΩ	(15.7)kΩ		
2.25	0.4kΩ	0.6kΩ	1.3kΩ	2.5kΩ	3.5kΩ	(20.7)kΩ	(2.3)kΩ	
2.3	0.3kΩ	0.5kΩ	1.1kΩ	2.2kΩ	3.0kΩ	(28.2)kΩ	(3.6)kΩ	
2.35	0.2kΩ	0.4kΩ	0.9kΩ	1.8kΩ	2.5kΩ	(40.7)kΩ	(5.1)kΩ	
2.4		0.3kΩ	0.8kΩ	1.6kΩ	2.2kΩ	(65.6)kΩ	(6.7)kΩ	
2.45		0.2kΩ	0.6kΩ	1.3kΩ	1.8kΩ	(140.0)kΩ	(8.5)kΩ	
2.5			0.5kΩ	1.1kΩ	1.6kΩ		(10.6)kΩ	(1.5)kΩ
2.55			0.4kΩ	0.9kΩ	1.3kΩ	95.6kΩ	(12.9)kΩ	(2.7)kΩ
2.6			0.3kΩ	0.8kΩ	1.1kΩ	45.7kΩ	(15.6)kΩ	(3.9)kΩ
2.65			0.2kΩ	0.6kΩ	6.9kΩ	29.0kΩ	(18.6)kΩ	(5.3)kΩ
2.7				0.5kΩ	0.8kΩ	20.7kΩ	(22.2)kΩ	(6.8)kΩ
2.75				0.4kΩ	0.6kΩ	15.7kΩ	(26.4)kΩ	(8.5)kΩ
2.8				0.3kΩ	0.5kΩ	12.4kΩ	(31.5)kΩ	(10.4)kΩ
2.85				0.2kΩ	0.4kΩ	10.0kΩ	(37.6)kΩ	(12.6)kΩ
2.9					0.3kΩ	8.3kΩ	(45.4)kΩ	(15.0)kΩ
2.95					0.2kΩ	0.9kΩ	(55.3)kΩ	(17.9)kΩ
3.0						5.8kΩ	(68.6)kΩ	(21.2)kΩ
3.1						4.1kΩ	(115.0)kΩ	(29.9)kΩ
3.2						2.9kΩ	(254.0)kΩ	(42.9)kΩ
3.3						2.0kΩ		(64.6)kΩ
3.4						1.3kΩ	109.0kΩ	(108.0)kΩ
3.5						0.8kΩ	48.4kΩ	(238.0)kΩ
3.6							28.2kΩ	
3.7							18.2kΩ	87.9kΩ
3.8							12.1kΩ	37.9kΩ
3.9	4/. V_{out} >3.8Vdc requires V_{in} >5.0Vdc !						8.1kΩ	21.2kΩ
4.0							5.2kΩ	12.9kΩ
4.1							3.0kΩ	7.9kΩ
4.2							1.3kΩ	4.6kΩ
4.3								2.2kΩ

R1 = (Blue) R2 = Black

Using the Standby Function on the PT6500 5V/3.3V Bus Converters

For applications requiring output voltage On/Off control, the 14-pin PT6500 ISR series incorporates a standby function. This function may be used in applications that require power-up/shutdown sequencing, and wherever there is a requirement for the output status of the module to be controlled by external circuitry.

The standby function is provided by the *STBY** control, pin 3. If pin 3 is left open-circuit the regulator operates normally, and provides a regulated output when a valid supply voltage is applied to V_{in} (pins 4, 5, & 6) with respect to GND (pins 7-10). If a low voltage[2] is then applied to pin-3 the regulator output will be disabled and the input current drawn by the ISR will drop to less than 50mA[4]. The standby control may also be used to hold-off the regulator output during the period that input power is applied.

The standby control pin is ideally controlled using an open-collector (or open-drain) discrete transistor (See Figure 1). It may also be driven directly from a dedicated TTL[3] compatible gate. Table 1 provides details of the threshold requirements.

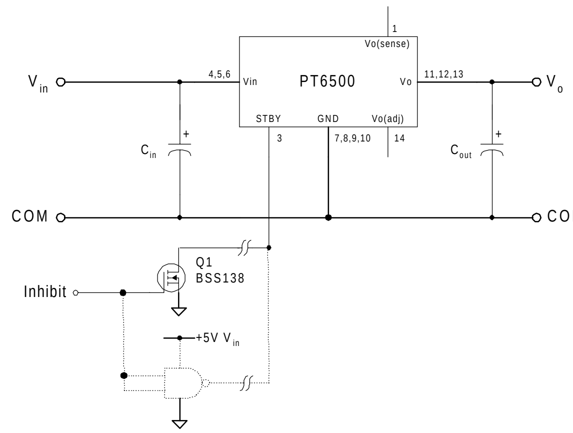
Table 1 Inhibit Control Thresholds [(2,3)]

Parameter	Min	Max
Enable (V_{IH})	1V	5V
Disable (V_{IL})	–0.1V	0.35V

Notes:

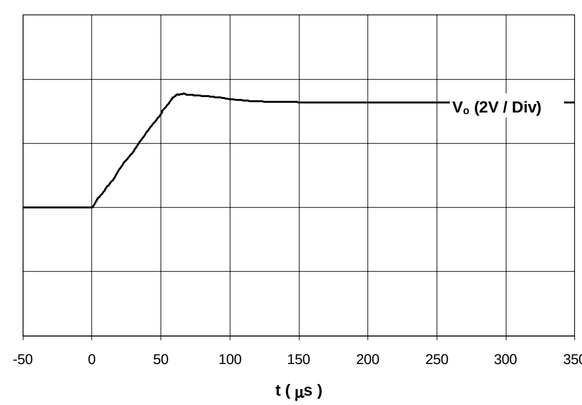
1. The Standby/Inhibit control logic is similar for all Power Trends' modules, but the flexibility and threshold tolerances will be different. For specific information on this function for other regulator models, consult the applicable application note.
2. The Standby control pin is ideally controlled using an open-collector (or open-drain) discrete transistor and requires no external pull-up resistor. The control input has an open-circuit voltage of about 1Vdc. To disable the regulator output, the control pin must be pulled to less than 0.35Vdc with a low-level 0.5mA sink to ground.
3. The Standby input on the PT6500 series may be driven by a differential output device, making it compatible with TTL logic. A standard TTL logic gate will meet the 0.35V V_{IL}(max) requirement (Table 1) at 0.5mA I_{OL}. *Do not* use devices that can drive the Standby control input above 5Vdc.
4. When the regulator output is disabled the current drawn from the input source is reduced to approximately 30–40mA (50mA maximum).

Figure 1



Turn-On Time: In the circuit of Figure 1, turning Q_1 on applies a low voltage to the Standby control (pin 3) and disables the regulator ouput. Correspondingly, turning Q_1 off releases the low-voltage signal and enables the output. The PT6500 ISR series regulators have a fast response and will provide a fully regulated output voltage within 250 µsec. The actual turn-on time will vary with load and the total amount of output capacitance. The waveform of Figure 2 shows the typical output voltage response of a PT6501 (3.3V) following the turn-off of Q_1 at time t = 0.0 secs. The waveform was measured with a 5Vdc input voltage, and 0.6Ω load.

Figure 2



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
PT6501A	LIFEBUY	SIP MODULE	EEA	14	12	TBD	Call TI	Level-1-215C-UNLIM	
PT6501B	LIFEBUY	SIP MODULE	EEK	14	12	TBD	Call TI	Level-1-215C-UNLIM	
PT6501C	OBSOLETE	SIP MODULE	EEC	14		TBD	Call TI	Call TI	
PT6501G	LIFEBUY	SIP MODULE	EEG	14	12	TBD	Call TI	Level-1-215C-UNLIM	
PT6501H	LIFEBUY	SIP MODULE	EEH	14	12	TBD	Call TI	Level-1-215C-UNLIM	
PT6501L	LIFEBUY	SIP MODULE	EEL	14	12	TBD	Call TI	Level-1-215C-UNLIM	
PT6501R	LIFEBUY	SIP MODULE	EEE	14	12	TBD	Call TI	Level-1-215C-UNLIM	
PT6502A	OBSOLETE	SIP MODULE	EEA	14		TBD	Call TI	Call TI	
PT6502B	LIFEBUY	SIP MODULE	EEK	14	12	TBD	Call TI	Level-1-215C-UNLIM	
PT6502G	LIFEBUY	SIP MODULE	EEG	14	12	TBD	Call TI	Level-1-215C-UNLIM	
PT6503A	LIFEBUY	SIP MODULE	EEA	14	12	TBD	Call TI	Level-1-215C-UNLIM	
PT6503B	LIFEBUY	SIP MODULE	EEK	14	12	TBD	Call TI	Level-1-215C-UNLIM	
PT6503C	OBSOLETE	SIP MODULE	EEC	14		TBD	Call TI	Call TI	
PT6504B	LIFEBUY	SIP MODULE	EEK	14	12	TBD	Call TI	Level-1-215C-UNLIM	
PT6506A	LIFEBUY	SIP MODULE	EEA	14	12	TBD	Call TI	Level-1-215C-UNLIM	
PT6506B	LIFEBUY	SIP MODULE	EEK	14	12	TBD	Call TI	Level-1-215C-UNLIM	
PT6506C	LIFEBUY	SIP MODULE	EEC	14	12	TBD	Call TI	Level-1-215C-UNLIM	
PT6506E	OBSOLETE	SIP MODULE	EEC	14		TBD	Call TI	Call TI	
PT6506F	OBSOLETE	SIP MODULE	EEF	14		TBD	Call TI	Call TI	
PT6506N	OBSOLETE	SIP MODULE	EED	14		TBD	Call TI	Call TI	
PT6507A	OBSOLETE	SIP MODULE	EEA	14		TBD	Call TI	Call TI	
PT6507B	OBSOLETE	SIP MODULE	EEK	14		TBD	Call TI	Call TI	
PT6507C	OBSOLETE	SIP MODULE	EEC	14		TBD	Call TI	Call TI	
PT6507F	OBSOLETE	SIP MODULE	EEF	14		TBD	Call TI	Call TI	
PT6507G	OBSOLETE	SIP MODULE	EEG	14		TBD	Call TI	Call TI	
PT6507L	OBSOLETE	SIP MODULE	EEL	14		TBD	Call TI	Call TI	
PT6507M	OBSOLETE	SIP MODULE	EEM	14		TBD	Call TI	Call TI	
PT6507N	OBSOLETE	SIP MODULE	EED	14		TBD	Call TI	Call TI	
PT6507Q	OBSOLETE	SIP MODULE	EEQ	14		TBD	Call TI	Call TI	
PT6507R	OBSOLETE	SIP MODULE	EEE	14		TBD	Call TI	Call TI	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
PT6508A	OBSOLETE	SIP MODULE	EEA	14		TBD	Call TI	Call TI	
PT6508B	OBSOLETE	SIP MODULE	EEK	14		TBD	Call TI	Call TI	
PT6508C	OBSOLETE	SIP MODULE	EEC	14		TBD	Call TI	Call TI	
PT6508F	OBSOLETE	SIP MODULE	EEF	14		TBD	Call TI	Call TI	
PT6508G	OBSOLETE	SIP MODULE	EEG	14		TBD	Call TI	Call TI	
PT6508L	OBSOLETE	SIP MODULE	EEL	14		TBD	Call TI	Call TI	
PT6508M	OBSOLETE	SIP MODULE	EEM	14		TBD	Call TI	Call TI	
PT6508N	OBSOLETE	SIP MODULE	EED	14		TBD	Call TI	Call TI	
PT6508Q	OBSOLETE	SIP MODULE	EEQ	14		TBD	Call TI	Call TI	
PT6508R	OBSOLETE	SIP MODULE	EEE	14		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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