Signetics

PNA7518
8-Bit Multiplying DAC

Product Specification

Linear Products

DESCRIPTION

The PNA7518 is an NMOS 8-bit multiplying digital-to-analog converter (DAC) designed for video applications. The device converts a digital input signal into a voltage-equivalent analog output at a sampling rate of 30MHz.

The input signal is latched, then fed to a decoder which switches a transfer gate array (1 out of 256) to select the appropriate analog signal from a resistor chain. Two external reference voltages supply the resistor chain.

The input latches are positive edge-triggered. The output impedance is approximately 0.5kΩ, depending upon the applied digital code. An additional operational amplifier is required for the full bandwidth. Two's complement is selected when STC (Pin 11) is HIGH or is not connected.

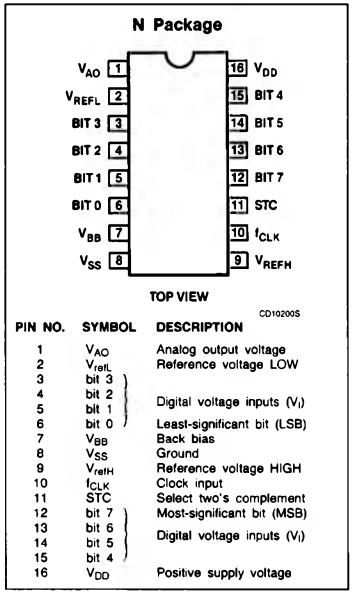
FEATURES

- **TTL input levels**
- **Positive edge-triggered**
- **Analog voltage output at 30MHz sampling rate**
- **Binary or two's complement input**
- **Output voltage accuracy to within ± ½ of the input LSB**

APPLICATIONS

- **Video data conversion**
- **CRT displays**
- **Waveform/test signal generation**
- **Color/black-and-white graphics**

PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	V_{AO}	Analog output voltage
2	V_{refL}	Reference voltage LOW
3	bit 3	Digital voltage inputs (V_I)
4	bit 2	
5	bit 1	
6	bit 0	Least-significant bit (LSB)
7	V_{BB}	Back bias
8	V_{SS}	Ground
9	V_{refH}	Reference voltage HIGH
10	f_{CLK}	Clock input
11	STC	Select two's complement
12	bit 7	Most-significant bit (MSB)
13	bit 6	Digital voltage inputs (V_I)
14	bit 5	
15	bit 4	
16	V_{DD}	Positive supply voltage

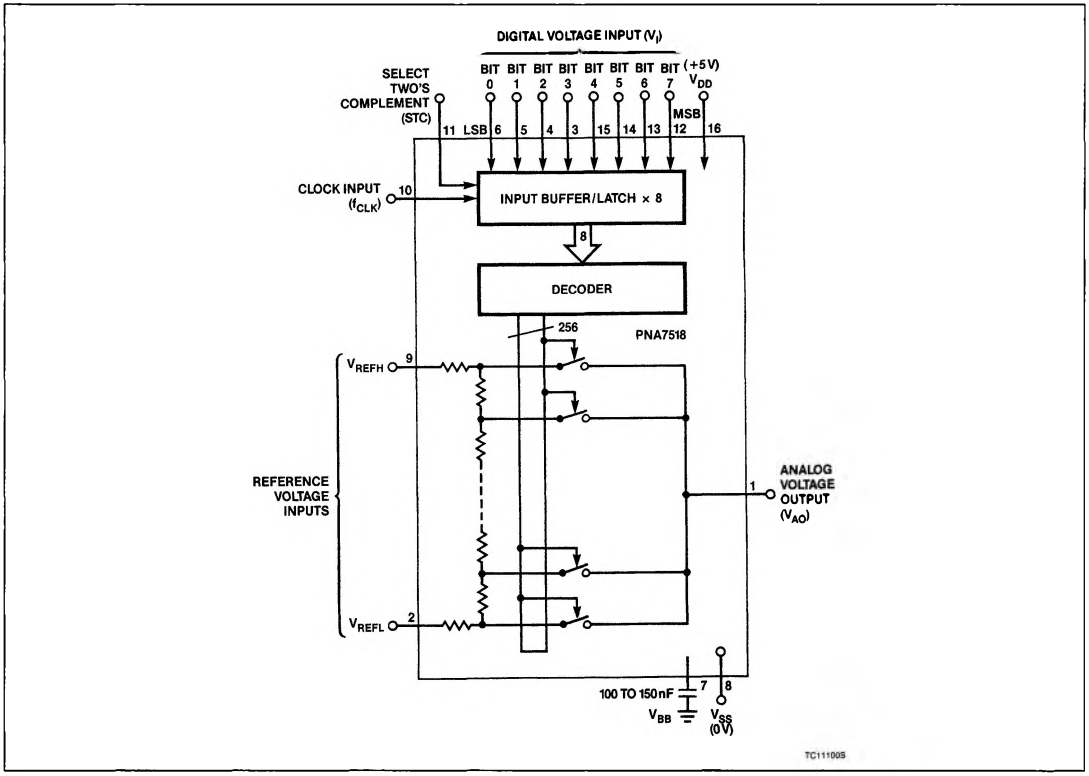
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38WE-1)	0 to +70°C	PNA7518N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (Pin 16)	−0.5 to +7	V
V_I	Input voltage range (Pins 3, 4, 5, 6, 11, 12, 13, 14 and 15)	−0.5 to +7	V
V_{AO}	Output voltage range (Pin 1)	−0.5 to +7	V
P_{TOT}	Total power dissipation	400	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

BLOCK DIAGRAM



HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

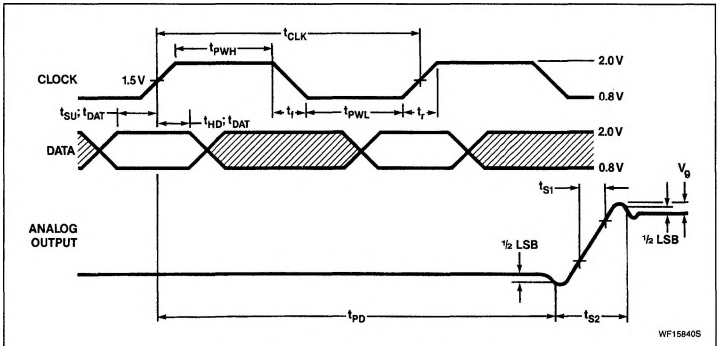


Figure 1. Switching Characteristics

DC ELECTRICAL CHARACTERISTICS V_{DD} = 4.5 to 5.5; V_{SS} = 0V; C_{BB} = 100nF; T_A = 0 to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 16)					
V_{DD}	Supply voltage	4.5	5	5.5	V
I_{DD}	Supply current		50	80	mA
Reference voltages					
V_{REFL}	Reference voltage LOW (Pin 2)	−0.1		+2.1	V
V_{REFH}	Reference voltage HIGH (Pin 9)	−0.1		+2.1	V
R_{REF}	Reference ladder	150	230	300	Ω
Inputs					
	Digital input levels (TTL)[1]				
V_{IL}	input voltage LOW	0		0.8	V
V_{IH}	input voltage HIGH	2.0		5.25	V
I_{LI}	input leakage current			10	μA
	Clock input (Pin 10)				
V_{IL}	input voltage LOW	0		0.8	V
V_{IH}	input voltage HIGH	2.0		5.25	V
I_{LI}	input leakage current			10	μA
Output					
	Analog voltage output (Pin 1)				
V_{AO}	at R_L = 200 kΩ)	0		2	V
BW	Bandwidth (−3 dB) at C_L = 6 pF		12		MHz
Output transients (glitches)[2]					
V_G	Glitch occurring at step 7F-80 (HEX):		3		LSB
	maximum amplitude for 1 LSB change area		23		LSB ns
V_G	Glitch occurring at step 00-AA (HEX):		5		LSB
	maximum amplitude for 1 LSB change area		41		LSB ns
P_{TOT}	Total power dissipation		300		mW

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 to 5.5; V_{SS} = 0V; C_{BB} = 100nF; T_A = 0 to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Clock input (Pin 10)				
f_{CLK}	frequency	1		30	MHz
t_{PWH}	pulse width HIGH	10			ns
t_{PWL}	pulse width LOW	10			ns
t_R	input rise time at f_{CLK} = 30MHz			3	ns
t_F	input fall time at f_{CLK} = 30MHz			3	ns
Switching characteristics (Figure 1)					
t_{SU}, t_{DAT}	Data setup time	3			ns
t_{HD}, t_{DAT}	Data hold time	4			ns
t_{PD}	Propagation delay time, input to output	t_{CLK} + 15	t_{CLK} + 22	t_{CLK} + 30	ns
t_{S1}	Settling time; 10 to 90% full-scale change; C_L = 6pF; R_L = 200kΩ		13	20	ns
t_{S2}	Settling time to ±1 LSB; C_L = 6pF; R_L = 200kΩ		40		ns
	Linearity at R_L = 200kΩ; $V_O = 2V_{P-P}$			± ½	LSB
Influence of clock frequency[2]					
	Cross-talk at 2 × f_{CLK}				
	amplitude		2		LSB
	area		8		LSB ns

NOTES:

1. Inputs Bit 0 to Bit 7 are positive edge-triggered and STC.
2. Measured at $V_{REFH} - V_{REFL}$ = 2.0 V; 1 × LSB = 7.8mV. The energy equivalent of output transients is given as the area contained by the graph of output amplitude (LSB) against time (ns). The glitch area is independent of the value of V_{REF}. Glitch amplitudes and clock cross-talk can be reduced by using a shielded printed circuit board (see Pin Configuration).