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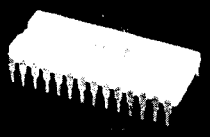


PCM58P

Precision, 18-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

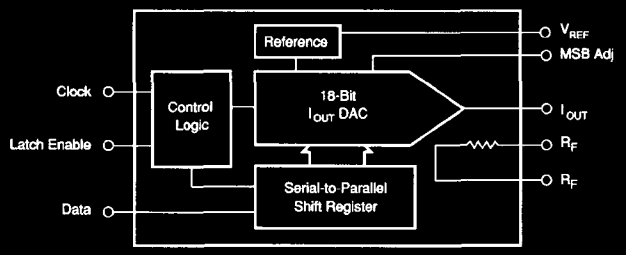
FEATURES

- 18-BIT MONOLITHIC AUDIO D/A CONVERTER
- VERY LOW MAX THD+N: –96dB Without External Adjustment; PCM58P-K
- SERIAL INPUT FORMAT 100% COMPATIBLE WITH INDUSTRY STD 16-BIT PCM56P
- VERY FAST SETTLING, GLITCH-FREE CURRENT OUTPUT (200ns)
- LOW-NOISE SCHMITT TRIGGER LOGIC INPUT CIRCUITRY
- COMPLETE WITH REFERENCE
- RELIABLE PLASTIC 28-PIN DIP PACKAGE

DESCRIPTION

The PCM58P is a complete, precision 18-bit digital-to-analog converter with ultra-low distortion over a very wide frequency range. The latched serial input data format of the PCM58P is totally based on the widely successful 16-bit PCM56P format (with the addition of two more data bits). The PCM58P features a very low noise and fast settling current output.

The PCM58P comes in a 28-pin plastic DIP package. A provision is made for external adjustment of the four MSBs to further improve the PCM58P's specifications, if desired. Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.



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SPECIFICATIONS

ELECTRICAL

All Specifications at 25°C, and $\pm V_{CC}$ = +5.0V and –12.0V unless otherwise noted.

PARAMETER	CONDITIONS	PCM58P /P,J/P,K MIN	TYP	MAX	UNITS
RESOLUTION				18	BITS
DYNAMIC RANGE			108		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2.0		$+V_{CC}$	V
V_{IL}		0.0		0.8	V
I_{IH}	V_{IH} = +2.7V			+1.0	µA
I_{IL}	V_{IL} = +0.4V			–50	µA
Data Format			Serial BTC[1]		
Input Clock Frequency		16.9	20		MHz
DYNAMIC CHARACTERISTICS					
TOTAL HARMONIC DISTORTION + N[2]	Without MSB Adjustments				
PCM58P:					
f = 991Hz (0dB)[3]	f_S = 176.4kHz[4]		–94	–92	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–74	–72	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–40	–34	dB
PCM58P-J:					
f = 991Hz (0dB)	f_S = 176.4kHz		–96	–94	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–80	–74	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–40	–34	dB
PCM58P-K					
f = 991Hz (0dB)	f_S = 176.4kHz		–100	–96	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–82	–80	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–42	–40	dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±1	±2	%
Bipolar Zero Error[5]			±10		mV
Gain Drift	0°C to 70°C		25		ppm/°C
Bipolar Zero Drift	0°C to 70°C		4		ppm of FSR/°C
Warm-up Time		1			Minute
IDLE CHANNEL SNR[6]	20Hz to 20kHz at BPZ[7]		+126		dB
POWER SUPPLY REJECTION			+72		dB
ANALOG OUTPUT					
Output Range		±0.98	±1.0	±1.02	mA
Output Impedance			1.2		kΩ
Internal Feedback			3		kΩ
Settling Time	1mA Step		200		ns
Glitch Energy			Meets all THD+N Specs Without External Deglitching		
POWER SUPPLY REQUIREMENTS					
$+V_{CC}$ Supply Voltage		+4.75	+5.00	+5.50	V
$-V_{CC}$ Supply Voltage		–10.8	–12.0	–13.2	V
Supply Current $+I_{CC}$	$+V_{CC}$ = +5.0V		+10		mA
$-I_{CC}$	$-V_{CC}$ = –12.0V		–30		mA
Power Dissipation			410		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$) / Signal$_{RMS}$. (3) D/A converter output frequency/signal level. (4) D/A converter sample frequency (4 x 44.1kHz; 4 times oversampling). (5) Offset error at bipolar zero. (6) Measured using an OPA27 and 10kΩ feedback and an A-weighted filter. (7) Bipolar Zero.

PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
P1	Decoupling Capacitor	CAP
P2	+Vcc Voltage Supply	$+V_{CC}$
P3	Decoupling Capacitor	CAP
P4	Decoupling Capacitor	CAP
P5	Bipolar Offset Point	BPO
P6	Current DAC I_{OUT}	I_{OUT}
P7	Feedback Resistor	R_{F1}
P8	Analog Common	ACOM
P9	$-V_{CC}$ Voltage Supply	$-V_{CC}$
P10	Feedback Resistor	R_{F2}
P11	Digital Common	DCOM
P12	No Connection	NC
P13	$+V_{CC}$ Voltage Supply	$+V_{CC}$
P14	No Connection	NC
P15	Decoupling Capacitor	CAP
P16	Clock	CLK
P17	DAC Latch Enable	LE
P18	No Connection	NC
P19	Data Input	DATA
P20	$-V_{CC}$ Voltage Supply	$-V_{CC}$
P21	No Connection	NC
P22	No Connection	NC
P23	No Connection	NC
P24	Bit 4 Adjust	B4 ADJ
P25	Bit 3 Adjust	B3 ADJ
P26	Bit 2 Adjust	B2 ADJ
P27	Bit 1 (MSB) Adjust	B1 ADJ
P28	Bit Adjust V_{POT}	V_{POT}

ORDERING INFORMATION

PCM58P -X

Basic Model Number
P: Plastic
Performance Grade Code

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$ Supply Voltages	+6V; −16V
Input Logic Voltage	−1V to $+V_{CC}$
Storage Temperature	−60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM58P	28-Pin Plastic DIP	215
PCM58P, J	28-Pin Plastic DIP	215
PCM58P, K	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

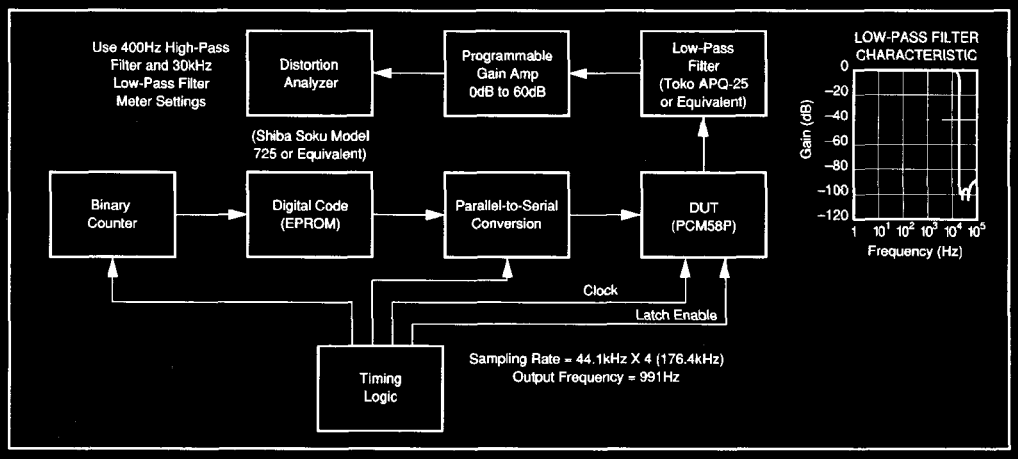


FIGURE 1. PCM58P Production THD+N Test Setup.

DISCUSSION OF SPECIFICATIONS

TOTAL HARMONIC DISTORTION + NOISE

The key specification for the PCM58P is total harmonic distortion plus noise. Digital data words are read into the PCM58P at four times the standard audio sampling frequency of 44.1kHz or 176.4kHz such that a sinewave output of 991Hz is realized. For production testing, the output of the DAC goes to a programmable gain amplifier to provide gain at lower signal output test levels and then through a 20kHz low pass filter before being fed into an analog type distortion analyzer. Figure 1 shows a block diagram of the production THD+N test setup.

In terms of signal measurement, THD+N is the ratio of $Distortion_{RMS}$ + $Noise_{RMS}$ / $Signal_{RMS}$ expressed in dB. For the PCM58P, THD+N is 100% tested at three different output levels using the test setup shown in Figure 1. It is significant to note that this test setup does not include any output deglitching circuitry. This means the PCM58P even meets its –60dB THD+N specification without use of external deglitchers.

ABSOLUTE LINEARITY

Even though absolute integral and differential linearity specs are not given for the PCM58P, the extremely low THD+N performance is typically indicative of 15-bit to 16-bit integral linearity in the DAC depending on the grade specified. The relationship between THD+N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

IDLE CHANNEL SNR

Another appropriate spec for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of the noise on the DAC output at bipolar zero in relation to the full scale range of the DAC. The output of the DAC is band-limited from 20Hz to 20kHz and an A-weighted filter is applied to make this measurement. The idle channel SNR for the PCM58P is typically greater than +126dB, making it ideal for low-noise applications.

OFFSET, GAIN, AND TEMPERATURE DRIFT

Although the PCM58P is primarily meant for use in dynamic applications, specifications are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain drift and offset drift.

TIMING CONSIDERATIONS

The PCM58P accepts TTL-compatible logic input levels. Noise immunity is enhanced by the use of Schmitt trigger input architectures on all input signal lines. The data format of the PCM58P is binary two's complement (BTC) with the most significant bit (MSB) being first in the serial input bit stream. Table I describes the exact input data to voltage output coding relationship. Any number of bits can precede the 18 bits to be loaded as only the last 18 will be transferred to the parallel DAC register after LE (P17; latch enable) has gone low.

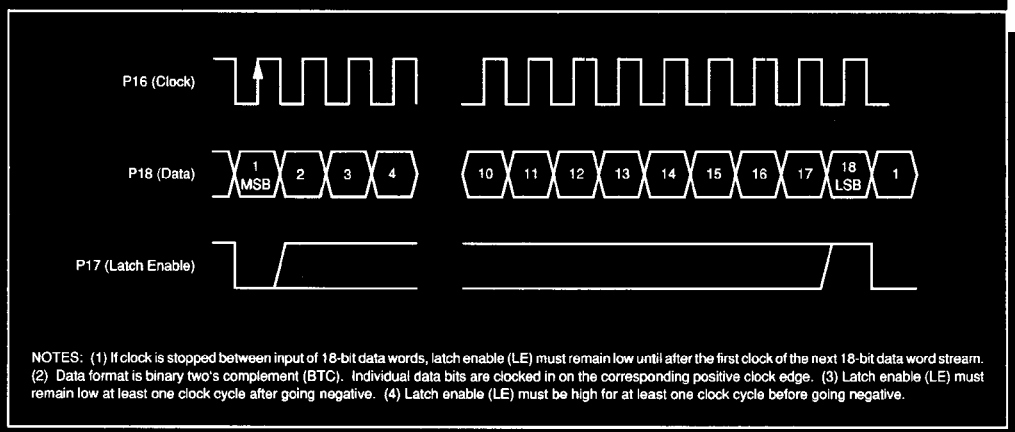
The individual DAC serial input data bit shifts transfer are triggered on positive CLK edges. The serial to parallel data transfer to the DAC occurs on the falling edge of LE (P17). Refer to Figure 2 for graphical relationships of these signals.

MAXIMUM CLOCK RATE

The maximum clock rate of 16.9mHz for the PCM58P is derived by multiplying the standard audio sample rate of 44.1kHz times sixteen (16X oversampling) times the standard audio word bit length of 24 (44.1kHz x 16 x 24 = 16.9mHz). Note that this clock rate accommodates a 24-bit word length, even though only 18 bits are actually being used.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V) V_{OUT} Mode	Current (mA) I_{OUT} Mode
3FFFF Hex	+FS	+2.9999943	–0.9999981
20000 Hex	BPZ	0.0000000	0.0000000
1FFFF Hex	BPZ – 1LSB	–0.0000057	+0.0000019
00000 Hex	–FS	–3.0000000	+1.0000000

TABLE I. PCM60P Input/Output Relationships.



NOTES: (1) If clock is stopped between input of 18-bit data words, latch enable (LE) must remain low until after the first clock of the next 18-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 2. PCM58P Timing Diagram.

"STOPPED-CLOCK" OPERATION

The PCM58P is normally operated with a continuous clock input signal. If the clock is to be stopped in between input data words, the last 18-bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until LE (latch enable) goes low. If the clock input (P16, CLK) is stopped between data words, LE (P17) must remain low until after the first clock cycle of the next data word to insure proper DAC operation. In either case, the setup and hold times for DATA and LE must still be observed as shown in Figure 3.

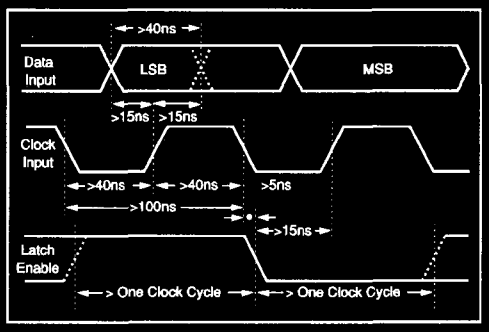


FIGURE 3. PCM58P Setup and Hold Timing Diagram.

INSTALLATION

Refer to Figure 4 for proper connection of the PCM58P in the voltage-out mode using the internal feedback resistor. The feedback resistor connections (P7 and P10) should be connected to ACOM (P8) if not used. The PCM58P requires only a +5V and –12V supply. It is very important that these supplies be as "clean" as possible to reduce coupling of supply noise to the output. Power supply decoupling capacitors shown in Figure 4 should be used, regardless of how good the supplies are to maximize power supply rejection. All grounds should be connected to the analog ground plane as close to the PCM58P as possible.

FILTER CAPACITOR REQUIREMENTS

As shown in Figure 4, other various decoupling capacitors are required around the supply and reference points with no special tolerances being required. Placement of all capacitors should be as close to the appropriate pins of the PCM58P as possible to reduce noise pickup from surrounding circuitry.

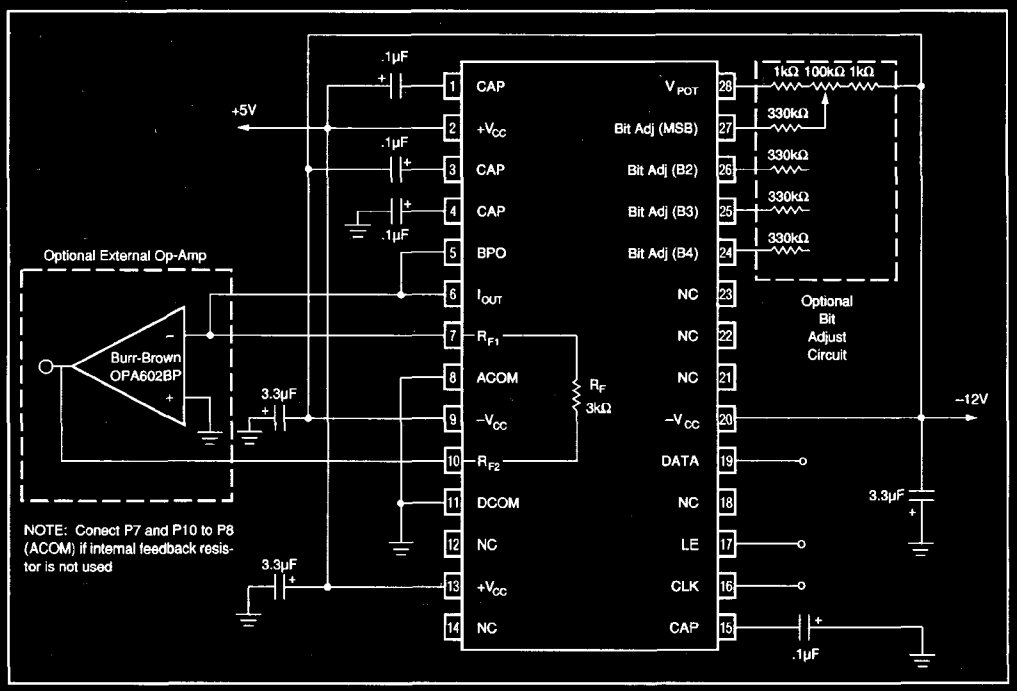


FIGURE 4. PCM58P Connection Diagram.

MSB ADJUSTMENT CIRCUITRY

With the optional bit adjustment circuitry shown in Figure 4, even greater performance can be realized by reducing the first four major bit carry output errors to zero. The most important adjustment for low level outputs would be the step between BPZ (bipolar zero; MSB on, all other bits off) and the code, which is one LSB less than BPZ (MSB off, all other bits on), since every crossing of zero would go through this bipolar major carry point. This MSB bit adjustment would be made by outputing a very low level signal sine wave and calibrating the 100kΩ potentiometer circuit connected to P28 and P27 while monitoring the THD+N of the PCM58P until peak performance is observed.

Bits 2 through 4 can also be adjusted if desired to obtain optimum full-scale output THD+N performance. An additional 100kΩ potentiometer adjustment circuit is required for every additional bit to be adjusted. If bit adjustment is not performed, the respective pins on the PCM58P should be left open.

Once bit adjustment is performed, the reference voltage at VPOT (P28) will track the internal reference, insuring that the THD+N performance of the PCM58P will remain unaffected by external temperature changes.