

PCF8571 1K Serial RAM

Product Specification

Linear Products

DESCRIPTION

The PCF8571 is a low power 1024-bit static CMOS RAM organized as 128 words by 8 bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins — A0, A1, and A2 — are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

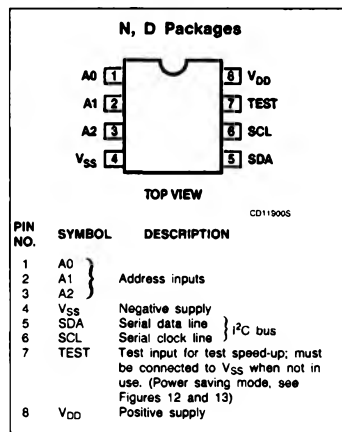
FEATURES

- Operating supply voltage: 2.5V to 6V
- Low data retention voltage: min. 1.0V
- Low standby current: max. 5 μ A
- Power saving mode: typ. 50nA
- Serial input/output bus (I^2C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIP package

APPLICATIONS

- Telephony
RAM expansion for stored numbers in repertory dialing (e.g., PCD3340 applications)
- Radio and television channel presets
- Video cassette recorder
- General purpose
RAM expansion for the micro-computer families MAB8400 and PCF84C00

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP (SOT-97A)	-25°C to +70°C	PCF8571PN
8-Pin Plastic SO (SOL-8; SOT-176)	-25°C to +70°C	PCF8571TD

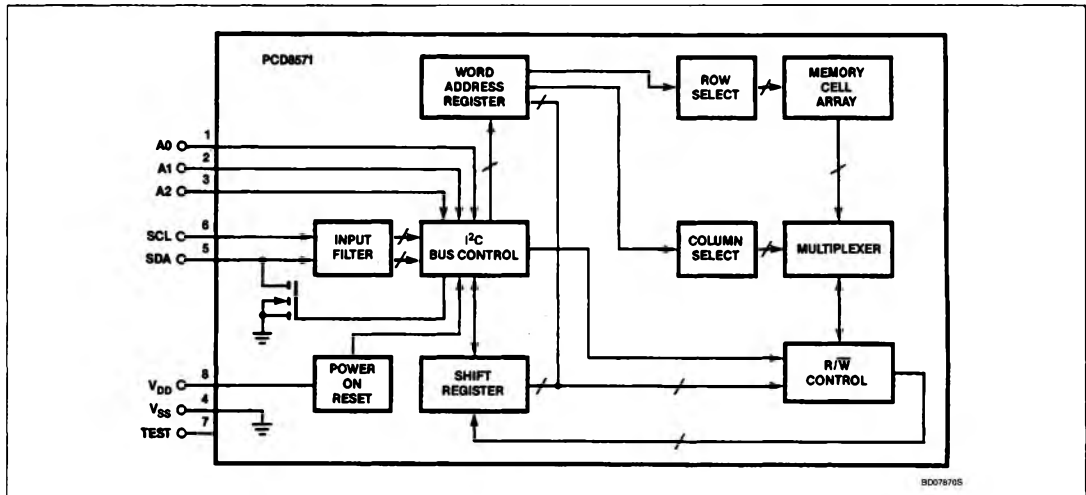
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V _{DD}	Supply voltage range (Pin 8)	-0.8 to +8.0	V
V _I	Voltage range on any input	-0.8 to V _{DD} + 0.8	V
±I _I	DC input current (any input)	10	mA
±I _O	DC output current (any output)	10	mA
±I _{DD} ; I _{SS}	Supply current (Pin 4 or Pin 8)	50	mA
P _{TOT}	Power dissipation per package	300	mW
P _O	Power dissipation per output	50	mW
T _{STG}	Storage temperature range	-65 to +150	°C
T _A	Operating ambient temperature range	-25 to +70	°C

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BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $V_{DD} = 2.5$ to $6V$; $V_{SS} = 0V$; $T_A = -25^\circ C$ to $+70^\circ C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Supply voltage	2.5		6	V
I_{DD} I_{DDO}	Supply current at $f_{SCL} = 100kHz$; $V_I = V_{SS}$ or V_{DD} operating standby			200 5	μA μA
V_{POR}	Power-on reset voltage level at $V_{SCL} = V_{SDA} = V_{DD}^1$	1.5	1.9	2.3	V
Input SCL; input/output SDA					
V_{IL}	Input voltage LOW ²	-0.8		$0.3 \times V_{DD}$	V
V_{IH}	Input voltage HIGH ²	$0.7 \times V_{DD}$		$V_{DD} + 0.8$	V
I_{OL}	Output current LOW at $V_{OL} = 0.4V$	3			mA
I_{OH}	Output leakage current HIGH at $V_{OH} = V_{DD}$			100	nA
$\pm I_I$	Input leakage current (A0, A1, A2) at $V_I = V_{DD}$ or V_{SS}			100	nA
f_{SCL}	Clock frequency (Figure 5)	0		100	kHz
C_I	Input capacitance (SCL, SDA) at $V_I = V_{SS}$			7	pF
t_{sw}	Tolerable spike width on bus			100	ns
LOW V_{DD} data retention					
V_{DDR}	Supply voltage for data retention	1			V
I_{DDR}	Supply current at $V_{DDR} = 1V$			2	μA
Power saving mode (Figure 12)					
I_{DSS}	Supply current at $T_A = 25^\circ C$; $TEST = A0 = A1 = A2 = V_{DDR}$		50	200	nA

NOTES:

1. The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$.
2. If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed $\pm 0.5mA$.

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CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a

serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as control signals.

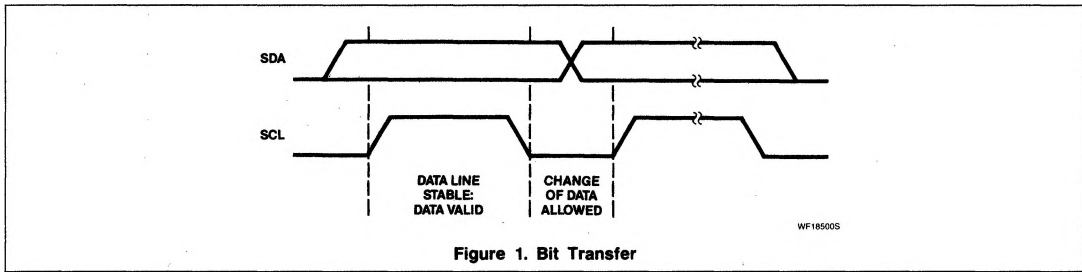


Figure 1. Bit Transfer

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transi-

tion of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the

clock is HIGH is defined as the stop condition (P).

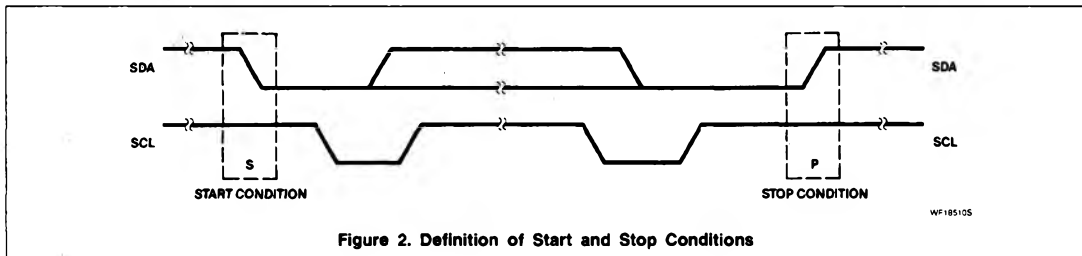


Figure 2. Definition of Start and Stop Conditions

System Configuration

A device generating a message is a "transmitter"; a device receiving a message is the

"receiver". The device that controls the message is the "master" and the devices which

are controlled by the master are the "slaves".

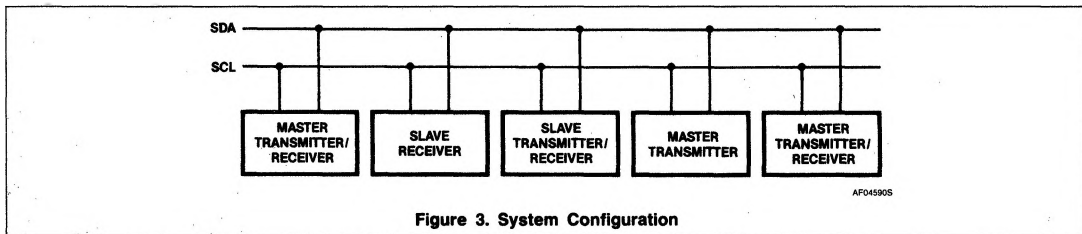


Figure 3. System Configuration

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Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge re-

lated clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW.

During the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end-of-data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

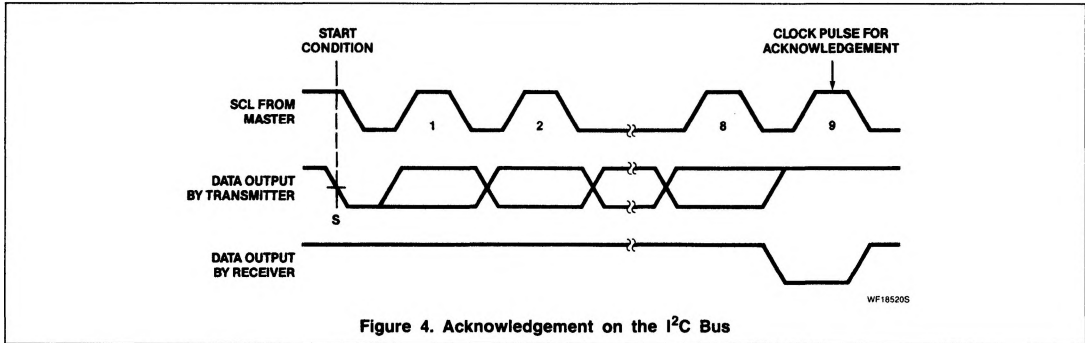


Figure 4. Acknowledgement on the I²C Bus

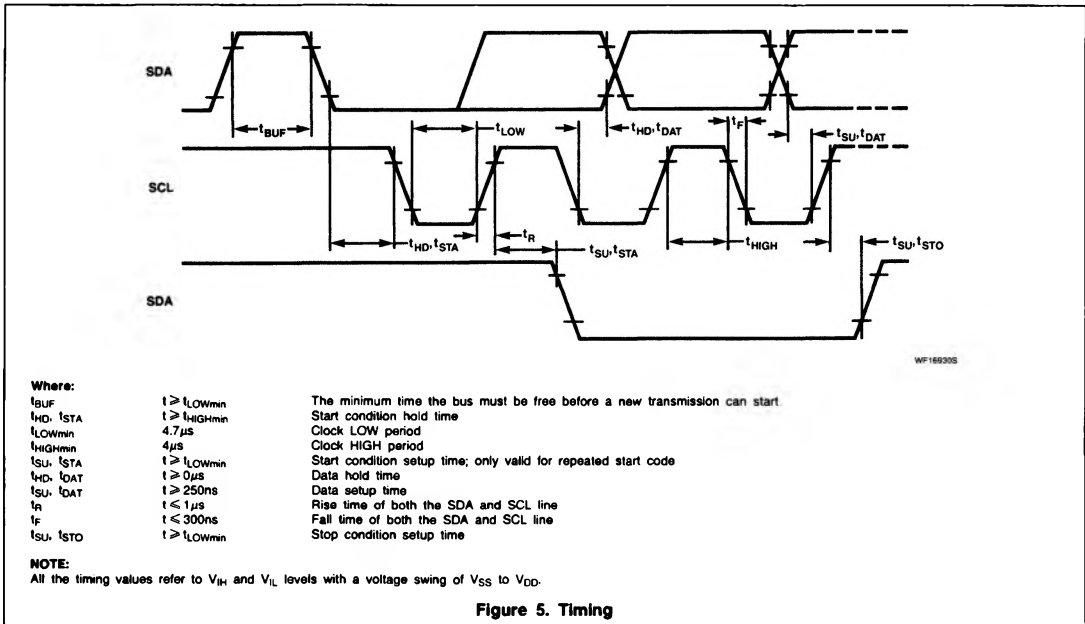
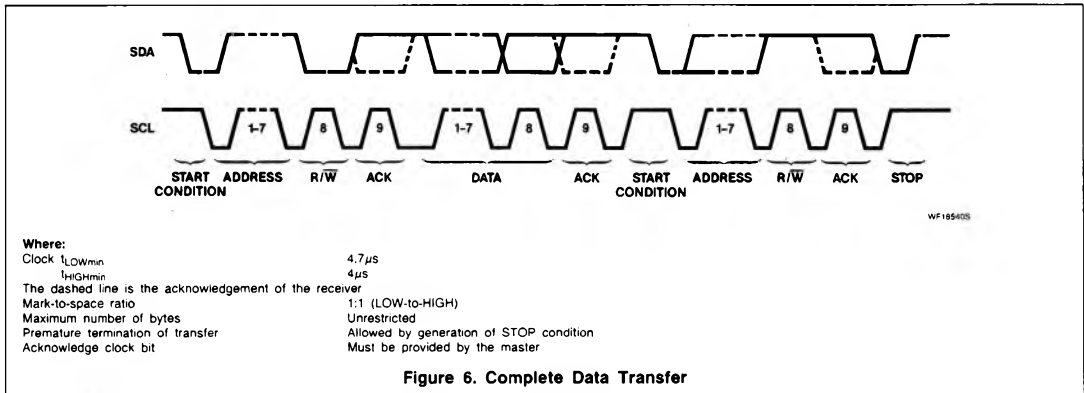


Figure 5. Timing

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Bus Protocol

Before any data is transmitted on the I²C bus, the device which should respond is ad-

ressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for dif-

ferent PCF8571 READ and WRITE cycles is shown in Figure 7.

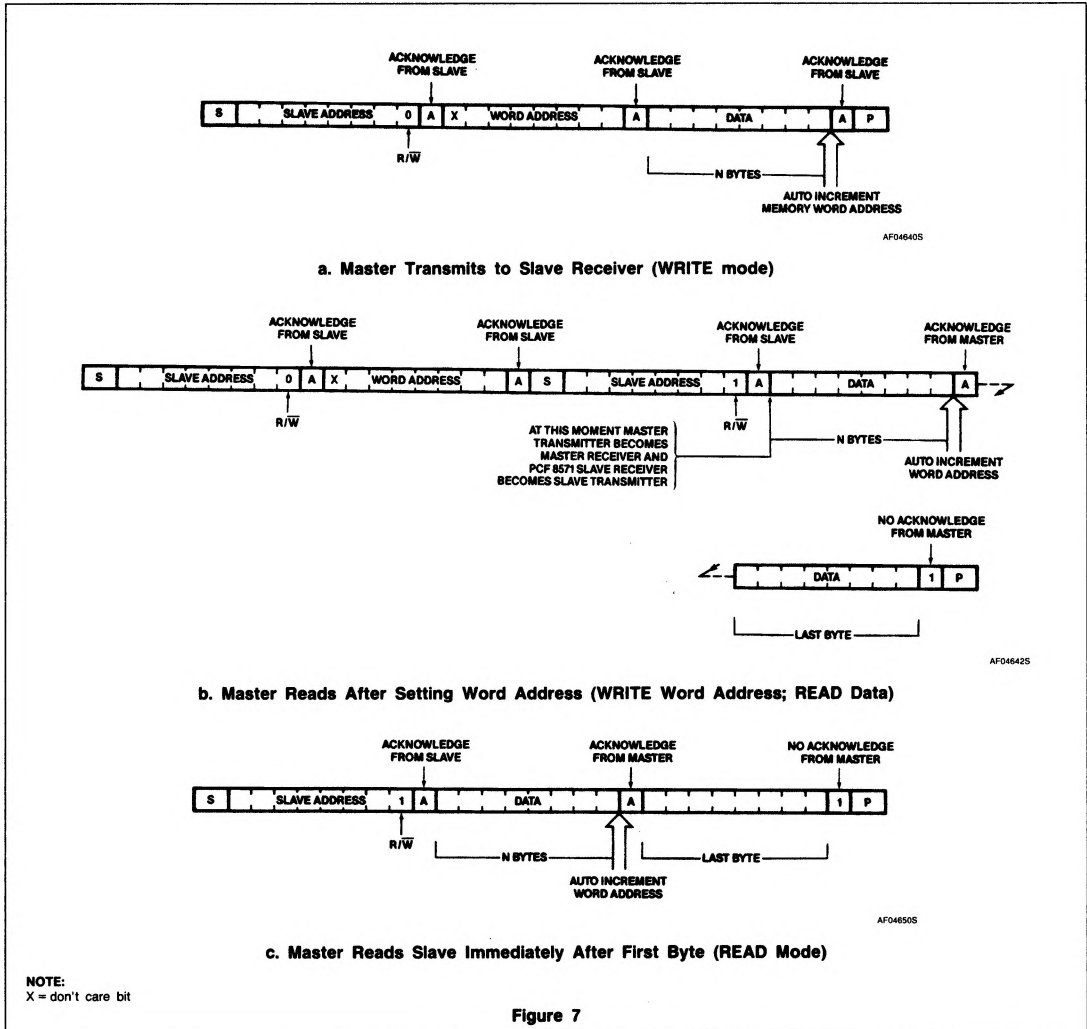


Figure 7

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APPLICATION INFORMATION

The PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Figure 8).

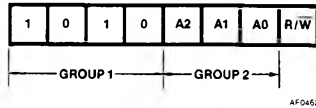
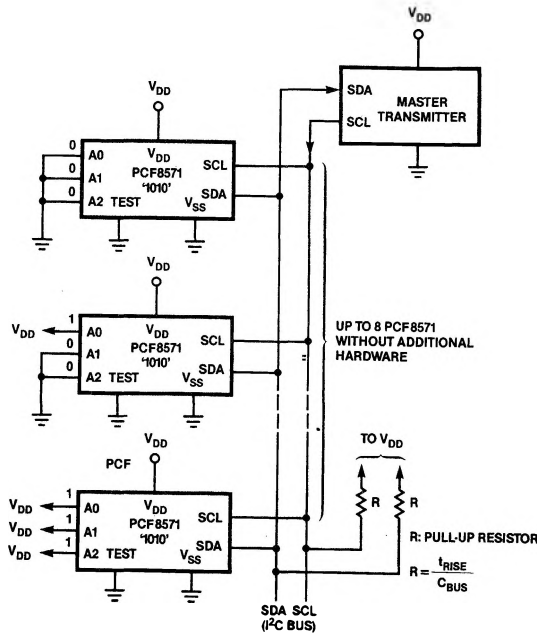


Figure 8. PCF8571 Address



NOTES:
A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

Figure 9. PCF8571 Application Diagram

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POWER SAVING MODE

With the condition TEST = A2 = A1 = A0 = V_{DD}, the PCF8571 goes into the power saving mode.

